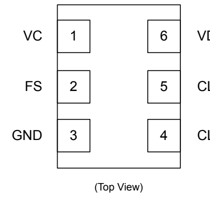
# Ultra Series™ 水晶発振器 (VCXO)
# Si566 データ・シート

## 超低ジッタ・デュアル任意周波数 VCXO (100 fs)、0.2 ～ 3000 MHz

Si566 Ultra Series™ 電圧制御水晶発振器は Silicon Laboratories の高度な第 4 世代 DSPLL® テクノロジーを使用し、超低ジッタ、低位相ノイズのクロックを選択可能な 2 つの周波数で実現します。デバイスは、0.2 ～ 3000 MHz で選択可能な 2 つの周波数に対応するよう、1 ppb 未満の分解能で工場出荷時にプログラムされ、動作範囲全体の整数周波数と分数周波数両方で非常に低いジッタを維持します。オンチップの電源フィルタリングにより、業界最先端の電源ノイズ除去性能を実現しており、スイッチング方式の電源を使用するノイズの多いシステムで、低ジッタ・クロックの生成タスクを簡素化します。Si566 は業界標準の 3.2×5 mm および 5×7 mm フットプリントで提供され、サプライ・チェーンが非常に簡素化されているため、Silicon Labs はカスタム周波数のサンプルを受注後 1 ～ 2 週間で出荷できます。出力周波数ごとに異なる水晶が必要な従来の XO とは違い、Si566 は 1 つの簡単な水晶と DSPLL IC ベースのアプローチで必要な出力周波数を生成します。Si566 は、周波数、出力形式、OE ピン配列/極性など、幅広いユーザ仕様に合わせて工場出荷時に構成できます。カスタム発振器に伴う長いリード・タイムを排除するために、固有の構成は工場出荷時にプログラムされています。


ピン配置



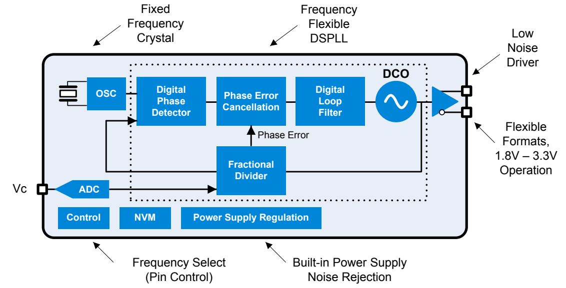

| ピン番号 | 説明 |
|---|---|
| 1 | VC = 電圧制御ピン |
| 2 | FS = 周波数選択 |
| 3 | GND = グランド |
| 4 | CLK+ = クロック出力 |
| 5 | CLK- = 相補クロック出力。CMOS には未使用。 |
| 6 | VDD = 電源 |

**主な機能**

- 200 kHz ～ 3000 MHz で選択可能な 2 つの周波数で利用可能
- 超低ジッタ：100 fs RMS（標準値）（12 kHz ～ 20 MHz）
- 優れた PSRR および電源ノイズ耐久性：-80 dBc（標準値）
- 同じ部品番号から、3.3 V、2.5 V および 1.8 V $V_{DD}$ の電源動作
- LVPECL、LVDS、CML、HCSL、CMOS、およびデュアル CMOS 出力オプション
- 3.2×5、5×7 mm パッケージ・フットプリント
- 1 ～ 2 週間のリード・タイムでサンプルを提供

**アプリケーション**

- 100G/200G/400G OTN、コヒーレント光学
- 10G/25G/40G/100G イーサネット
- 56G/112G PAM4 クロッキング
- 3G-SDI/12G-SDI/24G-SDI 放送ビデオ
- サーバ、スイッチ、ストレージ、NIC、検索の高速化
- テストおよび測定
- FPGA/ASIC クロッキング



# 1. Ordering Guide

The Si566 VCXO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to www.silabs.com/oscillators to access this tool and for further ordering instructions.

| VCXO Series | Description |
|---|---|
| 566 | Dual Frequency VCXO |

| Code | VC Pin | FS Pin |
|---|---|---|
| A | Pin 1 | Pin 2 |

| | Package |
|---|---|
| A | 5x7 mm |
| B | 3.2x5 mm |

| | Temperature Grade |
|---|---|
| G | -40 to 85 °C |

566 A A A - - - - - - A B G R

Device Revision

| Signal Format | VDD Range | Order Option |
|---|---|---|
| LVPECL | 2.5, 3.3 V | A |
| LVDS | 1.8, 2.5, 3.3 V | B |
| CMOS | 1.8, 2.5, 3.3 V | C |
| CML | 1.8, 2.5, 3.3 V | D |
| HCSL | 1.8, 2.5, 3.3 V | E |
| Dual CMOS (In-Phase) | 1.8, 2.5, 3.3 V | F |
| Dual CMOS (Complementary) | 1.8, 2.5, 3.3 V | G |
| Custom[1] | 1.8, 2.5, 3.3 V | X |

| | Temperature Stability = ± 20 ppm | | | |
|---|---|---|---|---|
| | Vc Tuning Slope Kv [ppm/V] | Min APR [± ppm] at VDD[3] | | |
| | | 3.3V | 2.5V | 1.8V |
| A | 60 | 20 | -- | -- |
| B | 75 | 40 | 20 | -- |
| C | 105 | 70 | 40 | 20 |
| D | 150 | 115 | 75 | 45 |
| E | 180 | 145 | 100 | 65 |
| F | 225 | 190 | 135 | 85 |

| Code | Reel |
|---|---|
| R | Tape and Reel |
| <Blank> | Coil Tape |

| Frequency Code[2] | Description |
|---|---|
| xxxxxx | Two unique frequencies can be specified within the supported range of the selected signal format. Either frequency can be assigned to FS=0 or FS=1. A six digit numeric code will be assigned for the specific combination of frequencies. |

**Notes:**

1. Contact Silicon Labs for non-standard configurations.
2. Create custom part numbers at www.silabs.com/oscillators.
3. Min Absolute Pull Range (APR) includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
    a. For best jitter and phase noise performance, always choose the smallest Kv that meets the application's minimum APR requirements. Unlike SAW-based solutions which require higher Kv values to account for their higher temperature dependence, the Si56x series provides lower Kv options to minimize noise coupling and jitter in real-world PLL designs.
    b. APR is the ability of a VCXO to track a signal over the product lifetime. A VCXO with an APR of ±20 ppm is able to lock to a clock with a ±20 ppm stability over 20 years over all operating conditions.
    c. APR (±) = (0.5 x VDD x tuning slope) - (initial accuracy + temp stability + load pulling + VDD variation + aging).
    d. Minimum APR values noted above include absolute worst case values for all parameters.
    e. See application note, "AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR)" for more information.

## 1.1 Technical Support

| | |
|---|---|
| Frequently Asked Questions (FAQ) | www.silabs.com/Si566-FAQ |
| Oscillator Phase Noise Lookup Utility | www.silabs.com/oscillator-phase-noise-lookup |
| Quality and Reliability | www.silabs.com/quality |
| Development Kits | www.silabs.com/oscillator-tools |

## 2. Electrical Specifications

**Table 2.1. Electrical Specifications**

$V_{DD}$ = 1.8 V, 2.5 or 3.3 V ± 5%, $T_A$ = –40 to 85 ºC

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature Range | $T_A$ | | –40 | — | 85 | ºC |
| Frequency Range | $F_{CLK}$ | LVPECL, LVDS, CML | 0.2 | — | 3000 | MHz |
| | | HCSL | 0.2 | — | 400 | MHz |
| | | CMOS, Dual CMOS | 0.2 | — | 250 | MHz |
| Supply Voltage | $V_{DD}$ | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| Supply Current | $I_{DD}$ | LVPECL (output enabled) | — | 120 | 170 | mA |
| | | LVDS/CML (output enabled) | — | 100 | 167 | mA |
| | | HCSL (output enabled) | — | 95 | 140 | mA |
| | | CMOS (output enabled) | — | 95 | 145 | mA |
| | | Dual CMOS (output enabled) | — | 105 | 155 | mA |
| | | Tristate Hi-Z (output disabled) | — | 83 | — | mA |
| Temperature Stability[1] | | -40 to 85 °C | –20 | — | 20 | ppm |
| Rise/Fall Time (20% to 80% $V_{PP}$) | $T_R/T_F$ | LVPECL/LVDS/CML | — | — | 350 | ps |
| | | CMOS / Dual CMOS ($C_L$ = 5 pF) | — | 0.5 | 1.5 | ns |
| | | HCSL, $F_{CLK}$ >50 MHz | — | — | 550 | ps |
| Duty Cycle | $D_C$ | All formats | 45 | — | 55 | % |
| Frequency Select (FS)[2] | $V_{IH}$ | | 0.7 × $V_{DD}$ | — | — | V |
| | $V_{IL}$ | | — | — | 0.3 × $V_{DD}$ | V |
| | $T_{FS}$ | Settling Time after FS Change | — | — | 10 | ms |
| Powerup Time | $t_{OSC}$ | Time from 0.9 × $V_{DD}$ until output frequency ($F_{CLK}$) within spec | — | — | 10 | ms |
| LVPECL Output Option[3] | $V_{OC}$ | Mid-level | $V_{DD}$ – 1.42 | — | $V_{DD}$ – 1.25 | V |
| | $V_O$ | Swing (diff, $F_{CLK} \leq$ 1.5 GHz) | 1.1 | — | 1.9 | $V_{PP}$ |
| | | Swing (diff, $F_{CLK}$ > 1.5 GHz)[6] | 0.55 | — | 1.7 | $V_{PP}$ |
| LVDS Output Option[4] | $V_{OC}$ | Mid-level (2.5 V, 3.3 V VDD) | 1.125 | 1.20 | 1.275 | V |
| | | Mid-level (1.8 V VDD) | 0.8 | 0.9 | 1.0 | V |
| | $V_O$ | Swing (diff, $F_{CLK} \leq$ 1.5 GHz) | 0.5 | 0.7 | 0.9 | $V_{PP}$ |
| | | Swing (diff, $F_{CLK}$ > 1.5 GHz) [6] | 0.25 | 0.5 | 0.8 | $V_{PP}$ |

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| HCSL Output Option[5] | $V_{OH}$ | Output voltage high | 660 | 800 | 850 | mV |
| | $V_{OL}$ | Output voltage low | –150 | 0 | 150 | mV |
| | $V_C$ | Crossing voltage | 250 | 410 | 550 | mV |
| CML Output Option (AC-Coupled) | $V_O$ | Swing (diff, $F_{CLK} \leq$ 1.5 GHz) | 0.6 | 0.8 | 1.0 | $V_{PP}$ |
| | | Swing (diff, $F_{CLK}$ > 1.5 GHz)[6] | 0.3 | 0.55 | 0.9 | $V_{PP}$ |
| CMOS Output Option | $V_{OH}$ | $I_{OH}$ = 8/6/4 mA for 3.3/2.5/1.8 V VDD | 0.85 × $V_{DD}$ | — | — | V |
| | $V_{OL}$ | $I_{OL}$ = 8/6/4 mA for 3.3/2.5/1.8 V VDD | — | — | 0.15 × $V_{DD}$ | V |

**Notes:**

1. Min APR includes temperature stability, initial accuracy, load pulling, VDD variation, and aging for 20 yrs at 70 ºC.
2. FS pin includes a 50 kΩ pull-up to VDD.
3. $R_{term}$ = 50 Ω to $V_{DD}$ – 2.0 V (see Figure 4.1).
4. $R_{term}$ = 100 Ω (differential) (see Figure 4.2).
5. $R_{term}$ = 50 Ω to GND (see Figure 4.2).
6. Refer to the figure below for Typical Clock Output Swing Amplitudes vs Frequency.

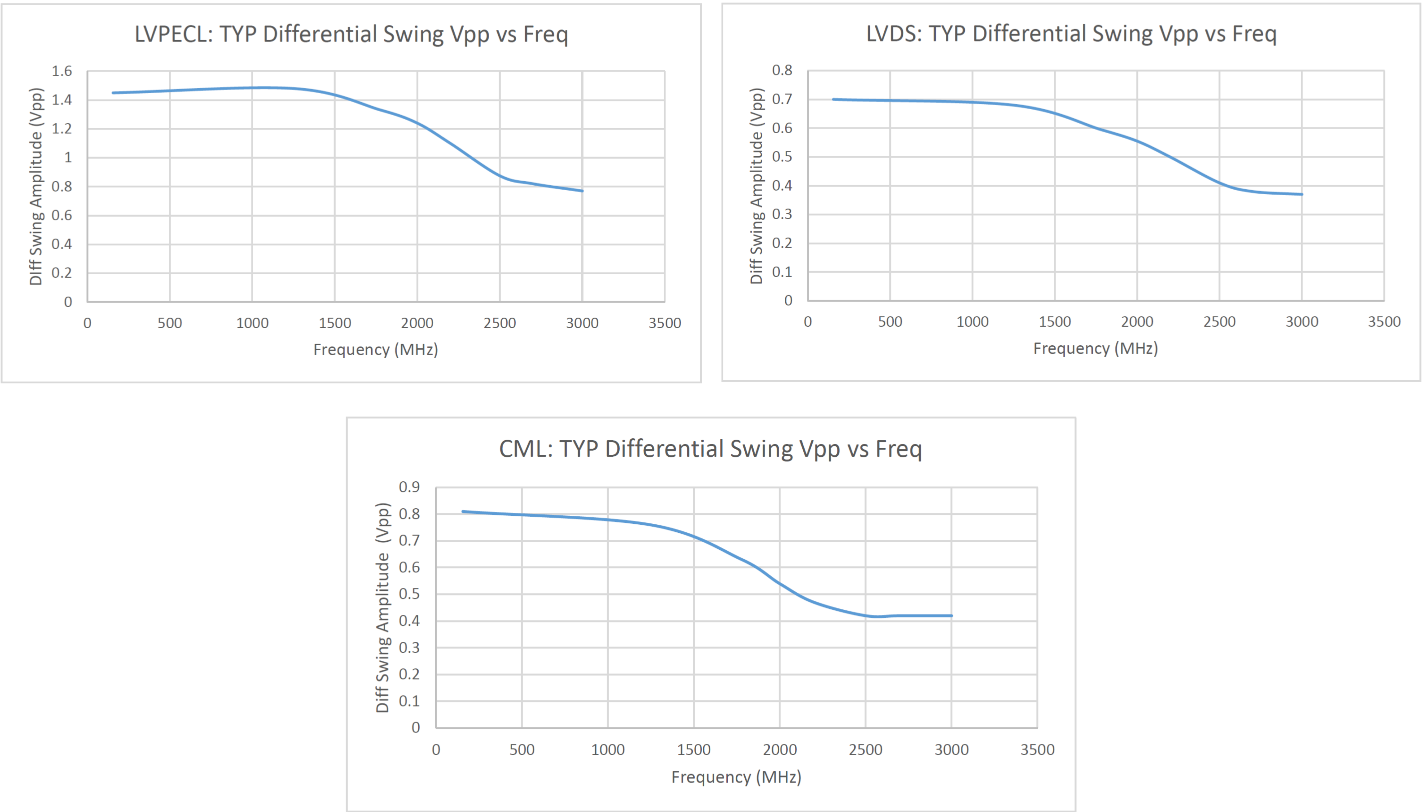



**Figure 2.1. Typical Clock Output Swing Amplitudes vs. Frequency**

**Table 2.2. $V_C$ Control Voltage Input**

$V_{DD}$ = 1.8, 2.5 or 3.3 V ± 5%, $T_A$ = –40 to 85 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Control Voltage Range | $V_C$ | | 0.1 x VDD | VDD/2 | 0.9 x VDD | V |
| Control Voltage Tuning Slope (Vc = 10% VDD to 90% VDD) | Kv | Positive slope, ordering option | 60, 75, 105, 150, 180, 225 | | | ppm/V |
| Kv Variation | Kv_var | | — | — | ±10 | % |
| Control Voltage Linearity | LVC | Best Straight Line fit | –1.5 | ±0.5 | +1.5 | % |
| Modulation Bandwidth | BW | | — | 10 | — | kHz |
| Vc Input Impedance | ZVC | | 500 | — | — | kΩ |

**Table 2.3. Clock Output Phase Jitter and PSRR**

$V_{DD}$ = 1.8 V, 2.5 or 3.3 V ± 5%, $T_A$ = –40 to 85 °C

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Phase Jitter (RMS, 12 kHz - 20 MHz)[1] All Differential Formats, $F_{CLK}$ ≥ 200 MHz | ϕJ | Kv = 60 ppm/V | — | 100 | 150 | fs |
| | | Kv = 75 ppm/V | — | 103 | — | fs |
| | | Kv = 105 ppm/V | — | 110 | — | fs |
| | | Kv = 150 ppm/V | — | 123 | — | fs |
| | | Kv = 180 ppm/V | — | 132 | — | fs |
| | | Kv = 225 ppm/V | — | 150 | — | fs |
| Phase Jitter (RMS, 12 kHz - 20 MHz)[1] All Diff Formats, 100 MHz ≤ $F_{CLK}$ < 200 MHz | ϕJ | Kv = 60 ppm/V | — | 115 | 170 | fs |
| | | Kv = 75 ppm/V | — | 118 | — | fs |
| | | Kv = 105 ppm/V | — | 125 | — | fs |
| | | Kv = 150 ppm/V | — | 138 | — | fs |
| | | Kv = 180 ppm/V | — | 147 | — | fs |
| | | Kv = 225 ppm/V | — | 165 | — | fs |
| Phase Jitter (RMS, 12 kHz - 20 MHz)[1] LVDS, $F_{CLK}$ = 156.25 MHz | ϕJ | Kv = 60 ppm/V | — | 110 | 130 | fs |
| | | Kv = 75 ppm/V | — | 113 | — | fs |
| | | Kv = 105 ppm/V | — | 120 | — | fs |
| | | Kv = 150 ppm/V | — | 133 | — | fs |
| | | Kv = 180 ppm/V | — | 142 | — | fs |
| | | Kv = 225 ppm/V | — | 160 | — | fs |
| Phase Jitter (RMS, 12 kHz - 20 MHz)[1] CMOS / Dual CMOS Formats | ϕJ | 10 MHz ≤ $F_{CLK}$ < 250 MHz | — | 200 | — | fs |

| Parameter | Symbol | Test Condition/Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output | PSRR | 100 kHz sine wave | | -83 | | dBc |
| | | 200 kHz sine wave | | -83 | | |
| | | 500 kHz sine wave | | -82 | | |
| | | 1 MHz sine wave | | -85 | | |

**Note:**

1. Jitter inclusive of any spurs.

**Table 2.4. 3.2 x 5 mm Clock Output Phase Noise (Typical)**

| Offset Frequency (f) | 156.25 MHz LVDS | 200 MHz LVDS | 644.53125 MHz LVDS | Unit |
|---|---|---|---|---|
| 100 Hz | –73 | –71 | –60 | dBc/Hz |
| 1 kHz | –102 | –102 | –93 | |
| 10 kHz | –130 | –128 | –118 | |
| 100 kHz | –141 | –139 | –129 | |
| 1 MHz | –150 | –148 | –138 | |
| 10 MHz | –159 | –160 | –153 | |
| 20 MHz | –160 | –162 | –154 | |
| **Offset Frequency (f)** | **156.25 MHz LVPECL** | **200 MHz LVPECL** | **644.53125 MHz LVPECL** | **Unit** |
| 100 Hz | –72 | –71 | –60 | dBc/Hz |
| 1 kHz | –103 | –101 | –92 | |
| 10 kHz | –130 | –127 | –117 | |
| 100 kHz | –142 | –139 | –129 | |
| 1 MHz | –150 | –148 | –138 | |
| 10 MHz | –160 | –162 | –154 | |
| 20 MHz | –161 | –162 | –156 | |

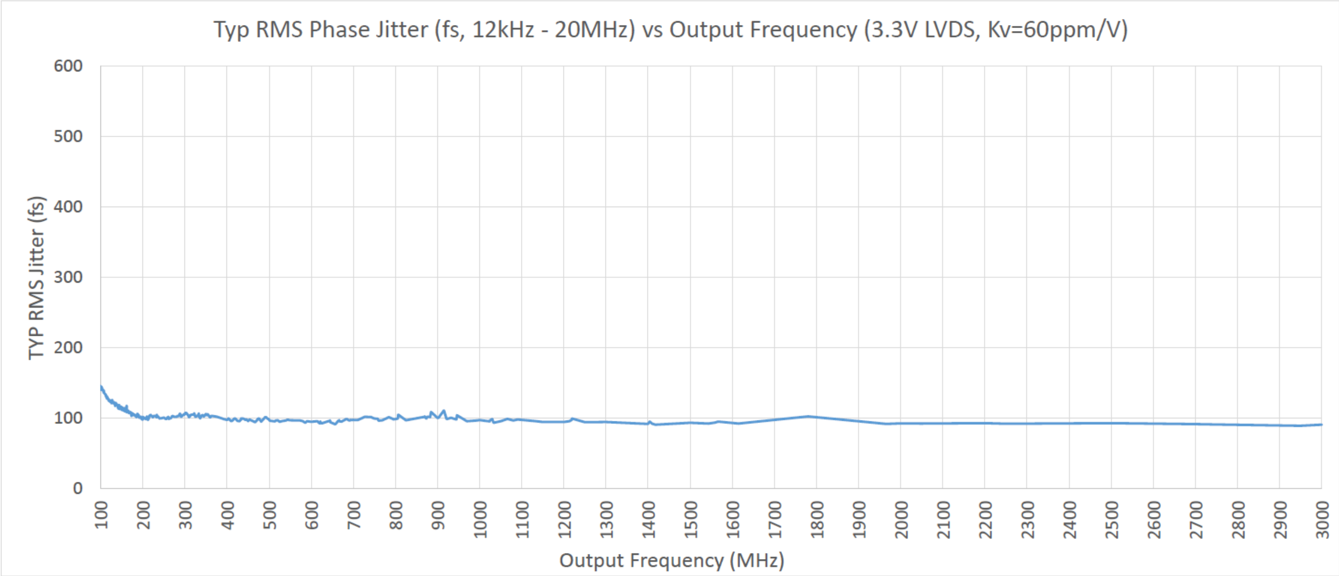



**Figure 2.2. Phase Jitter vs. Output Frequency**

Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at www.silabs.com/oscillators.

**Table 2.5. Environmental Compliance and Package Information**

| Parameter | Test Condition |
|---|---|
| Mechanical Shock | MIL-STD-883, Method 2002 |
| Mechanical Vibration | MIL-STD-883, Method 2007 |
| Solderability | MIL-STD-883, Method 2003 |
| Gross and Fine Leak | MIL-STD-883, Method 1014 |
| Resistance to Solder Heat | MIL-STD-883, Method 2036 |
| Moisture Sensitivity Level (MSL) | 1 |
| Contact Pads | Gold over Nickel |

**Note:**

1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: www.silabs.com/support/quality/Pages/RoHSInformation.aspx.

**Table 2.6. Thermal Conditions**

| Package | Parameter | Symbol | Test Condition | Value | Unit |
|---|---|---|---|---|---|
| 3.2 × 5 mm 6-pin CLCC | Thermal Resistance Junction to Ambient | $\Theta_{JA}$ | Still Air, 85 °C | 80.3 | ºC/W |
| | Thermal Resistance Junction to Board | $\Theta_{JB}$ | Still Air, 85 °C | 50.8 | ºC/W |
| | Max Junction Temperature | $T_J$ | Still Air, 85 °C | 125 | ºC |
| 5 × 7 mm 6-pin CLCC | Thermal Resistance Junction to Ambient | $\Theta_{JA}$ | Still Air, 85 °C | 68.4 | ºC/W |
| | Thermal Resistance Junction to Board | $\Theta_{JB}$ | Still Air, 85 °C | 52.9 | ºC/W |
| | Max Junction Temperature | $T_J$ | Still Air, 85 °C | 125 | ºC |

**Table 2.7. Absolute Maximum Ratings[1]**

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Maximum Operating Temp. | $T_{AMAX}$ | 95 | ºC |
| Storage Temperature | $T_S$ | –55 to 125 | ºC |
| Supply Voltage | $V_{DD}$ | –0.5 to 3.8 | ºC |
| Input Voltage | $V_{IN}$ | –0.5 to $V_{DD}$ + 0.3 | V |
| ESD HBM (JESD22-A114) | HBM | 2.0 | kV |
| Solder Temperature[2] | $T_{PEAK}$ | 260 | ºC |
| Solder Time at $T_{PEAK}$[2] | $T_P$ | 20–40 | sec |

**Notes:**

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

## 3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple VCXOs with a single Si566 device.

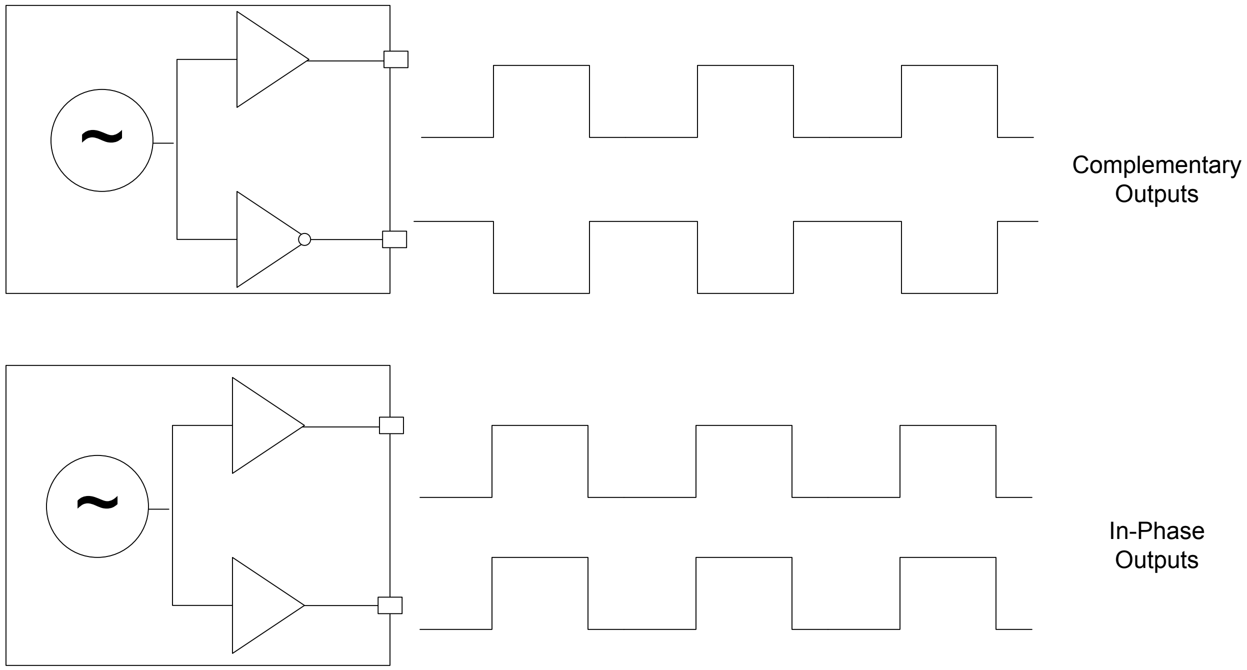



**Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs**

## 4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.

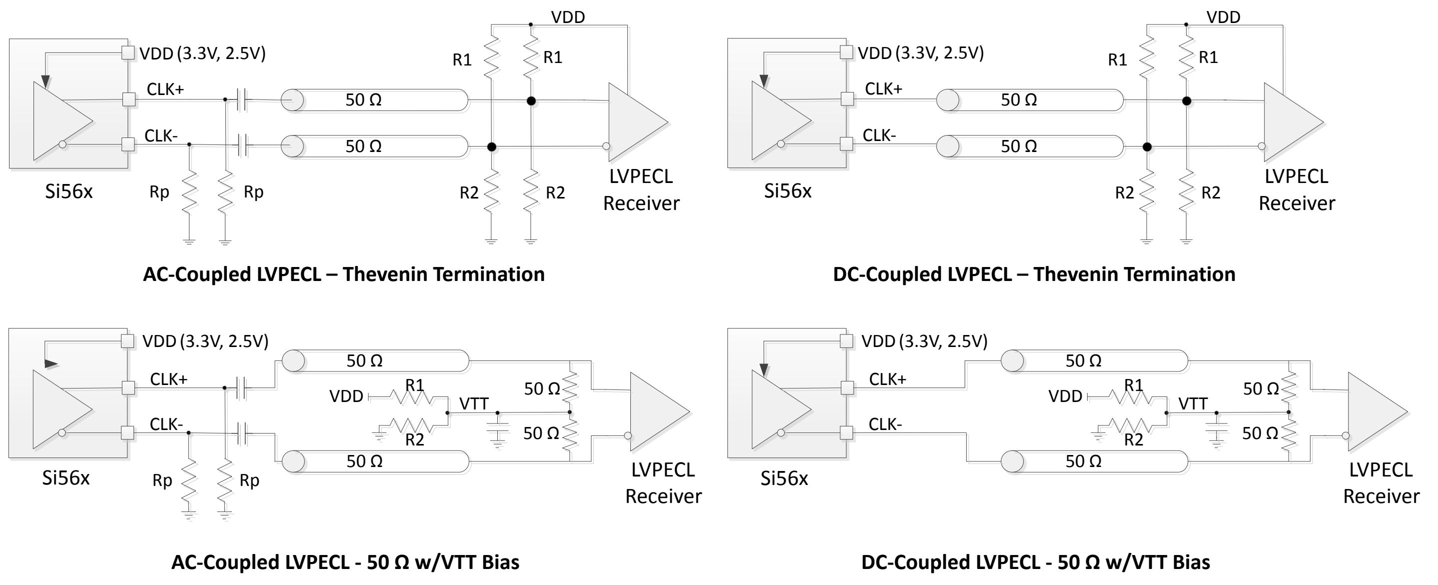



**Figure 4.1. LVPECL Output Terminations**

| AC-Coupled LVPECL Termination Resistor Values | | | |
|---|---|---|---|
| **VDD** | R1 | R2 | Rp |
| **3.3 V** | 127 Ω | 82.5 Ω | 130 Ω |
| **2.5 V** | 250 Ω | 62.5 Ω | 90 Ω |

| DC-Coupled LVPECL Termination Resistor Values | | |
|---|---|---|
| **VDD** | R1 | R2 |
| **3.3 V** | 127 Ω | 82.5 Ω |
| **2.5 V** | 250 Ω | 62.5 Ω |

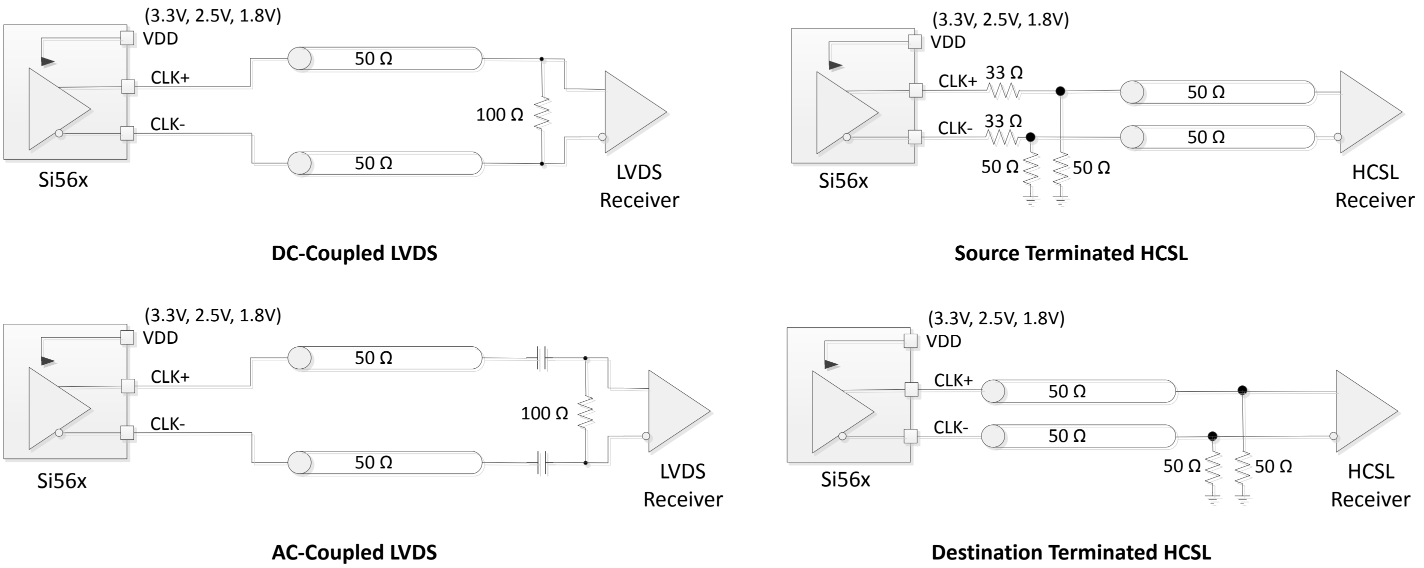



**Figure 4.2. LVDS and HCSL Output Terminations**

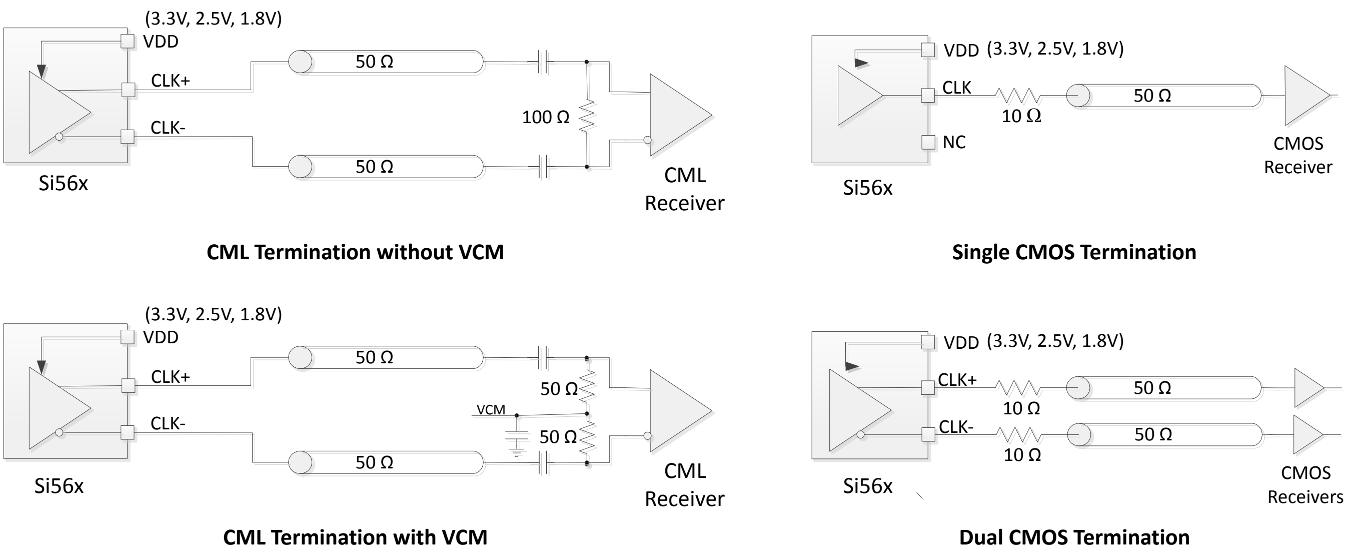



**Figure 4.3. CML and CMOS Output Terminations**

# 5. Package Outline

## 5.1 Package Outline (5×7 mm)

The figure below illustrates the package details for the 5×7 mm Si566. The table below lists the values for the dimensions shown in the illustration.

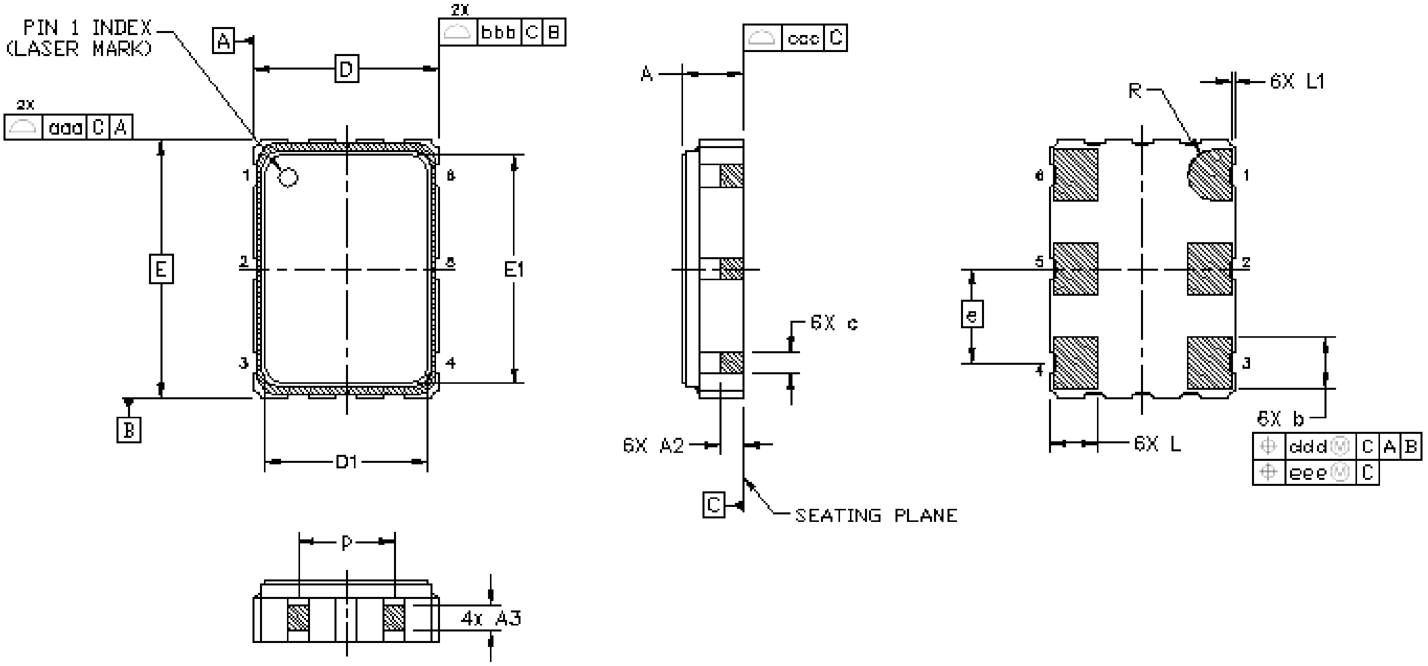



Figure 5.1. Si566 (5×7 mm) Outline Diagram

Table 5.1. Package Diagram Dimensions (mm)

| Dimension | Min | Nom | Max | | Dimension | Min | Nom | Max |
|---|---|---|---|---|---|---|---|---|
| A | 1.13 | 1.28 | 1.43 | | L | 1.17 | 1.27 | 1.37 |
| A2 | 0.50 | 0.55 | 0.60 | | L1 | 0.05 | 0.10 | 0.15 |
| A3 | 0.50 | 0.55 | 0.60 | | p | 1.70 | — | 1.90 |
| b | 1.30 | 1.40 | 1.50 | | R | 0.70 REF | | |
| c | 0.50 | 0.60 | 0.70 | | aaa | 0.15 | | |
| D | 5.00 BSC | | | | bbb | 0.15 | | |
| D1 | 4.30 | 4.40 | 4.50 | | ccc | 0.08 | | |
| e | 2.54 BSC | | | | ddd | 0.10 | | |
| E | 7.00 BSC | | | | eee | 0.05 | | |
| E1 | 6.10 | 6.20 | 6.30 | | | | | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 5.2 Package Outline (3.2×5 mm)

The figure below illustrates the package details for the 3.2×5 mm Si566. The table below lists the values for the dimensions shown in the illustration.

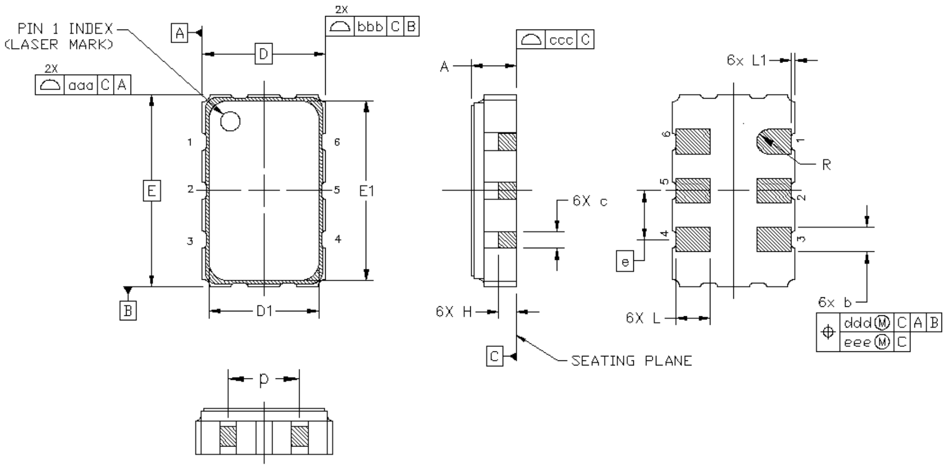



**Figure 5.2. Si566 (3.2×5 mm) Outline Diagram**

**Table 5.2. Package Diagram Dimensions (mm)**

| Dimension | Min | Nom | Max |
|---|---|---|---|
| A | 1.06 | 1.17 | 1.33 |
| b | 0.54 | 0.64 | 0.74 |
| c | 0.35 | 0.45 | 0.55 |
| D | | 3.20 BSC | |
| D1 | 2.55 | 2.60 | 2.65 |
| e | | 1.27 BSC | |
| E | | 5.00 BSC | |
| E1 | 4.35 | 4.40 | 4.45 |
| H | 0.45 | 0.55 | 0.65 |
| L | 0.80 | 0.90 | 1.00 |
| L1 | 0.05 | 0.10 | 0.15 |
| p | 1.36 | 1.46 | 1.56 |
| R | | 0.32 REF | |
| aaa | | 0.15 | |
| bbb | | 0.15 | |
| ccc | | 0.08 | |
| ddd | | 0.10 | |
| eee | | 0.05 | |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

# 6. PCB Land Pattern

## 6.1 PCB Land Pattern (5×7 mm)

The figure below illustrates the 5×7 mm PCB land pattern for the Si566. The table below lists the values for the dimensions shown in the illustration.

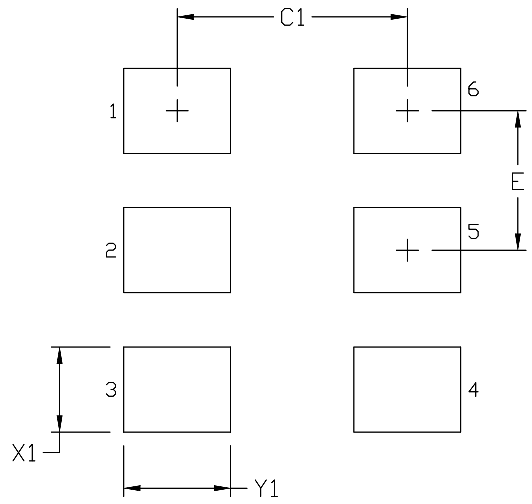



**Figure 6.1. Si566 (5×7 mm) PCB Land Pattern**

**Table 6.1. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) |
|---|---|
| C1 | 4.20 |
| E | 2.54 |
| X1 | 1.55 |
| Y1 | 1.95 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

### 6.2 PCB Land Pattern (3.2×5 mm)

The figure below illustrates the 3.2×5.0 mm PCB land pattern for the Si566. The table below lists the values for the dimensions shown in the illustration.

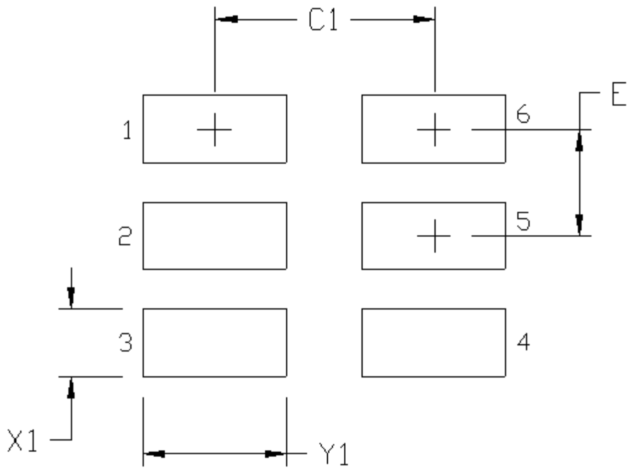



**Figure 6.2. Si566 (3.2×5 mm) PCB Land Pattern**

**Table 6.2. PCB Land Pattern Dimensions (mm)**

| Dimension | (mm) |
|---|---|
| C1 | 2.60 |
| E | 1.27 |
| X1 | 0.80 |
| Y1 | 1.70 |

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 7. Top Marking

The figure below illustrates the mark specification for the Si566. The table below lists the line information.

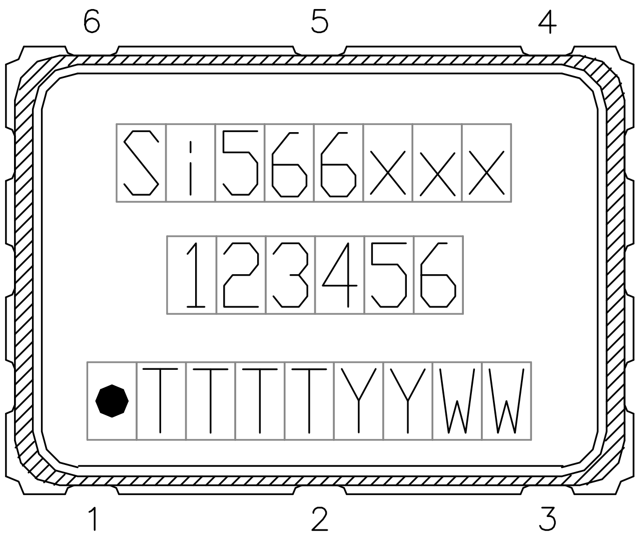



**Figure 7.1. Mark Specification**

**Table 7.1. Si566 Top Mark Description**

| Line | Position | Description |
|---|---|---|
| 1 | 1–8 | "Si566", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si566AAA) |
| 2 | 1–6 | Frequency Code<br>(6-digit custom code as described in the Ordering Guide) |
| 3 | **Trace Code** | |
| | Position 1 | Pin 1 orientation mark (dot) |
| | Position 2 | Product Revision (B) |
| | Position 3–5 | Tiny Trace Code (3 alphanumeric characters per assembly release instructions) |
| | Position 6–7 | Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17) |
| | Position 8–9 | Calendar Work Week number (1–53), to be assigned by assembly site |

# 8. Revision History

**Revision 1.0**

June, 2018

- Initial draft

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