Ultra Series™ 晶体振荡器系列 (VCXO) Si567 数据表

超低抖动任意四频 VCXO (100 fs)，0.2 至 3000 MHz

Si567 Ultra Series™ 电压控制晶体振荡器系列采用 Silicon Laboratories 先进的第四代 DSPLL® 技术，提供可选双频的超低抖动和低相位噪声时钟。这款设备经过出厂前预编程，可提供频率范围在 0.2 至 3000 MHz 之间的任意可选四频，分辨率小于 <1 ppb，可以在整个工作范围内实现整数和小数频率的超低抖动。片上电源滤波可以实现行业领先的电源噪音抑制特性，简化了使用开关式电源的噪声系统生成低抖动时钟的任务。Si567 振荡器系列采用行业标准 3.2×5 mm 和 5×7 mm 封装，大幅简化供应链，使 Silicon Labs 在收到订单后 1-2 周内即可将定制频率样品送达。不同于传统的 XO，Si567 振荡器系列无需使用不同的晶体实现不同的输出频率，而使用单一晶体和基于 DSPLL IC 的方法提供所需输出频率。Si567 振荡器系列经工厂配置，可以满足各种各样的用户规格，包括频率、输出格式和 OE 引脚位置/极性。特殊配置在发货时经过出厂前编程，消除了与定制频率振荡器有关的长交付周期。

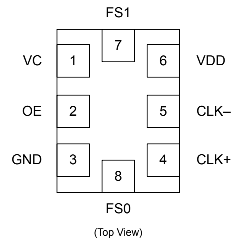
主要特点

- 可以选择 200 kHz 至 3000 MHz 之间的任意可选四频
- 超低抖动：100 fs RMS 典型值（12 kHz － 20 MHz）
- 出色的 PSRR 和电源噪声抗扰度：－80 dBc（典型值）
- 相同部件编号可实现 3.3 V、2.5 V 和 1.8 V 的供电电压电源操作
- 提供 LVPECL、LVDS、CML、HCSL、CMOS 和双路 CMOS 输出选项
- 3.2×5、5×7 mm 封装尺寸
- 样品交付周期为 1-2 周

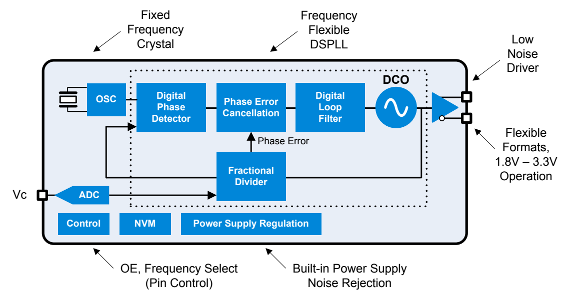
应用

- 100G/200G/400G 相干光学 OTN
- 10G/25G/40G/100G 以太网
- 56G/112G PAM4 时钟
- 3G-SDI/12G-SDI/24G-SDI 广播视频
- 服务器、开关、存储、网卡、搜索加速
- 测试和测量
- FPGA/ASIC 时钟设计

引脚分配



引脚编号	说明
1	VC = 电压控制销
2	OE = 输出使能
3	GND 表示“接地”
4	CLK+ 表示“时钟输出”
5	CLK- 表示“互补时钟输出”。CMOS 输出格式下不可用。
6	VDD 表示“电源电压”
7	FS1 表示“频率选择 1”
8	FS0 表示“频率选择 0”



1. Ordering Guide

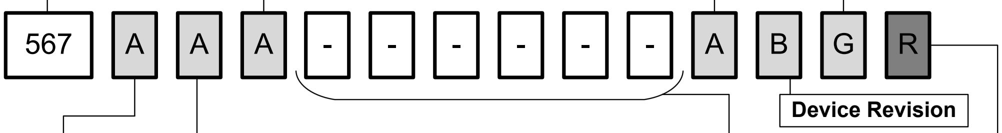
The Si567 VCXO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to www.silabs.com/oscillators to access this tool and for further ordering instructions.

VCXO Series	Description
567	Quad Frequency VCXO

Code	OE Pin	OE Polarity
A	Pin 2	Active High
B	Pin 2	Active Low

	Package
A	5x7 mm
B	3.2x5 mm

	Temperature Grade
G	-40 to 85 °C



Code	Reel
R	Tape and Reel
<Blank>	Coil Tape

Signal Format	VDD Range	Order Option
LVPECL	2.5, 3.3 V	A
LVDS	1.8, 2.5, 3.3 V	B
CMOS	1.8, 2.5, 3.3 V	C
CML	1.8, 2.5, 3.3 V	D
HCSL	1.8, 2.5, 3.3 V	E
Dual CMOS (In-Phase)	1.8, 2.5, 3.3 V	F
Dual CMOS (Complementary)	1.8, 2.5, 3.3 V	G
Custom[1]	1.8, 2.5, 3.3 V	X

	Temperature Stability = ± 20 ppm			
	Vc Tuning Slope Kv [ppm/V]	Min APR [± ppm] at VDD[3]		
		3.3V	2.5V	1.8V
A	60	20	--	--
B	75	40	20	--
C	105	70	40	20
D	150	115	75	45
E	180	145	100	65
F	225	190	135	85

Frequency Code[2]	Description
xxxxxx	Four unique frequencies can be specified within the supported range of the selected signal format. The frequencies can be arranged in any order from FS[1:0]=00 to FS[1:0]=11. A six digit numeric code will be assigned for the specific combination of frequencies.

Notes:

1. Contact Silicon Labs for non-standard configurations.
2. Create custom part numbers at www.silabs.com/oscillators.
3. Min Absolute Pull Range (APR) includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
    a. For best jitter and phase noise performance, always choose the smallest Kv that meets the application's minimum APR requirements. Unlike SAW-based solutions which require higher Kv values to account for their higher temperature dependence, the Si56x series provides lower Kv options to minimize noise coupling and jitter in real-world PLL designs.
    b. APR is the ability of a VCXO to track a signal over the product lifetime. A VCXO with an APR of ±20 ppm is able to lock to a clock with a ±20 ppm stability over 20 years over all operating conditions.
    c. APR (±) = (0.5 x VDD x tuning slope) - (initial accuracy + temp stability + load pulling + VDD variation + aging).
    d. Minimum APR values noted above include absolute worst case values for all parameters.
    e. See application note, "AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR)" for more information.

1.1 Technical Support

Frequently Asked Questions (FAQ)	www.silabs.com/Si567-FAQ
Oscillator Phase Noise Lookup Utility	www.silabs.com/oscillator-phase-noise-lookup
Quality and Reliability	www.silabs.com/quality
Development Kits	www.silabs.com/oscillator-tools

2. Electrical Specifications

Table 2.1. Electrical Specifications

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 ºC

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	T_A		–40	—	85	ºC
Frequency Range	F_{CLK}	LVPECL, LVDS, CML	0.2	—	3000	MHz
		HCSL	0.2	—	400	MHz
		CMOS, Dual CMOS	0.2	—	250	MHz
Supply Voltage	V_{DD}	3.3 V	3.135	3.3	3.465	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
Supply Current	I_{DD}	LVPECL (output enabled)	—	120	170	mA
		LVDS/CML (output enabled)	—	100	167	mA
		HCSL (output enabled)	—	95	140	mA
		CMOS (output enabled)	—	95	145	mA
		Dual CMOS (output enabled)	—	105	155	mA
		Tristate Hi-Z (output disabled)	—	83	—	mA
Temperature Stability[1]		-40 to 85 °C	–20	—	20	ppm
Rise/Fall Time (20% to 80% V_{PP})	T_R/T_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS / Dual CMOS (C_L = 5 pF)	—	0.5	1.5	ns
		HCSL, F_{CLK} >50 MHz	—	—	550	ps
Duty Cycle	D_C	All formats	45	—	55	%
Output Enable (OE) Frequency Select (FS0, FS1)[2]	V_{IH}		0.7 × V_{DD}	—	—	V
	V_{IL}		—	—	0.3 × V_{DD}	V
	T_D	Output Disable Time, F_{CLK} > 10 MHz	—	—	3	µs
	T_E	Output Enable Time, F_{CLK} > 10 MHz	—	—	20	µs
	T_{FS}	Settling Time after FS Change	—	—	10	ms
Powerup Time	t_{OSC}	Time from 0.9 × V_{DD} until output frequency (F_{CLK}) within spec	—	—	10	ms
LVPECL Output Option[3]	V_{OC}	Mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_O	Swing (diff, $F_{CLK} \leq$ 1.5 GHz)	1.1	—	1.9	V_{PP}
		Swing (diff, F_{CLK} > 1.5 GHz)[6]	0.55	—	1.7	V_{PP}

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
LVDS Output Option[4]	V_{OC}	Mid-level (2.5 V, 3.3 V VDD)	1.125	1.20	1.275	V
		Mid-level (1.8 V VDD)	0.8	0.9	1.0	V
	V_O	Swing (diff, $F_{CLK} \leq 1.5$ GHz)	0.5	0.7	0.9	V_{PP}
		Swing (diff, $F_{CLK} > 1.5$ GHz) [6]	0.25	0.5	0.8	V_{PP}
HCSL Output Option[5]	V_{OH}	Output voltage high	660	800	850	mV
	V_{OL}	Output voltage low	–150	0	150	mV
	V_C	Crossing voltage	250	410	550	mV
CML Output Option (AC-Coupled)	V_O	Swing (diff, $F_{CLK} \leq 1.5$ GHz)[6]	0.6	0.8	1.0	V_{PP}
		Swing (diff, $F_{CLK} > 1.5$ GHz)[6]	0.3	0.55	0.9	V_{PP}
CMOS Output Option	V_{OH}	I_{OH} = 8/6/4 mA for 3.3/2.5/1.8 V VDD	0.85 × V_{DD}	—	—	V
	V_{OL}	I_{OL} = 8/6/4 mA for 3.3/2.5/1.8 V VDD	—	—	0.15 × V_{DD}	V

Notes:

1. Min APR includes temperature stability, initial accuracy, load pulling, VDD variation, and aging for 20 yrs at 70 ºC.
2. OE includes a 50 kΩ pull-up to VDD for OE active high, or includes a 50 kΩ pull-down to GND for OE active low. FS0 and FS1 pins each include a 50 kΩ pull-up to VDD.
3. R_{term} = 50 Ω to V_{DD} – 2.0 V (see Figure 4.1).
4. R_{term} = 100 Ω (differential) (see Figure 4.2).
5. R_{term} = 50 Ω to GND (see Figure 4.2).
6. Refer to the figure below for Typical Clock Output Swing Amplitudes vs Frequency.

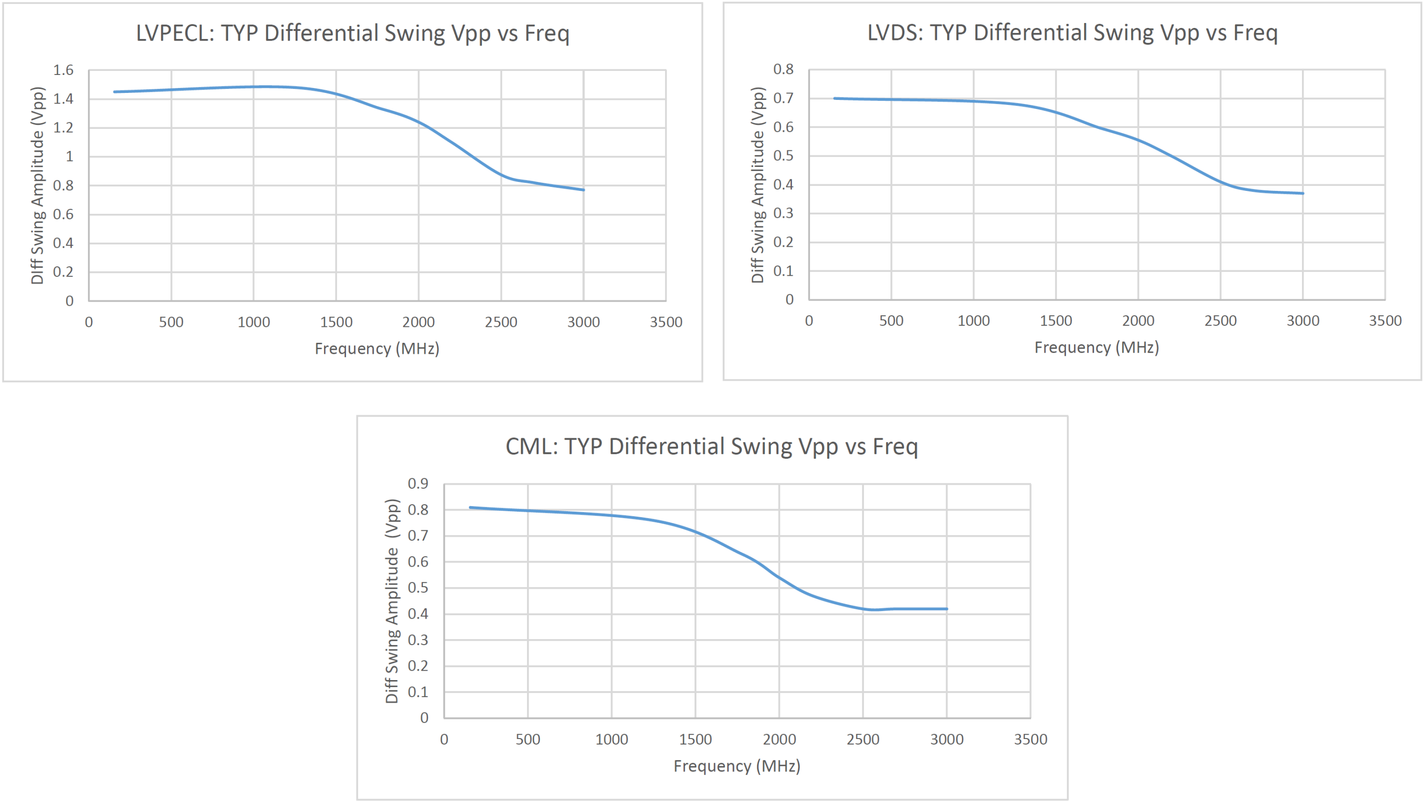


Figure 2.1. Typical Clock Output Swing Amplitudes vs. Frequency

Table 2.2. V_C Control Voltage Input

V_{DD} = 1.8, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 ºC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Control Voltage Range	V_C		0.1 x VDD	VDD/2	0.9 x VDD	V
Control Voltage Tuning Slope (Vc = 10% VDD to 90% VDD)	Kv	Positive slope, ordering option	60, 75, 105, 150, 180, 225			ppm/V
Kv Variation	Kv_var		—	—	±10	%
Control Voltage Linearity	LVC	Best Straight Line fit	–1.5	±0.5	+1.5	%
Modulation Bandwidth	BW		—	10	—	kHz
Vc Input Impedance	ZVC		500	—	—	kΩ

Table 2.3. Clock Output Phase Jitter and PSRR

V_{DD} = 1.8 V, 2.5 or 3.3 V ± 5%, T_A = –40 to 85 ºC

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Phase Jitter (RMS, 12 kHz - 20 MHz)[1] All Differential Formats, F_{CLK} ≥ 200 MHz	ϕJ	Kv = 60 ppm/V	—	100	150	fs
		Kv = 75 ppm/V	—	103	—	fs
		Kv = 105 ppm/V	—	110	—	fs
		Kv = 150 ppm/V	—	123	—	fs
		Kv = 180 ppm/V	—	132	—	fs
		Kv = 225 ppm/V	—	150	—	fs
Phase Jitter (RMS, 12 kHz - 20 MHz) [1] All Diff Formats, 100 MHz ≤ F_{CLK} < 200 MHz	ϕJ	Kv = 60 ppm/V	—	115	170	fs
		Kv = 75 ppm/V	—	118	—	fs
		Kv = 105 ppm/V	—	125	—	fs
		Kv = 150 ppm/V	—	138	—	fs
		Kv = 180 ppm/V	—	147	—	fs
		Kv = 225 ppm/V	—	165	—	fs
Phase Jitter (RMS, 12 kHz - 20 MHz)[1] LVDS, F_{CLK} = 156.25 MHz	ϕJ	Kv = 60 ppm/V	—	110	130	fs
		Kv = 75 ppm/V	—	113	—	fs
		Kv = 105 ppm/V	—	120	—	fs
		Kv = 150 ppm/V	—	133	—	fs
		Kv = 180 ppm/V	—	142	—	fs
		Kv = 225 ppm/V	—	160	—	fs
Phase Jitter (RMS, 12 kHz - 20 MHz)[1] CMOS / Dual CMOS Formats	ϕJ	10 MHz ≤ F_{CLK} < 250 MHz	—	200	—	fs

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output	PSRR	100 kHz sine wave		-83		dBc
		200 kHz sine wave		-83		
		500 kHz sine wave		-82		
		1 MHz sine wave		-85		

Note:

1. Jitter inclusive of any spurs.

Table 2.4. 3.2 x 5 mm Clock Output Phase Noise (Typical)

Offset Frequency (f)	156.25 MHz LVDS	200 MHz LVDS	644.53125 MHz LVDS	Unit
100 Hz	–73	–71	–60	dBc/Hz
1 kHz	–102	–102	–93	
10 kHz	–130	–128	–118	
100 kHz	–141	–139	–129	
1 MHz	–150	–148	–138	
10 MHz	–159	–160	–153	
20 MHz	–160	–162	–154	
Offset Frequency (f)	**156.25 MHz LVPECL**	**200 MHz LVPECL**	**644.53125 MHz LVPECL**	**Unit**
100 Hz	–72	–71	–60	dBc/Hz
1 kHz	–103	–101	–92	
10 kHz	–130	–127	–117	
100 kHz	–142	–139	–129	
1 MHz	–150	–148	–138	
10 MHz	–160	–162	–154	
20 MHz	–161	–162	–156	

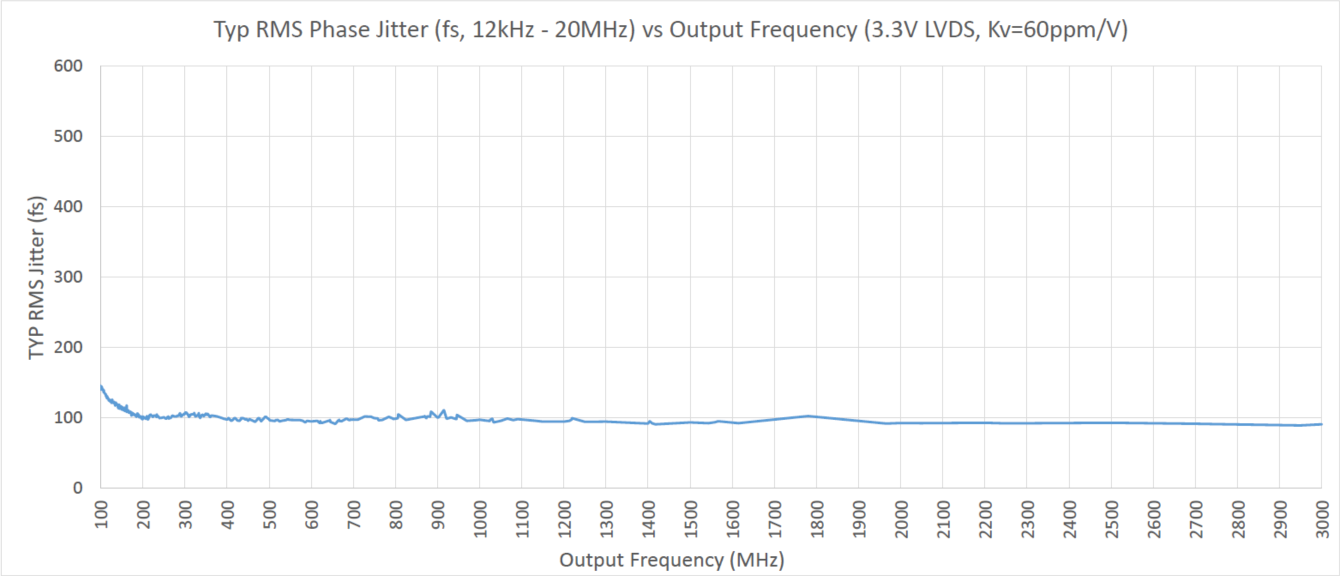


Figure 2.2. Phase Jitter vs. Output Frequency

Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at www.silabs.com/oscillators.

Table 2.5. Environmental Compliance and Package Information

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level (MSL)	1
Contact Pads	Gold over Nickel

Note:

1. For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: www.silabs.com/support/quality/Pages/RoHSInformation.aspx.

Table 2.6. Thermal Conditions

Package	Parameter	Symbol	Test Condition	Value	Unit
3.2×5 mm 8-pin CLCC	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air, 85 °C	79.1	ºC/W
	Thermal Resistance Junction to Board	Θ_{JB}	Still Air, 85 °C	49.6	ºC/W
	Max Junction Temperature	T_J	Still Air, 85 °C	125	ºC
5×7 mm 8-pin CLCC	Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air, 85 °C	67.1	ºC/W
	Thermal Resistance Junction to Board	Θ_{JB}	Still Air, 85 °C	51.7	ºC/W
	Max Junction Temperature	T_J	Still Air, 85 °C	125	ºC

Table 2.7. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Unit
Maximum Operating Temp.	T_{AMAX}	95	ºC
Storage Temperature	T_S	–55 to 125	ºC
Supply Voltage	V_{DD}	–0.5 to 3.8	ºC
Input Voltage	V_{IN}	–0.5 to V_{DD} + 0.3	V
ESD HBM (JESD22-A114)	HBM	2.0	kV
Solder Temperature[2]	T_{PEAK}	260	ºC
Solder Time at T_{PEAK}[2]	T_P	20–40	sec

Notes:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020.

3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple VCXOs with a single Si567 device.

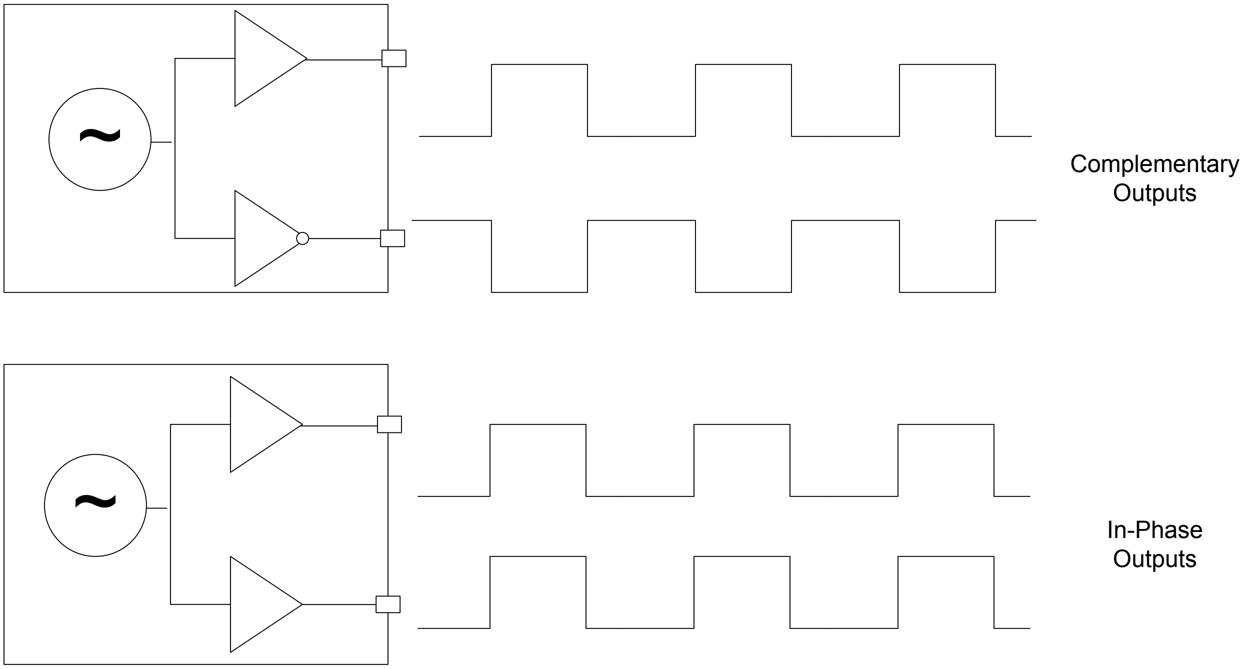


Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs

4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.

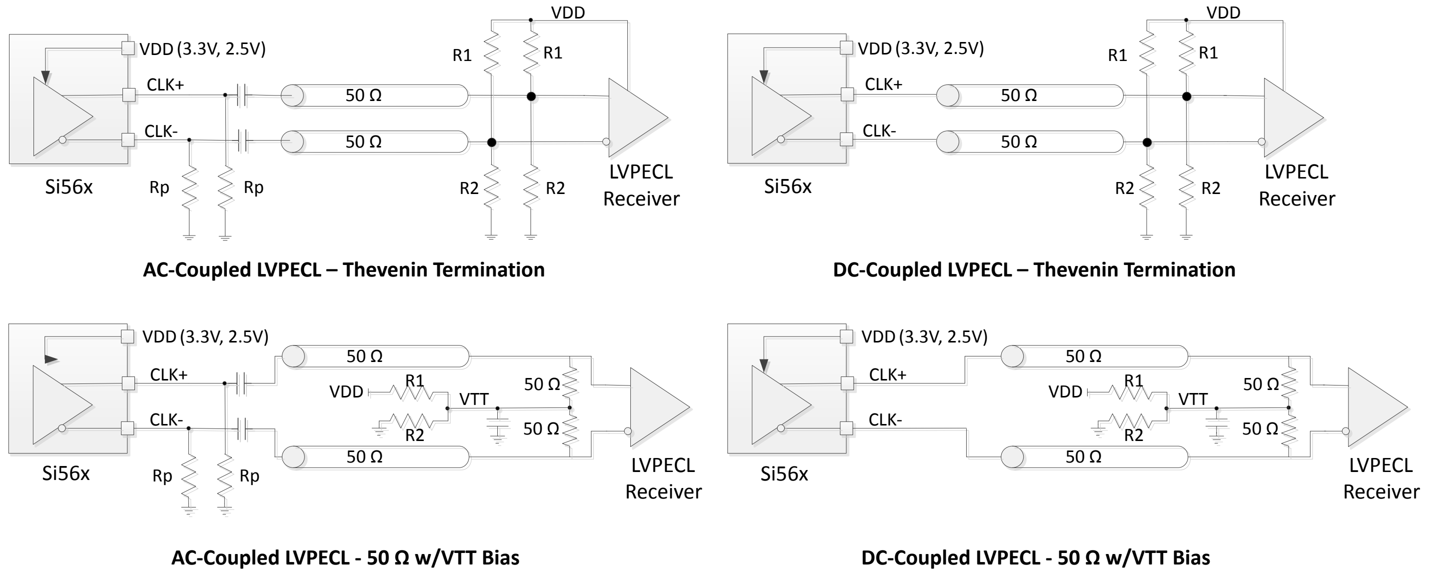


Figure 4.1. LVPECL Output Terminations

AC-Coupled LVPECL Termination Resistor Values			
VDD	R1	R2	Rp
3.3 V	127 Ω	82.5 Ω	130 Ω
2.5 V	250 Ω	62.5 Ω	90 Ω

DC-Coupled LVPECL Termination Resistor Values		
VDD	R1	R2
3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω

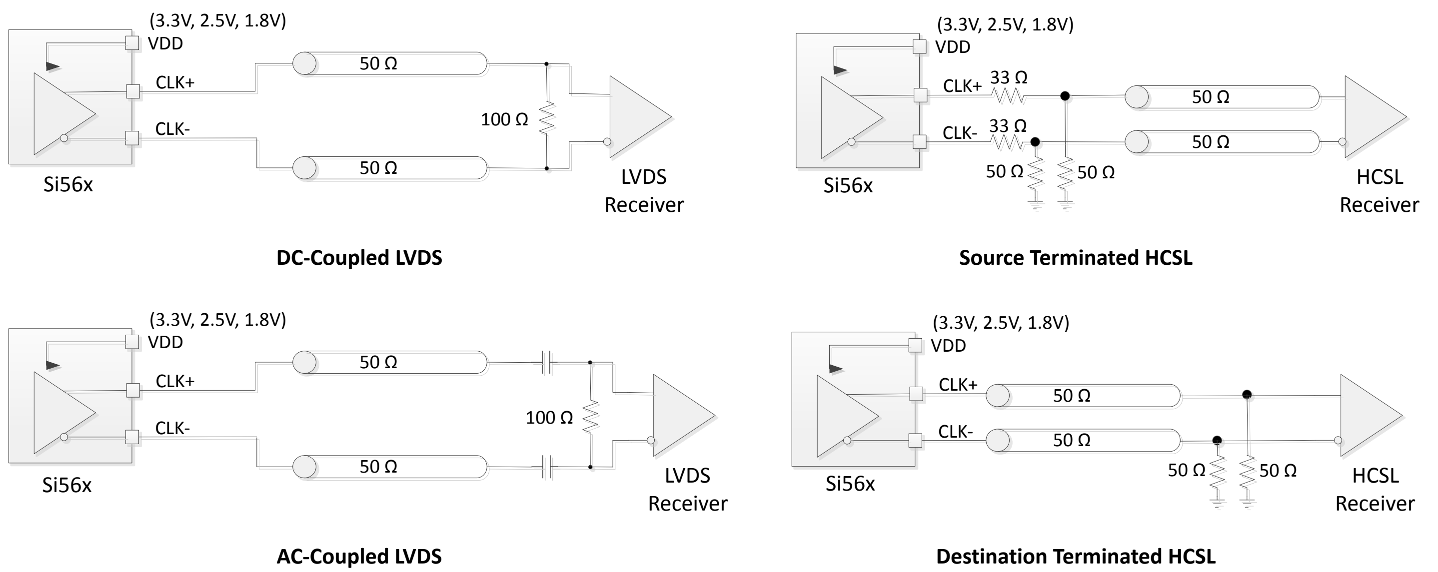


Figure 4.2. LVDS and HCSL Output Terminations

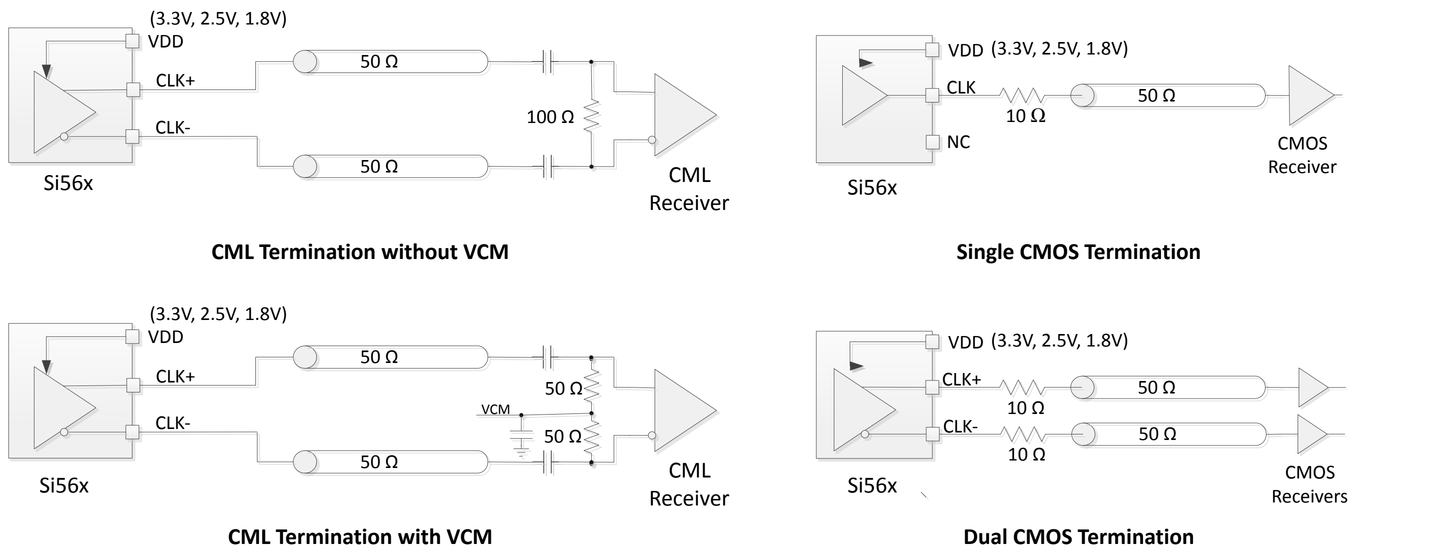


Figure 4.3. CML and CMOS Output Terminations

5. Package Outline

5.1 Package Outline (5x7 mm)

The figure below illustrates the package details for the 5x7 mm Si567. The table below lists the values for the dimensions shown in the illustration.

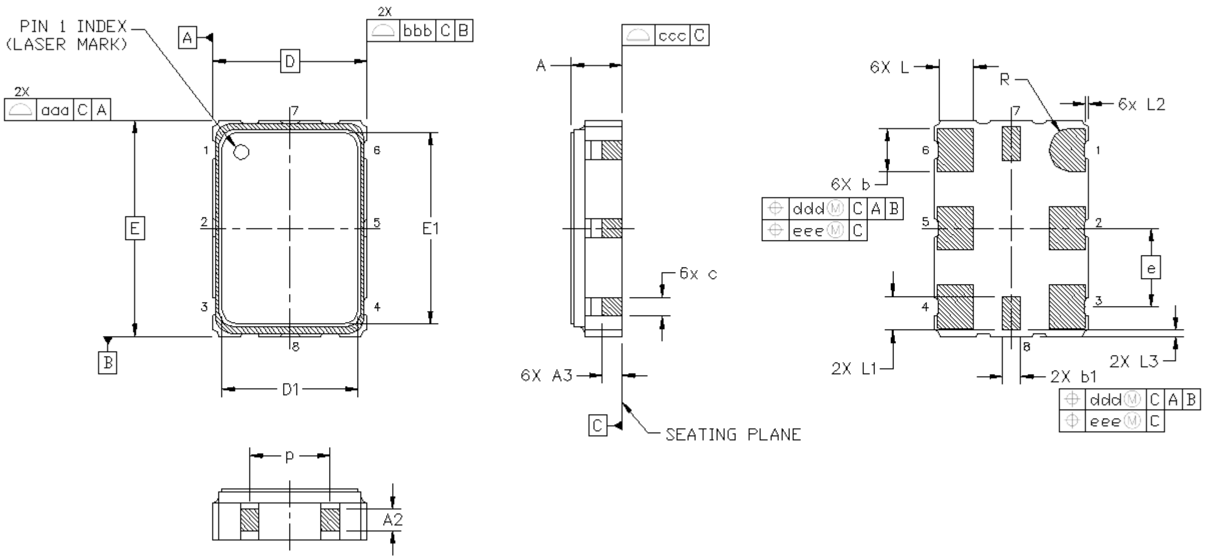


Figure 5.1. Si567 (5x7 mm) Outline Diagram

Table 5.1. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	1.07	1.18	1.33	E1	6.10	6.20	6.30
A2	0.40	0.50	0.60	L	1.07	1.17	1.27
A3	0.45	0.55	0.65	L1	1.00	1.10	1.20
b	1.30	1.40	1.50	p	1.70	--	1.90
b1	0.50	0.60	0.70	R	0.70 REF		
c	0.50	0.60	0.70	aaa	0.15		
D	5.00 BSC			bbb	0.15		
D1	4.30	4.40	4.50	ccc	0.08		
e	2.54 BSC			ddd	0.10		
E	7.00 BSC			eee	0.05		

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5.2 Package Outline (3.2x5 mm)

The figure below illustrates the package details for the 5x3.2 mm Si567. The table below lists the values for the dimensions shown in the illustration.

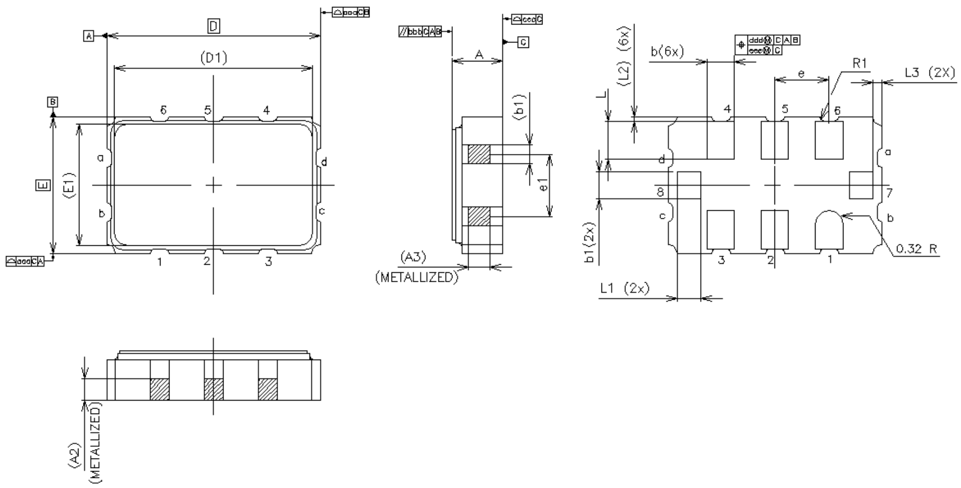


Figure 5.2. Si567 (3.2x5 mm) Outline Diagram

Table 5.2. Package Diagram Dimensions (mm)

Dimension	MIN	NOM	MAX		Dimension	MIN	NOM	MAX
A	1.02	1.17	1.33		E1		2.85 BSC	
A2	0.50	0.55	0.60		L	0.8	0.9	1.0
A3	0.45	0.50	0.55		L1	0.45	0.55	0.65
b	0.54	0.64	0.74		L2	0.05	0.10	0.15
b1	0.54	0.64	0.75		L3	0.15	0.20	0.25
D		5.00 BSC			aaa		0.15	
D1		4.65 BSC			bbb		0.15	
e		1.27 BSC			ccc		0.08	
e1		1.625 TYP			ddd		0.10	
E		3.20 BSC			eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

6. PCB Land Pattern

6.1 PCB Land Pattern (5x7 mm)

The figure below illustrates the 5x7 mm PCB land pattern for the Si567. The table below lists the values for the dimensions shown in the illustration.

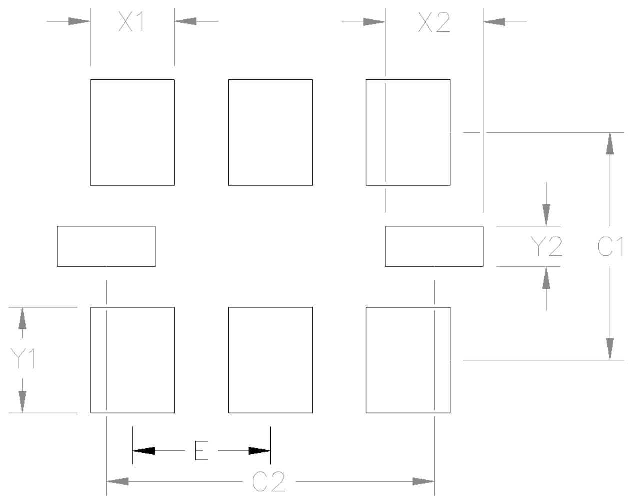


Figure 6.1. Si567 (5x7 mm) PCB Land Pattern

Table 6.1. PCB Land Pattern Dimensions (mm)

Dimension	(mm)		Dimension	(mm)
C1	4.20		Y1	1.95
C2	6.05		X2	1.80
E	2.54		Y2	0.75
X1	1.55			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

6.2 PCB Land Pattern (3.2x5 mm)

The figure below illustrates the 3.2x5.0 mm PCB land pattern for the Si567. The table below lists the values for the dimensions shown in the illustration.

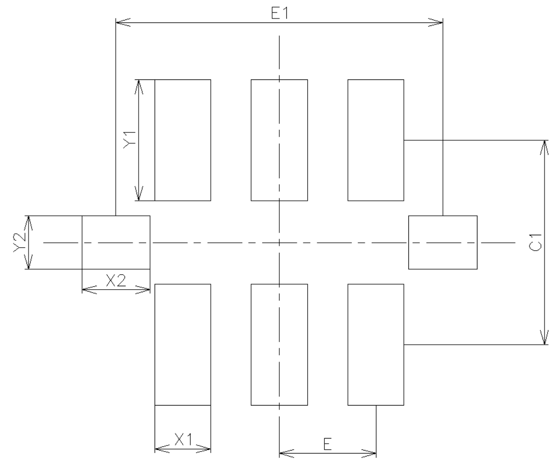


Figure 6.2. Si567 (3.2x5 mm) PCB Land Pattern

Table 6.2. PCB Land Pattern Dimensions (mm)

Dimension	(mm)		Dimension	(mm)
C1	2.70		X2	0.90
E	1.27		Y1	1.60
E1	4.30		Y2	0.70
X1	0.74			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7. Top Marking

The figure below illustrates the mark specification for the Si567. The table below lists the line information.

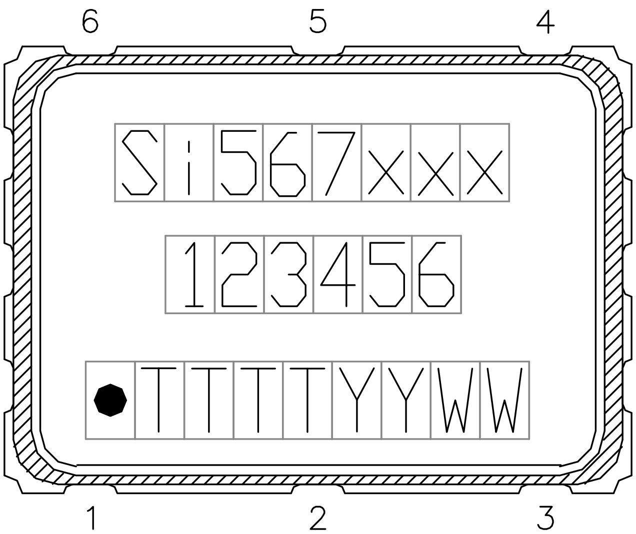


Figure 7.1. Mark Specification

Table 7.1. Si567 Top Mark Description

Line	Position	Description
1	1–8	"Si567", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si567AAA)
2	1–6	Frequency Code (6-digit custom code as described in the Ordering Guide)
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (B)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

8. Revision History

Revision 1.0

June, 2018

- Initial draft

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SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com