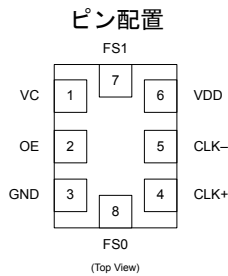


# Ultra Series™ 水晶発振器 (VCXO)

## Si567 データ・シート

### 超低ジッタ・クワッド任意周波数 VCXO (100 fs)、0.2 ~ 3000 MHz

Si567 Ultra Series™ 電圧制御水晶発振器は Silicon Laboratories の高度な第 4 世代 DSPLL® テクノロジーを使用し、超低ジッタ、低位相ノイズのクロックを選択可能な 4 つの周波数で実現します。デバイスは、0.2 ~ 3000 MHz で選択可能な 4 つの周波数に対応するよう、1 ppb 未満の分解能で工場出荷時にプログラムされ、動作範囲全体の整数周波数と分数周波数両方で非常に低いジッタを維持します。オンチップの電源フィルタリングにより、業界最先端の電源ノイズ除去性能を実現しており、スイッチング方式の電源を使用するノイズの多いシステムで、低ジッタ・クロックの生成タスクを簡素化します。Si567 は業界標準の 3.2x5 mm および 5x7 mm フットプリントで提供され、サプライ・チェーンが非常に簡素化されているため、Silicon Labs はカスタム周波数のサンプルを受注後 1 ~ 2 週間出荷できます。出力周波数ごとに異なる水晶が必要な従来の XO とは違い、Si567 は 1 つの簡単な水晶と DSPLL IC ベースのアプローチで必要な出力周波数を生成します。Si567 は、周波数、出力形式、OE ピン配列/極性など、幅広いユーザ仕様に合わせて工場出荷時に構成できます。カスタム発振器に伴う長いリード・タイムを排除するために、固有の構成は工場出荷時にプログラムされています。



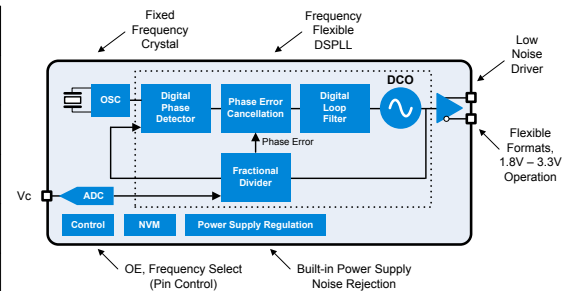
ピン番号	説明
1	VC = 電圧制御ピン
2	OE = 出力イネーブル
3	GND = グランド
4	CLK+ = クロック出力
5	CLK- = 相補クロック出力。CMOS には未使用。
6	VDD = 電源
7	FS1 = 周波数選択 1
8	FS0 = 周波数選択 0

#### 主な機能

- 200 kHz ~ 3000 MHz で選択可能な 4 つの周波数で利用可能
- 超低ジッタ : 100 fs RMS (標準値) (12 kHz ~ 20 MHz)
- 優れた PSRR および電源ノイズ耐久性 : -80 dBc (標準値)
- 同じ部品番号から、3.3 V、2.5 V および 1.8 V V<sub>DD</sub> の電源動作
- LVPECL、LVDS、CML、HCSL、CMOS、およびデュアル CMOS 出力オプション
- 3.2x5、5x7 mm パッケージ・フットプリント
- 1 ~ 2 週間のリード・タイムでサンプルを提供

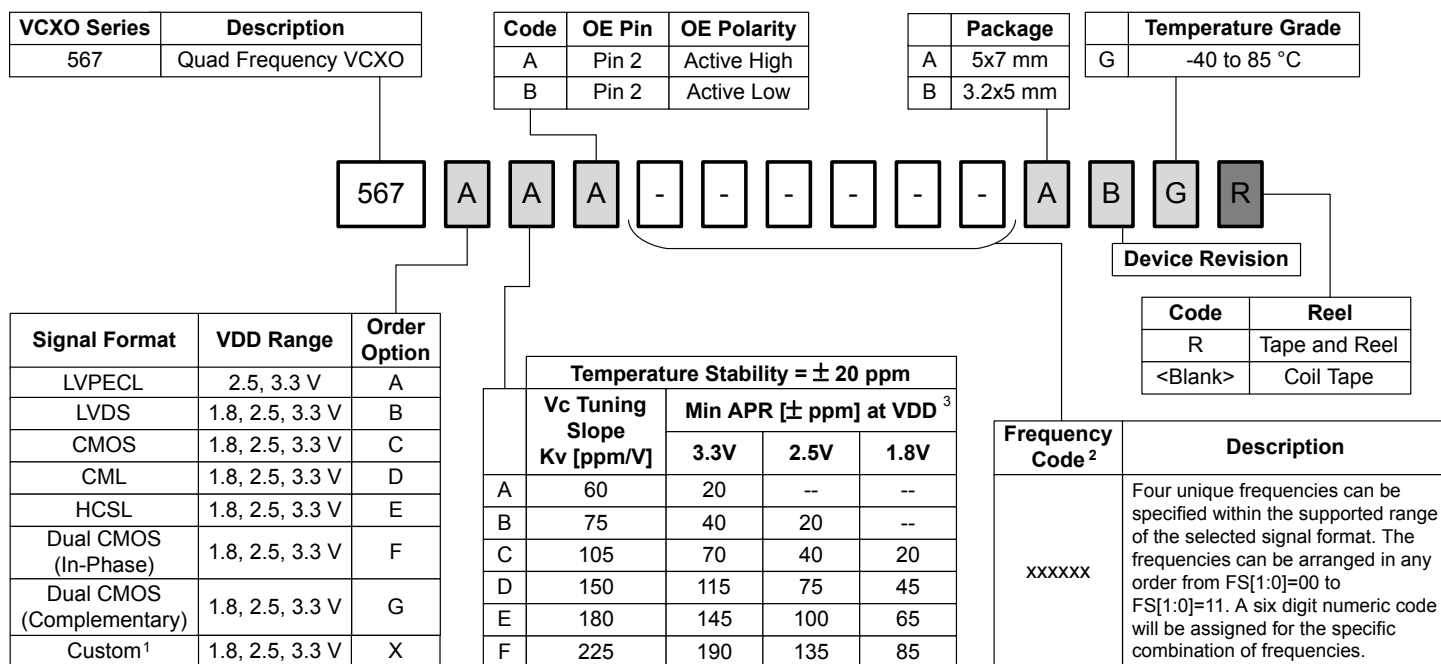
#### アプリケーション

- 100G/200G/400G OTN、コヒーレント光学
- 10G/25G/40G/100G イーサネット
- 56G/112G PAM4 クロッキング
- 3G-SDI/12G-SDI/24G-SDI 放送ビデオ
- サーバ、スイッチ、ストレージ、NIC、検索の高速化
- テストおよび測定
- FPGA/ASIC クロッキング



## 1. Ordering Guide

The Si567 VCXO supports a variety of options including frequency, output format, and OE pin location/polarity, as shown in the chart below. Specific device configurations are programmed into the part at time of shipment, and samples are available in 1-2 weeks. Silicon Laboratories provides an online part number configuration utility to simplify this process. Refer to [www.silabs.com/oscillators](http://www.silabs.com/oscillators) to access this tool and for further ordering instructions.



### Notes:

- Contact Silicon Labs for non-standard configurations.
- Create custom part numbers at [www.silabs.com/oscillators](http://www.silabs.com/oscillators).
- Min Absolute Pull Range (APR) includes temp stability, initial accuracy, load pulling, VDD variation, and 20 year aging at 70 °C.
  - For best jitter and phase noise performance, always choose the smallest Kv that meets the application's minimum APR requirements. Unlike SAW-based solutions which require higher Kv values to account for their higher temperature dependence, the Si56x series provides lower Kv options to minimize noise coupling and jitter in real-world PLL designs.
  - APR is the ability of a VCXO to track a signal over the product lifetime. A VCXO with an APR of ±20 ppm is able to lock to a clock with a ±20 ppm stability over 20 years over all operating conditions.
  - $APR (\pm) = (0.5 \times VDD \times \text{tuning slope}) - (\text{initial accuracy} + \text{temp stability} + \text{load pulling} + \text{VDD variation} + \text{aging})$ .
  - Minimum APR values noted above include absolute worst case values for all parameters.
  - See application note, "AN266: VCXO Tuning Slope (Kv), Stability, and Absolute Pull Range (APR)" for more information.

### 1.1 Technical Support

Frequently Asked Questions (FAQ)	<a href="http://www.silabs.com/Si567-FAQ">www.silabs.com/Si567-FAQ</a>
Oscillator Phase Noise Lookup Utility	<a href="http://www.silabs.com/oscillator-phase-noise-lookup">www.silabs.com/oscillator-phase-noise-lookup</a>
Quality and Reliability	<a href="http://www.silabs.com/quality">www.silabs.com/quality</a>
Development Kits	<a href="http://www.silabs.com/oscillator-tools">www.silabs.com/oscillator-tools</a>

## 2. Electrical Specifications

**Table 2.1. Electrical Specifications**
 $V_{DD} = 1.8\text{ V}, 2.5\text{ V or }3.3\text{ V} \pm 5\%$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$ 

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Temperature Range	$T_A$		-40	—	85	$^\circ\text{C}$
Frequency Range	$F_{CLK}$	LVPECL, LVDS, CML	0.2	—	3000	MHz
		HCSL	0.2	—	400	MHz
		CMOS, Dual CMOS	0.2	—	250	MHz
Supply Voltage	$V_{DD}$	3.3 V	3.135	3.3	3.465	V
		2.5 V	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
Supply Current	$I_{DD}$	LVPECL (output enabled)	—	120	170	mA
		LVDS/CML (output enabled)	—	100	167	mA
		HCSL (output enabled)	—	95	140	mA
		CMOS (output enabled)	—	95	145	mA
		Dual CMOS (output enabled)	—	105	155	mA
		Tristate Hi-Z (output disabled)	—	83	—	mA
Temperature Stability <sup>1</sup>		-40 to 85 $^\circ\text{C}$	-20	—	20	ppm
Rise/Fall Time (20% to 80% $V_{PP}$ )	$T_R/T_F$	LVPECL/LVDS/CML	—	—	350	ps
		CMOS / Dual CMOS ( $C_L = 5\text{ pF}$ )	—	0.5	1.5	ns
		HCSL, $F_{CLK} > 50\text{ MHz}$	—	—	550	ps
Duty Cycle	$D_C$	All formats	45	—	55	%
Output Enable (OE) Frequency Select (FS0, FS1) <sup>2</sup>	$V_{IH}$		$0.7 \times V_{DD}$	—	—	V
	$V_{IL}$		—	—	$0.3 \times V_{DD}$	V
	$T_D$	Output Disable Time, $F_{CLK} > 10\text{ MHz}$	—	—	3	$\mu\text{s}$
	$T_E$	Output Enable Time, $F_{CLK} > 10\text{ MHz}$	—	—	20	$\mu\text{s}$
	$T_{FS}$	Settling Time after FS Change	—	—	10	ms
Powerup Time	$t_{OSC}$	Time from $0.9 \times V_{DD}$ until output frequency ( $F_{CLK}$ ) within spec	—	—	10	ms
LVPECL Output Option <sup>3</sup>	$V_{OC}$	Mid-level	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
	$V_O$	Swing (diff, $F_{CLK} \leq 1.5\text{ GHz}$ )	1.1	—	1.9	$V_{PP}$
		Swing (diff, $F_{CLK} > 1.5\text{ GHz}$ ) <sup>6</sup>	0.55	—	1.7	$V_{PP}$

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
LVDS Output Option <sup>4</sup>	V <sub>OC</sub>	Mid-level (2.5 V, 3.3 V V <sub>DD</sub> )	1.125	1.20	1.275	V
		Mid-level (1.8 V V <sub>DD</sub> )	0.8	0.9	1.0	V
	V <sub>O</sub>	Swing (diff, F <sub>CLK</sub> ≤ 1.5 GHz)	0.5	0.7	0.9	V <sub>PP</sub>
		Swing (diff, F <sub>CLK</sub> > 1.5 GHz) <sup>6</sup>	0.25	0.5	0.8	V <sub>PP</sub>
HCSL Output Option <sup>5</sup>	V <sub>OH</sub>	Output voltage high	660	800	850	mV
	V <sub>OL</sub>	Output voltage low	-150	0	150	mV
	V <sub>C</sub>	Crossing voltage	250	410	550	mV
CML Output Option (AC-Coupled)	V <sub>O</sub>	Swing (diff, F <sub>CLK</sub> ≤ 1.5 GHz) <sup>6</sup>	0.6	0.8	1.0	V <sub>PP</sub>
		Swing (diff, F <sub>CLK</sub> > 1.5 GHz) <sup>6</sup>	0.3	0.55	0.9	V <sub>PP</sub>
CMOS Output Option	V <sub>OH</sub>	I <sub>OH</sub> = 8/6/4 mA for 3.3/2.5/1.8 V V <sub>DD</sub>	0.85 × V <sub>DD</sub>	—	—	V
	V <sub>OL</sub>	I <sub>OL</sub> = 8/6/4 mA for 3.3/2.5/1.8 V V <sub>DD</sub>	—	—	0.15 × V <sub>DD</sub>	V

**Notes:**

1. Min APR includes temperature stability, initial accuracy, load pulling, V<sub>DD</sub> variation, and aging for 20 yrs at 70 °C.
2. OE includes a 50 kΩ pull-up to V<sub>DD</sub> for OE active high, or includes a 50 kΩ pull-down to GND for OE active low. FS0 and FS1 pins each include a 50 kΩ pull-up to V<sub>DD</sub>.
3. R<sub>term</sub> = 50 Ω to V<sub>DD</sub> - 2.0 V (see Figure 4.1).
4. R<sub>term</sub> = 100 Ω (differential) (see Figure 4.2).
5. R<sub>term</sub> = 50 Ω to GND (see Figure 4.2).
6. Refer to the figure below for Typical Clock Output Swing Amplitudes vs Frequency.

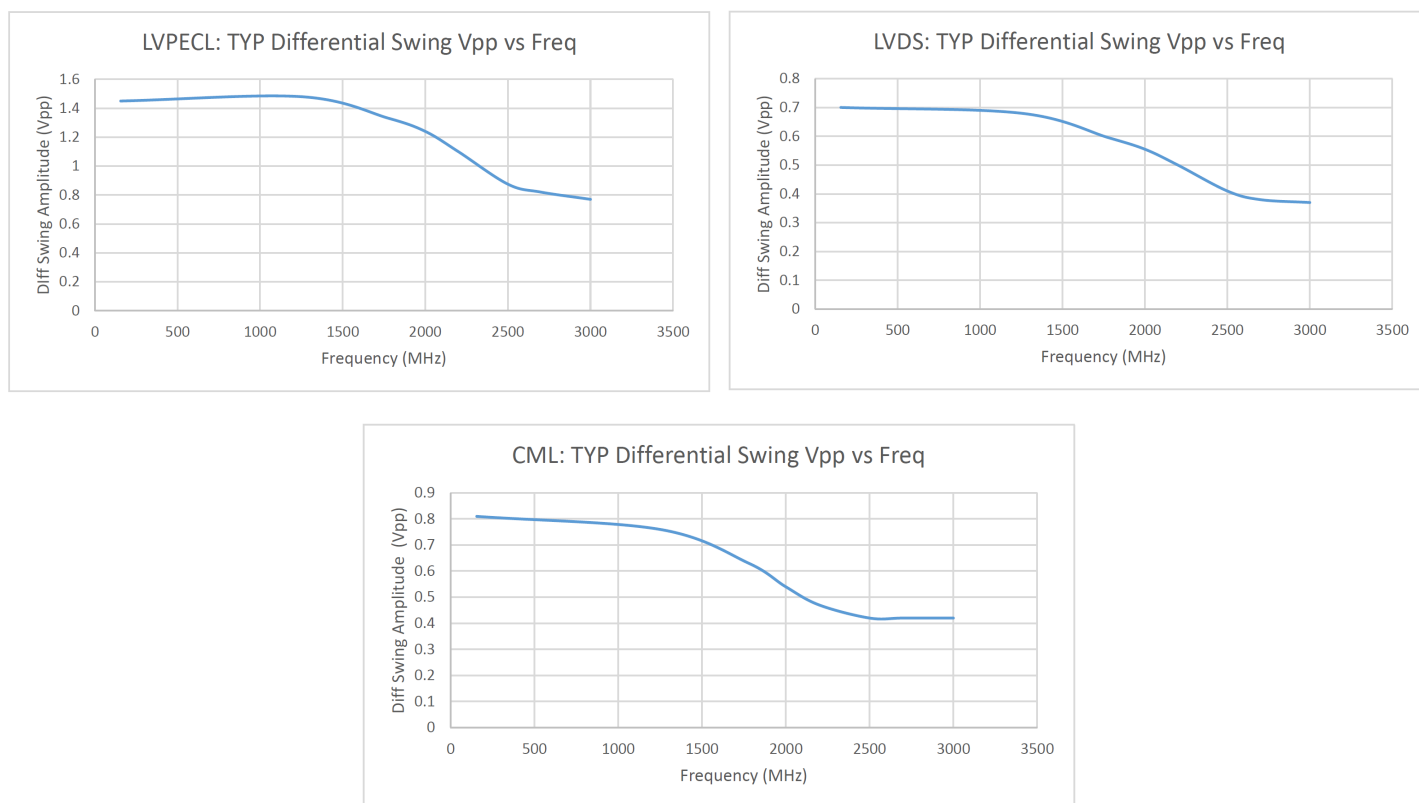
**Figure 2.1. Typical Clock Output Swing Amplitudes vs. Frequency**

Table 2.2.  $V_C$  Control Voltage Input $V_{DD} = 1.8, 2.5$  or  $3.3 V \pm 5\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ 

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Control Voltage Range	$V_C$		$0.1 \times V_{DD}$	$V_{DD}/2$	$0.9 \times V_{DD}$	V
Control Voltage Tuning Slope ( $V_C = 10\% V_{DD}$ to $90\% V_{DD}$ )	Kv	Positive slope, ordering option	60, 75, 105, 150, 180, 225			ppm/V
Kv Variation	Kv_var		—	—	$\pm 10$	%
Control Voltage Linearity	LVC	Best Straight Line fit	-1.5	$\pm 0.5$	+1.5	%
Modulation Bandwidth	BW		—	10	—	kHz
Vc Input Impedance	ZVC		500	—	—	k $\Omega$

Table 2.3. Clock Output Phase Jitter and PSRR

 $V_{DD} = 1.8 V, 2.5$  or  $3.3 V \pm 5\%$ ,  $T_A = -40$  to  $85\text{ }^\circ\text{C}$ 

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> All Differential Formats, $F_{CLK} \geq 200$ MHz	$\phi_J$	Kv = 60 ppm/V	—	100	150	fs
		Kv = 75 ppm/V	—	103	—	fs
		Kv = 105 ppm/V	—	110	—	fs
		Kv = 150 ppm/V	—	123	—	fs
		Kv = 180 ppm/V	—	132	—	fs
		Kv = 225 ppm/V	—	150	—	fs
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> All Diff Formats, $100 \text{ MHz} \leq F_{CLK} < 200$ MHz	$\phi_J$	Kv = 60 ppm/V	—	115	170	fs
		Kv = 75 ppm/V	—	118	—	fs
		Kv = 105 ppm/V	—	125	—	fs
		Kv = 150 ppm/V	—	138	—	fs
		Kv = 180 ppm/V	—	147	—	fs
		Kv = 225 ppm/V	—	165	—	fs
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> LVDS, $F_{CLK} = 156.25$ MHz	$\phi_J$	Kv = 60 ppm/V	—	110	130	fs
		Kv = 75 ppm/V	—	113	—	fs
		Kv = 105 ppm/V	—	120	—	fs
		Kv = 150 ppm/V	—	133	—	fs
		Kv = 180 ppm/V	—	142	—	fs
		Kv = 225 ppm/V	—	160	—	fs
Phase Jitter (RMS, 12 kHz - 20 MHz) <sup>1</sup> CMOS / Dual CMOS Formats	$\phi_J$	$10 \text{ MHz} \leq F_{CLK} < 250 \text{ MHz}$	—	200	—	fs

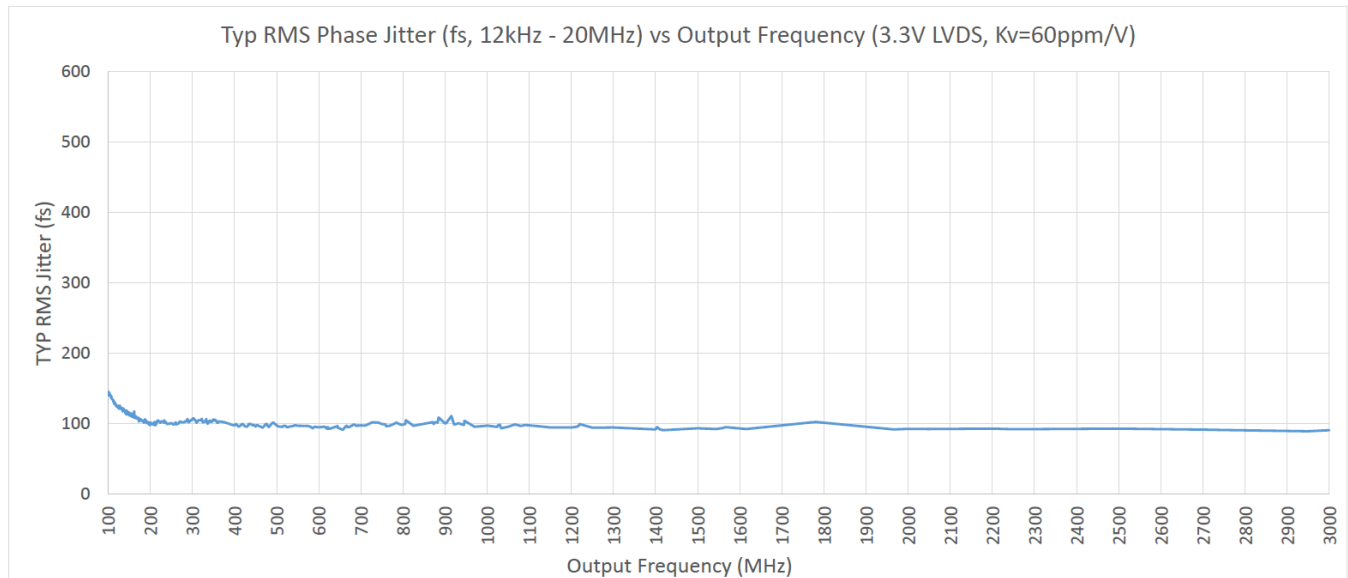
Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Spurs Induced by External Power Supply Noise, 50 mVpp Ripple. LVDS 156.25 MHz Output	PSRR	100 kHz sine wave		-83		dBc
		200 kHz sine wave		-83		
		500 kHz sine wave		-82		
		1 MHz sine wave		-85		

**Note:**

1. Jitter inclusive of any spurs.

**Table 2.4. 3.2 x 5 mm Clock Output Phase Noise (Typical)**

Offset Frequency (f)	156.25 MHz LVDS	200 MHz LVDS	644.53125 MHz LVDS	Unit
100 Hz	-73	-71	-60	dBc/Hz
1 kHz	-102	-102	-93	
10 kHz	-130	-128	-118	
100 kHz	-141	-139	-129	
1 MHz	-150	-148	-138	
10 MHz	-159	-160	-153	
20 MHz	-160	-162	-154	
Offset Frequency (f)	156.25 MHz LVPECL	200 MHz LVPECL	644.53125 MHz LVPECL	Unit
100 Hz	-72	-71	-60	dBc/Hz
1 kHz	-103	-101	-92	
10 kHz	-130	-127	-117	
100 kHz	-142	-139	-129	
1 MHz	-150	-148	-138	
10 MHz	-160	-162	-154	
20 MHz	-161	-162	-156	



**Figure 2.2. Phase Jitter vs. Output Frequency**

Phase jitter measured with Agilent E5052 using a differential-to-single ended converter (balun or buffer). Measurements collected for >700 commonly used frequencies. Phase noise plots for specific frequencies are available using our free, online Oscillator Phase Noise Lookup Tool at [www.silabs.com/oscillators](http://www.silabs.com/oscillators).

**Table 2.5. Environmental Compliance and Package Information**

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Moisture Sensitivity Level (MSL)	1
Contact Pads	Gold over Nickel

**Note:**

- For additional product information not listed in the data sheet (e.g. RoHS Certifications, MDDS data, qualification data, REACH Declarations, ECCN codes, etc.), refer to our "Corporate Request For Information" portal found here: [www.silabs.com/support/quality/Pages/RoHSInformation.aspx](http://www.silabs.com/support/quality/Pages/RoHSInformation.aspx).

**Table 2.6. Thermal Conditions**

Package	Parameter	Symbol	Test Condition	Value	Unit
3.2×5 mm 8-pin CLCC	Thermal Resistance Junction to Ambient	$\Theta_{JA}$	Still Air, 85 °C	79.1	°C/W
	Thermal Resistance Junction to Board	$\Theta_{JB}$	Still Air, 85 °C	49.6	°C/W
	Max Junction Temperature	$T_J$	Still Air, 85 °C	125	°C
5×7 mm 8-pin CLCC	Thermal Resistance Junction to Ambient	$\Theta_{JA}$	Still Air, 85 °C	67.1	°C/W
	Thermal Resistance Junction to Board	$\Theta_{JB}$	Still Air, 85 °C	51.7	°C/W
	Max Junction Temperature	$T_J$	Still Air, 85 °C	125	°C

**Table 2.7. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Rating	Unit
Maximum Operating Temp.	$T_{AMAX}$	95	°C
Storage Temperature	$T_S$	-55 to 125	°C
Supply Voltage	$V_{DD}$	-0.5 to 3.8	°C
Input Voltage	$V_{IN}$	-0.5 to $V_{DD} + 0.3$	V
ESD HBM (JESD22-A114)	HBM	2.0	kV
Solder Temperature <sup>2</sup>	$T_{PEAK}$	260	°C
Solder Time at $T_{PEAK}$ <sup>2</sup>	$T_P$	20–40	sec

**Notes:**

- Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
- The device is compliant with JEDEC J-STD-020.



### 3. Dual CMOS Buffer

Dual CMOS output format ordering options support either complementary or in-phase signals for two identical frequency outputs. This feature enables replacement of multiple VCXOs with a single Si567 device.



Figure 3.1. Integrated 1:2 CMOS Buffer Supports Complementary or In-Phase Outputs

## 4. Recommended Output Terminations

The output drivers support both AC-coupled and DC-coupled terminations as shown in figures below.



Figure 4.1. LVPECL Output Terminations

AC-Coupled LVPECL Termination Resistor Values				DC-Coupled LVPECL Termination Resistor Values		
VDD	R1	R2	Rp	VDD	R1	R2
3.3 V	127 Ω	82.5 Ω	130 Ω	3.3 V	127 Ω	82.5 Ω
2.5 V	250 Ω	62.5 Ω	90 Ω	2.5 V	250 Ω	62.5 Ω



Figure 4.2. LVDS and HCSL Output Terminations

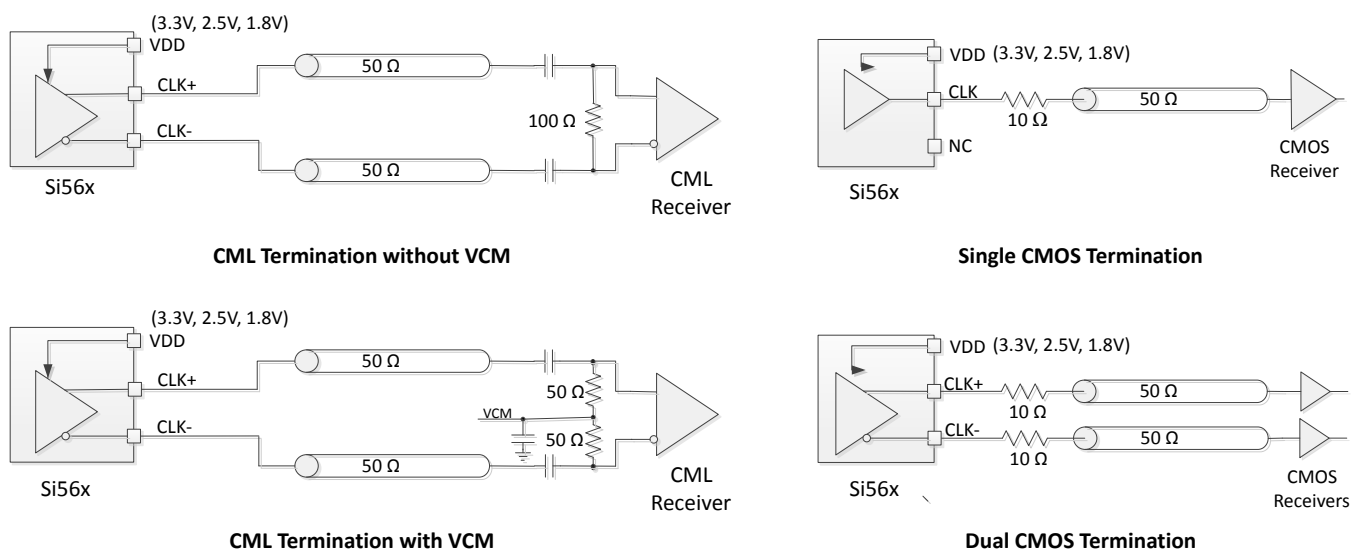


Figure 4.3. CML and CMOS Output Terminations

## 5. Package Outline

### 5.1 Package Outline (5x7 mm)

The figure below illustrates the package details for the 5x7 mm Si567. The table below lists the values for the dimensions shown in the illustration.

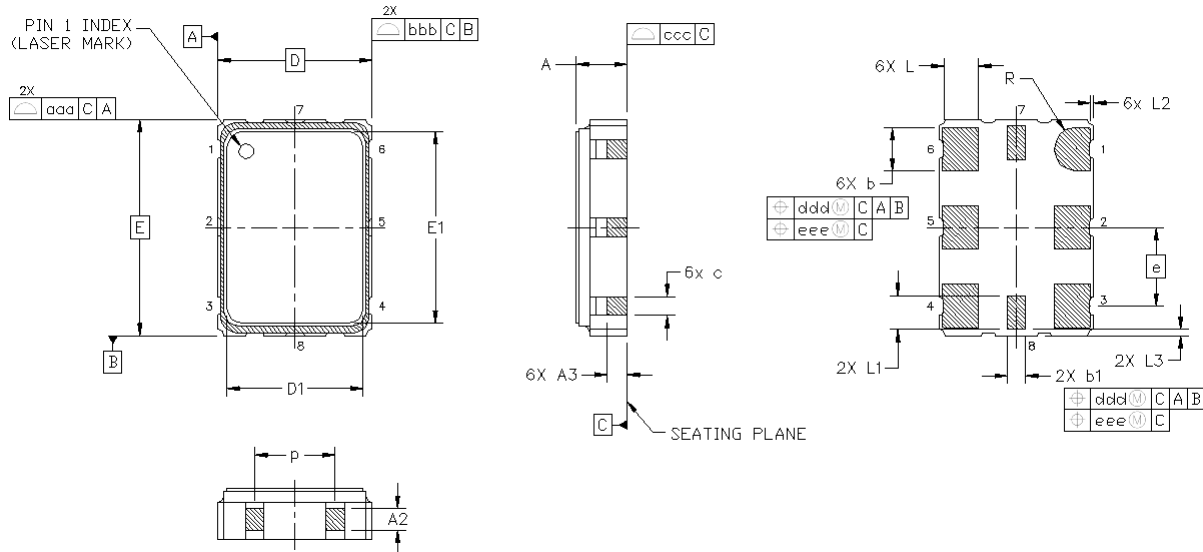


Figure 5.1. Si567 (5x7 mm) Outline Diagram

Table 5.1. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	1.07	1.18	1.33	E1	6.10	6.20	6.30
A2	0.40	0.50	0.60	L	1.07	1.17	1.27
A3	0.45	0.55	0.65	L1	1.00	1.10	1.20
b	1.30	1.40	1.50	p	1.70	--	1.90
b1	0.50	0.60	0.70	R	0.70 REF		
c	0.50	0.60	0.70	aaa	0.15		
D	5.00 BSC			bbb	0.15		
D1	4.30	4.40	4.50	ccc	0.08		
e	2.54 BSC			ddd	0.10		
E	7.00 BSC			eee	0.05		

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 5.2 Package Outline (3.2x5 mm)

The figure below illustrates the package details for the 5x3.2 mm Si567. The table below lists the values for the dimensions shown in the illustration.



Figure 5.2. Si567 (3.2x5 mm) Outline Diagram

Table 5.2. Package Diagram Dimensions (mm)

Dimension	MIN	NOM	MAX	Dimension	MIN	NOM	MAX
A	1.02	1.17	1.33	E1	2.85 BSC		
A2	0.50	0.55	0.60	L	0.8	0.9	1.0
A3	0.45	0.50	0.55	L1	0.45	0.55	0.65
b	0.54	0.64	0.74	L2	0.05	0.10	0.15
b1	0.54	0.64	0.75	L3	0.15	0.20	0.25
D	5.00 BSC			aaa	0.15		
D1	4.65 BSC			bbb	0.15		
e	1.27 BSC			ccc	0.08		
e1	1.625 TYP			ddd	0.10		
E	3.20 BSC			eee	0.05		

### Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 6. PCB Land Pattern

### 6.1 PCB Land Pattern (5x7 mm)

The figure below illustrates the 5x7 mm PCB land pattern for the Si567. The table below lists the values for the dimensions shown in the illustration.



Figure 6.1. Si567 (5x7 mm) PCB Land Pattern

Table 6.1. PCB Land Pattern Dimensions (mm)

Dimension	(mm)	Dimension	(mm)
C1	4.20	Y1	1.95
C2	6.05	X2	1.80
E	2.54	Y2	0.75
X1	1.55		

#### Notes:

##### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

##### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

##### Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

##### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

## 6.2 PCB Land Pattern (3.2x5 mm)

The figure below illustrates the 3.2x5.0 mm PCB land pattern for the Si567. The table below lists the values for the dimensions shown in the illustration.



Figure 6.2. Si567 (3.2x5 mm) PCB Land Pattern

Table 6.2. PCB Land Pattern Dimensions (mm)

Dimension	(mm)	Dimension	(mm)
C1	2.70	X2	0.90
E	1.27	Y1	1.60
E1	4.30	Y2	0.70
X1	0.74		

### Notes:

#### General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

#### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

#### Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

#### Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

## 7. Top Marking

The figure below illustrates the mark specification for the Si567. The table below lists the line information.

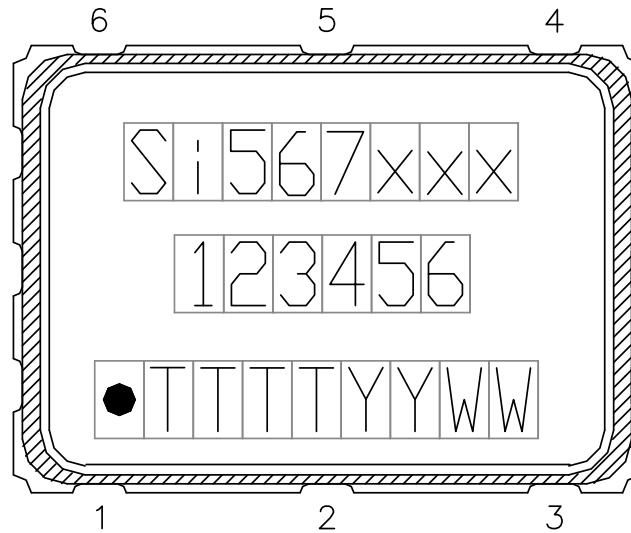


Figure 7.1. Mark Specification

Table 7.1. Si567 Top Mark Description

Line	Position	Description
1	1–8	"Si567", xxx = Ordering Option 1, Option 2, Option 3 (e.g. Si567AAA)
2	1–6	Frequency Code (6-digit custom code as described in the Ordering Guide)
3	<b>Trace Code</b>	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (B)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of the year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site



## 8. Revision History

### Revision 1.0

June, 2018

- Initial draft



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Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

<http://www.silabs.com>