

1 ps 最大抖动晶体振荡器 (XO) (10 MHz 至 810 MHz)

特性

- 在 10 至 810 MHz 之间的任意频率输出频率下可用
- 具有卓越抖动性能的第 3 代 DSPLL[®]: 1 ps 最大抖动
- 频率稳定性高于基于 SAW 的振荡器
- 内部基础模式晶体确保高可靠性
- 提供 CMOS、LVPECL、LVDS 和 CML 输出
- 3.3、2.5 和 1.8 V 电源选项
- 符合行业标准的 5x7 和 3.2x5 毫米封装
- 无铅 / 符合 RoHS
- 工作温度范围为 -40 至 +85 °C

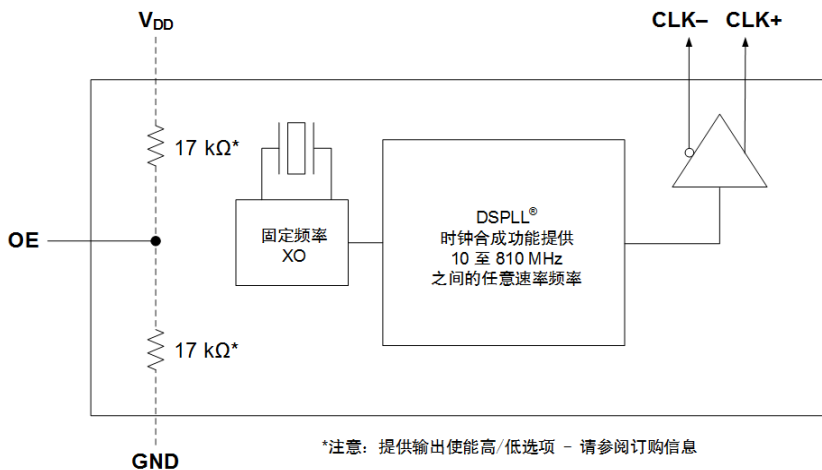
应用

- SONET/SDH (OC-3/12/48)
- 网络
- SD/HD SDI/3G SDI 视频
- 测试和测量
- 存储
- FPGA/ASIC 时钟脉冲振荡

说明

Si590/591 XO 采用 Silicon Laboratories 先进的 DSPLL[®] 电路, 可在高频率下提供低抖动时钟。Si590/591 支持 10 至 810 MHz 之间的任意频率。不同于传统 XO 对于各个输出频率都需要使用唯一的晶体, Si590/591 使用一个固定晶体即可提供宽范围的输出频率。借助这个基于 IC 的方法, 晶体谐振器的频率稳定性和可靠性达到一流水平。另外, DSPLL 时钟合成提供了出色的电源噪声抑制, 简化了在嘈杂环境中生成低抖动时钟的任务 (常见于通信系统中)。可针对各种各样的用户规格要求在工厂内对基于 IC 的 Si590/591 XO 进行配置, 包括频率、电源电压、输出格式和稳定性。特殊配置在发货时经过出厂编程, 因此消除了定制振荡器所导致的长交付周期。

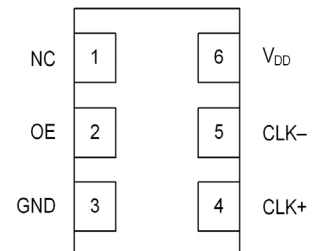
功能方框图



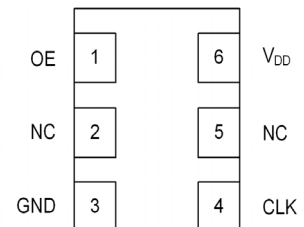
订购信息:
请参阅第 7 页。

引脚分配:
请参阅第 6 页。

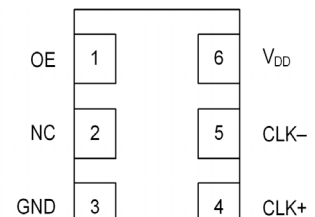
(俯视图)



Si590 (LVDS/LVPECL/CML)



Si590 (CMOS)



Si591 (LVDS/LVPECL/CML)

TABLE OF CONTENTS

1. Electrical Specifications	3
2. Pin Descriptions	7
3. Ordering Information	8
4. Package Outline Drawing: 5 x 7 mm, 6-pin	9
5. PCB Land Pattern: 5 x 7 mm, 6-pin	10
6. Package Outline Drawing: 3.2 x 5 mm, 6-pin	11
7. PCB Land Pattern: 3.2 x 5 mm, 6-pin	12
8. Si590/Si591 Top Marking: 5 x 7 mm	13
9. Si590/Si591 Top Marking: 3.2 x 5 mm	14
Revision History	15

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage ¹	V _{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	I _{DD}	Output enabled LVPECL	—	110	125	mA
		CML	—	100	110	
		LVDS	—	90	100	
		CMOS	—	80	90	
		Tristate mode	—	60	75	
Output Enable (OE) ²		V _{IH}	0.75 x V _{DD}	—	—	V
		V _{IL}	—	—	0.5	
Operating Temperature Range	T _A		−40	—	85	°C

Notes:

- Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 8 for further details.
- OE pin includes an internal 17 kΩ pullup resistor to V_{DD} for output enable active high or a 17 kΩ pull-down resistor to GND for output enable active low. See 3. "Ordering Information" on page 8.

Table 2. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency ^{1,2}	f _O	LVPECL/LVDS/CML	10	—	810	MHz
		CMOS	10	—	160	
Initial Accuracy	f _i	Measured at +25 °C at time of shipping	—	±1.5	—	ppm
Total Stability		Note 3, second option code "D"	—	—	±20	ppm
		Note 3, second option code "C"	—	—	±30	ppm
		Note 4, second option code "B"	—	—	±50	ppm
		Note 4, second option code "A"	—	—	±100	ppm
Temperature Stability		second option code "D"	—	—	±7	ppm
		second option code "C"	—	—	±20	ppm
		second option code "B"	—	—	±25	ppm
		second option code "A"	—	—	±50	ppm
Powerup Time ⁵	t _{OSC}		—	—	10	ms

Notes:

- See Section 3. "Ordering Information" on page 8 for further details.
- Specified at time of order by part number.
- Includes initial accuracy, temperature, shock, vibration, power supply and load drift, and 10 years aging at 40 °C. See 3. "Ordering Information" on page 8.
- Includes initial accuracy, temperature, shock, vibration, power supply and load drift, and 15 years aging at 70 °C. See 3. "Ordering Information" on page 8.
- Time from powerup or tristate mode to f_O.

Table 3. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option ¹	V_O	mid-level	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option ²	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.5	0.7	0.9	V_{PP}
CML Output Option ²	V_O	2.5/3.3 V option mid-level	—	$V_{DD} - 1.30$	—	V
		1.8 V option mid-level	—	$V_{DD} - 0.36$	—	
	V_{OD}	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	V_{PP}
		1.8 V option swing (diff)	0.35	0.425	0.50	
CMOS Output Option ³	V_{OH}		$0.8 \times V_{DD}$	—	V_{DD}	V
	V_{OL}		—	—	0.4	
Rise/Fall time (20/80%)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with $C_L = 15$ pF	—	2	—	ns
Symmetry (duty cycle)	SYM	LVPECL: $V_{DD} - 1.3$ V (diff) LVDS: 1.25 V (diff) CMOS: $V_{DD}/2$	45	—	55	%

Notes:

1. 50Ω to $V_{DD} - 2.0$ V.
2. $R_{term} = 100 \Omega$ (differential).
3. $C_L = 15$ pF. Sinking or sourcing 12 mA for $V_{DD} = 3.3$ V, 6 mA for $V_{DD} = 2.5$ V, 3 mA for $V_{DD} = 1.8$ V.

Table 4. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS) ¹ for $50 \text{ MHz} \leq F_{OUT} \leq 810 \text{ MHz}$ (LVPECL/LVDS/CML)	ϕ_J	12 kHz to 20 MHz	—	0.5	1.0	ps
Phase Jitter (RMS) ¹ (LVPECL/LVDS/CML)	ϕ_J	12 kHz to 20 MHz, 155.52 MHz output frequency	—	0.4	0.7	ps
Phase Jitter (RMS) ² for $50 \text{ MHz} \leq F_{OUT} \leq 160 \text{ MHz}$ (CMOS)	ϕ_J	12 kHz to 20 MHz	—	0.6	1.0	ps

Notes:

1. Refer to AN256 for further information.
2. Single-ended CMOS output phase jitter measured using 33Ω series termination into 50Ω phase noise test equipment. 3.3 V supply voltage option only.

Table 5. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J _{PER}	RMS	—	—	3	ps
		Peak-to-Peak	—	—	35	

*Note: Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

Table 6. Environmental Compliance and Package Information

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Contact Pads	Gold over Nickel

Table 7. Thermal Characteristics

(Typical values T_A = 25 °C, V_{DD} = 3.3 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5x7mm, Thermal Resistance Junction to Ambient	θ _{JA}	Still Air	—	84.6	—	°C/W
5x7mm, Thermal Resistance Junction to Case	θ _{JC}	Still Air	—	38.8	—	°C/W
3.2x5mm, Thermal Resistance Junction to Ambient	θ _{JA}	Still Air	—	31.1	—	°C/W
3.2x5mm, Thermal Resistance Junction to Case	θ _{JC}	Still Air	—	13.3	—	°C/W
Ambient Temperature	T _A		-40	—	85	°C
Junction Temperature	T _J		—	—	125	°C

Table 8. Absolute Maximum Ratings¹

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T_{AMAX}	85	°C
Supply Voltage, 1.8 V Option	V_{DD}	-0.5 to +1.9	V
Supply Voltage, 2.5/3.3 V Option	V_{DD}	-0.5 to +3.8	V
Input Voltage (any input pin)	V_I	-0.5 to $V_{DD} + 0.3$	V
Storage Temperature	T_S	-55 to +125	°C
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	V
Soldering Temperature (Pb-free profile) ²	T_{PEAK}	260	°C
Soldering Temperature Time @ T_{PEAK} (Pb-free profile) ²	t_P	20–40	seconds

Notes:

1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download at www.silabs.com/VCXO for further information, including soldering profiles.

2. Pin Descriptions

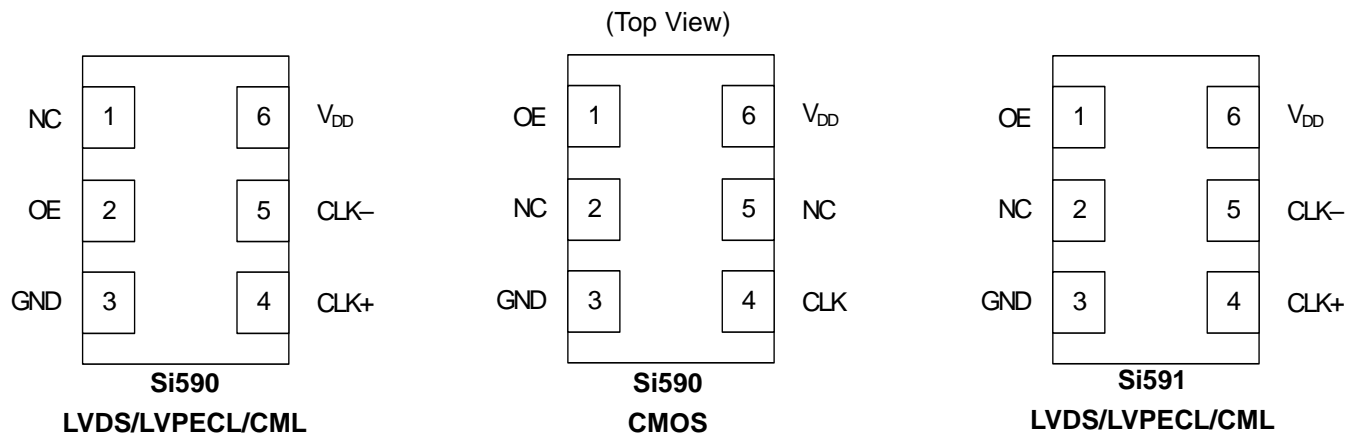


Table 9. Pinout for Si590 Series

Pin	Symbol	LVDS/LVPECL/CML Function	CMOS Function
1	OE*	No connection Make no external connection to this pin	Output enable
2	OE*	Output enable	No connection Make no external connection to this pin
3	GND	Electrical and Case Ground	Electrical and Case Ground
4	CLK+	Oscillator Output	Oscillator Output
5	CLK-	Complementary Output	No connection Make no external connection to this pin
6	V _{DD}	Power Supply Voltage	Power Supply Voltage

***Note:** OE pin includes an internal 17 kΩ pullup resistor to V_{DD} for output enable active high or a 17 kΩ pulldown resistor to GND for output enable active low. See 3. "Ordering Information" on page 8.

Table 10. Pinout for Si591 Series

Pin	Symbol	LVDS/LVPECL/CML Function
1	OE*	Output enable
2	No connection Make no external connection to this pin	No connection Make no external connection to this pin
3	GND	Electrical and Case Ground
4	CLK+	Oscillator Output
5	CLK-	Complementary output
6	V _{DD}	Power Supply Voltage

***Note:** OE pin includes an internal 17 kΩ pullup resistor to V_{DD} for output enable active high or a 17 kΩ pulldown resistor to GND for output enable active low. See 3. "Ordering Information" on page 8.

3. Ordering Information

The Si590/591 XO supports a variety of options including frequency, temperature stability, output format, and V_{DD} . Specific device configurations are programmed into the Si590/591 at time of shipment. Configurations can be specified using the Part Number Configuration chart below. Silicon Laboratories provides a web browser-based part number configuration utility to simplify this process. To access this tool refer to www.silabs.com/oscillators and click "Customize" in the product table. The Si590 and Si591 XO series are supplied in an industry-standard, RoHS compliant, 6-pad, 5 x 7 mm and 3.2 x 5 mm packages. The Si591 Series supports an alternate OE pinout (pin #1) for LVPECL, LVDS, and CML output formats. See Tables 9 and 10 for the pinout differences between the Si590 and Si591 series.

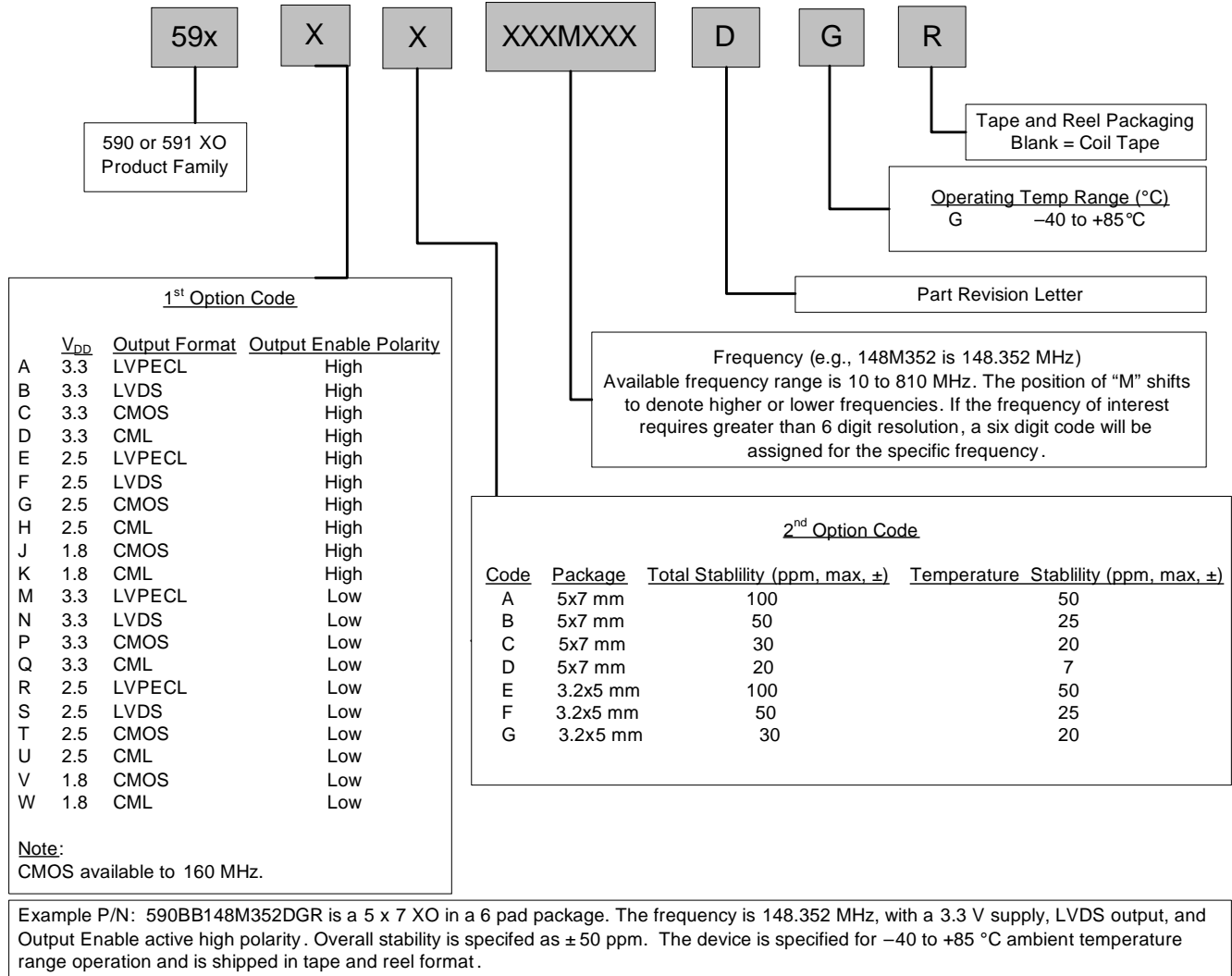


Figure 1. Part Number Convention

4. Package Outline Drawing: 5 x 7 mm, 6-pin

Figure 2 illustrates the package details for the 5 x 7 mm Si590/591. Table 11 lists the values for the dimensions shown in the illustration.

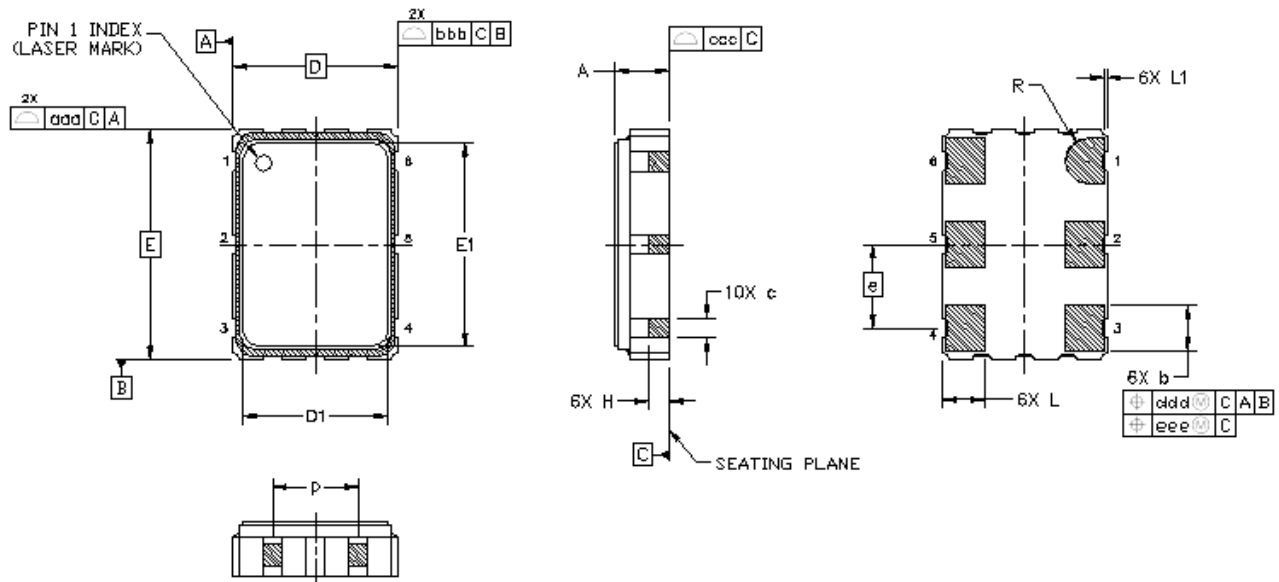


Figure 2. Si590/591 Outline Diagram

Table 11. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D	5.00 BSC		
D1	4.30	4.40	4.50
e	2.54 BSC		
E	7.00 BSC		
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	0.05	0.10	0.15
p	1.80	—	2.60
R	0.70 REF		
aaa	0.15		
bbb	0.15		
ccc	0.10		
ddd	0.10		
eee	0.05		

5. PCB Land Pattern: 5 x 7 mm, 6-pin

Figure 3 illustrates the 6-pin PCB land pattern for the 5 x 7 mm Si590/591. Table 12 lists the values for the dimensions shown in the illustration.

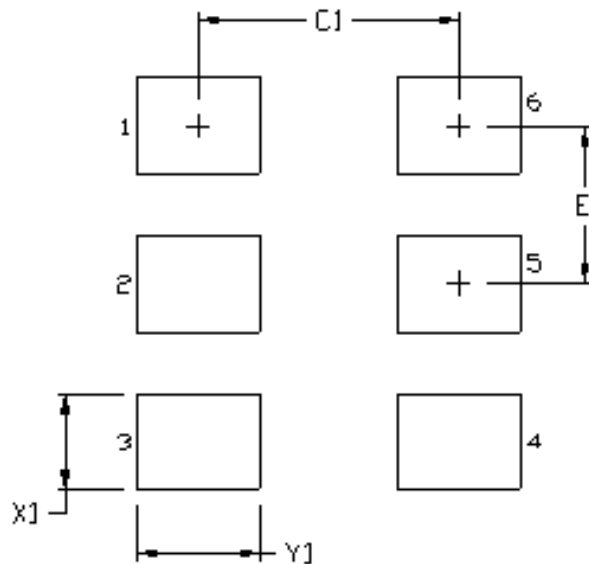


Figure 3. Si590/591 PCB Land Pattern

Table 12. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6. Package Outline Drawing: 3.2 x 5 mm, 6-pin

Figure illustrates the package details for the 3.2 x 5 mm Si590/591. Table 13 lists the values for the dimensions shown in the illustration.

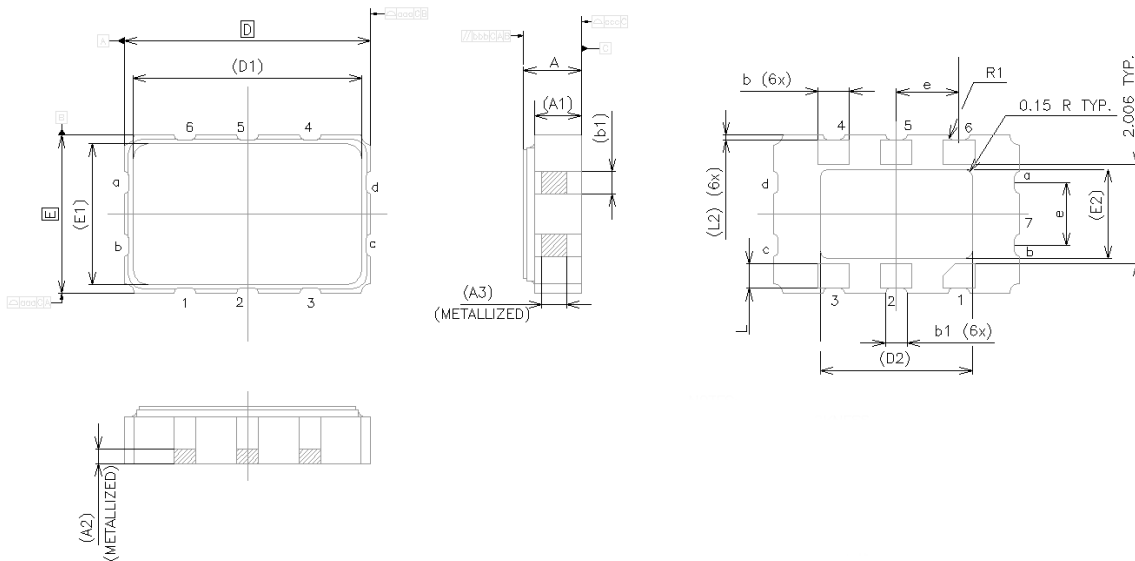


Figure 4. Si590/591 Outline Diagram

Table 13. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	1.02	1.17	1.32	E1	2.85 BSC		
A1	0.99	1.10	1.21	E2	1.91 BSC		
A2	0.5 BSC			L	0.35	0.45	0.55
A3	0.30 BSC			L2	0.05	0.10	0.15
b	0.54	0.64	0.74	R1	0.10 REF		
B1	0.35	0.45	0.55	aaa	0.15		
D	5.00 BSC			bbb	0.15		
D1	4.65 BSC			ccc	0.08		
D2	3.38 BSC			ddd	0.10		
e	1.27 BSC			eee	0.05		
E	3.20 BSC						

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7. PCB Land Pattern: 3.2 x 5 mm, 6-pin

Figure 5 illustrates the 6-pin PCB land pattern for the 3.2 x 5 mm Si590/591. Table 14 lists the values for the dimensions shown in the illustration.

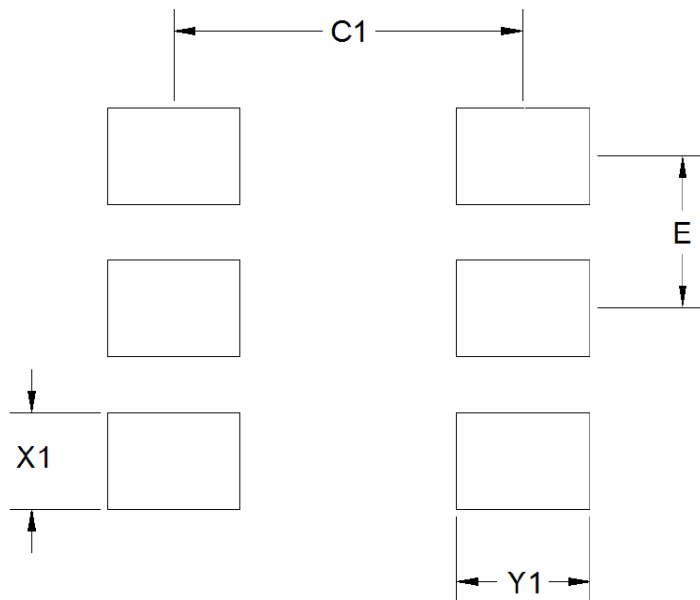


Figure 5. Si590/591 PCB Land Pattern

Table 14. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.91
E	1.27
X1	0.80
Y1	1.10

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8. Si590/Si591 Top Marking: 5 x 7 mm

Figure 6 illustrates the mark specification for the 5 x 7 mm Si590/Si591. Table 15 lists the line information.

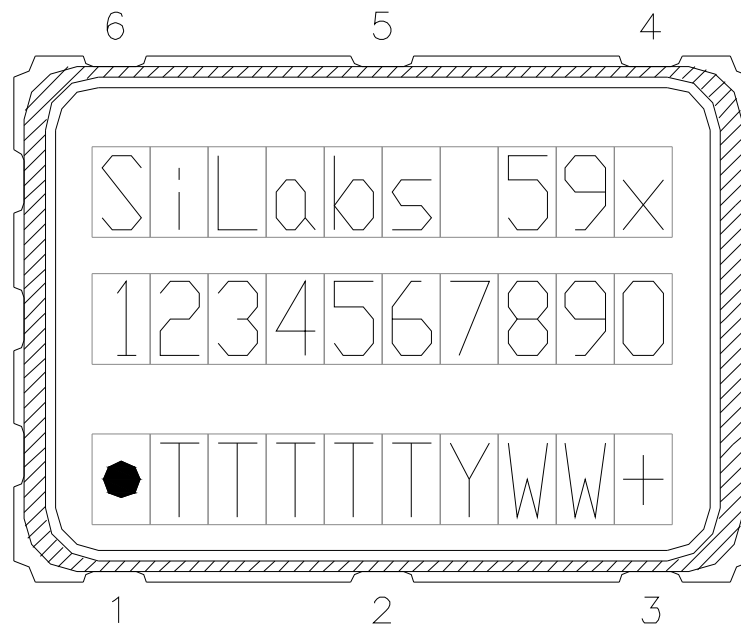


Figure 6. Top Mark Specification

Table 15. Si59x Top Mark Description

Line	Position	Description
1	1–10	“SiLabs”+ Part Family Number, 59x (First 3 characters in part number where x = 0 indicates a 590 device and x = 1 indicates a 591 device)
2	1–10	Si590, Si591: Option1 + Option2 + Freq(7) + Temp Si590/Si591 w/ 8-digit resolution: Option1 + Option2 + ConfigNum(6) + Temp
3	Trace Code	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2009 = 9)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

Si590/591

9. Si590/Si591 Top Marking: 3.2 x 5 mm

Figure 7 illustrates the mark specification for the 3.2 x 5 mm Si590/Si591. Table 16 lists the line information.

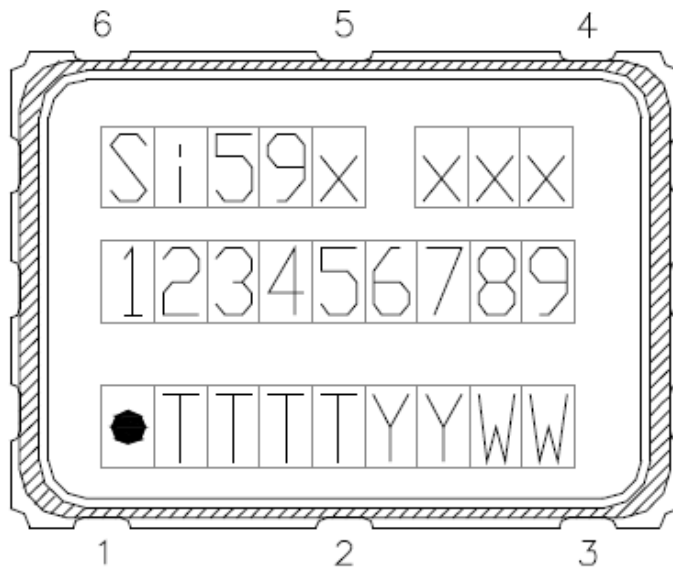


Figure 7. Top Mark Specification

Table 16. Si59x Top Mark Description

Line	Position	Description
1	1–5	“Si”+ Part Family Number, 59x (First 3 characters in part number where x = 0 indicates a 590 device and x = 1 indicates a 591 device)
	6–8	Crystal trace code (3 alphanumeric characters assigned by assembly site)
2	1–9	Si590, Si591: Option1 + Option2 + Freq(7) Si590/Si591 w/ 8-digit resolution: Option1 + Option2 + ConfigNum(6)
3	Trace Code	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of year), to be assigned by assembly site (ex: 20017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

REVISION HISTORY

Revision 1.2

June, 2018

- Changed “Trays” to “Coil Tape” in 3. "Ordering Information" on page 8.

Revision 1.1

December, 2017

- Added 3.2 x 5 mm package.

Revision 1.0

- Updated 2.5 V/3.3 V and 1.8 V CML output level specifications in Table 3 on page 4.
- Updated Si590/591 devices to support frequencies up to 810 MHz for LVPECL, LVDS, and CML outputs.
- Separated 1.8 V, 2.5 V/3.3 V supply voltage. specifications for CML output in Table 3 on page 4.
- Updated Note 1 of Table 4 on page 4 to refer to AN256.
- Updated Table 4 on page 4.
 - Updated phase jitter specification.
- Updated Table 6 on page 5 to include the "Moisture Sensitivity Level" and "Contact Pads" rows.
- Updated Figure 3 and Table 15 on page 13 to reflect specific marking information.
- Added Table 7, “Thermal Characteristics,” on page 5.
- Rearranged sections to conform to new quality standard.

Revision 0.4

- Added ± 7 ppm temperature stability ordering option in Table 4 on page 4 and Figure 1 on page 8.

Revision 0.3

- Updated Table 4 on page 4 by adding the 155.51 MHz “Phase Jitter (RMS) (LVPECL/LVDS/CML)” row.
- Updated and clarified Table 6 on page 5 to correct typos and include the “Moisture Sensitivity Level” and “Contact Pads” rows.
- Corrected BSC value in rows D and E in Table 11 on page 9.

Revision 0.25

- Total Stability Maximum changed to ± 30 in Table 2 on page 3.
- Total Stability Maximum changed to ± 30 in Figure 1 on page 8.



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

www.silabs.com/CBPro



Timing Portfolio
www.silabs.com/timing



SW/HW
www.silabs.com/CBPro



Quality
www.silabs.com/quality



Support and Community
community.silabs.com

Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Labs shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any Life Support System without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information

Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, Clockbuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, ISOModem®, Micrium, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri, Z-Wave, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>