

## 電圧制御水晶発振器 (VCXO) 10 ~ 810 MHz

### 特長

- 任意のレートでの 10 ~ 810 MHz 出力周波数で利用可能
- 優れたジッタ性能の第 3 世代 DSPLL<sup>®</sup>
- 内部固定基本モード水晶周波数により、高い信頼性と経年劣化の低減を実現
- CMOS、LVPECL、LVDS、および CML 出力で利用可能
- 3.3、2.5、および 1.8 V の電源オプション
- 業界標準の 5 x 7 および 3.2x5 mm パッケージ
- 鉛フリー対応 /RoHS 準拠
- -40 ~ +85 °C 動作温度

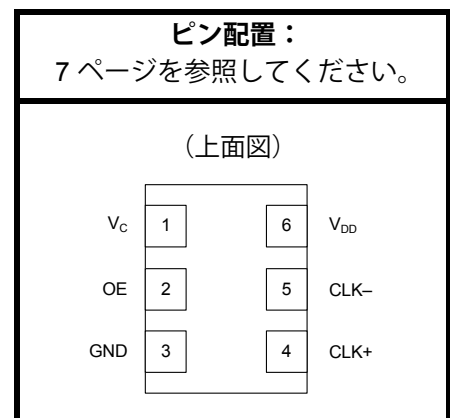
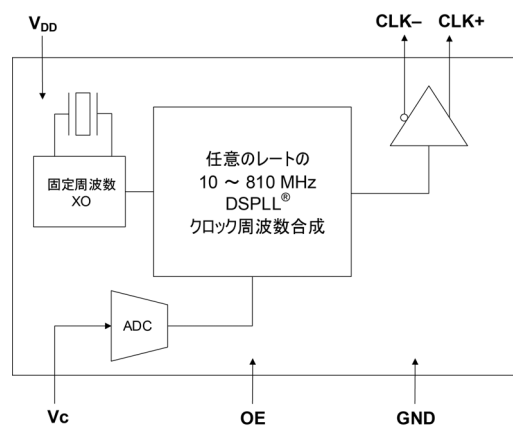
### アプリケーション

- SONET/SDH (OC-3/12/48)
- ネットワーキング
- SD/HD SDI/3G SDI ビデオ
- FTTx
- クロック・リカバリおよびジッタ・クリーンアップ PLL
- FPGA/ASIC クロック生成

### 説明

Si595 VCXO は、Silicon Laboratories の高度な DSPLL<sup>®</sup> 回路を採用し、高周波数での低ジッタ・クロックを実現します。Si595 は、任意のレートでの 10 ~ 810 MHz 出力周波数で利用可能です。出力周波数ごとに異なる水晶が必要な従来の VCXO とは異なり、Si595 は 1 つの固定水晶で広範囲の出力周波数を提供します。この IC ベースのアプローチにより、水晶共振器の高い周波数安定度と信頼性を実現します。さらに、DSPLL クロック合成は優れた電源ノイズ除去性能を提供するため、ノイズの多い環境で低ジッタ・クロック生成を簡素化できます。Si595 IC ベースの VCXO は、周波数、供給電圧、出力形式、チューニング・スロープ、絶対周波数可変範囲 (APR) など、幅広いユーザ設定に合わせて工場出荷時に構成できます。カスタム発振器に伴う長いリード・タイムを排除するために、固有の構成は工場出荷時にプログラムされています。

### 機能ブロック・ダイアグラム



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## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage <sup>1</sup>	$V_{DD}$	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	$I_{DD}$	Output enabled LVPECL	—	120	135	mA
		CML	—	110	120	
		LVDS	—	100	110	
		CMOS	—	90	100	
		Tristate mode	—	60	75	
Output Enable (OE) <sup>2</sup>		$V_{IH}$	$0.75 \times V_{DD}$	—	—	V
		$V_{IL}$	—	—	0.5	
Operating Temperature Range	$T_A$		−40	—	85	°C

**Notes:**

- Selectable parameter specified by part number. See 3. "Ordering Information" on page 9 for further details.
- OE pin includes an internal 17 k $\Omega$  pullup resistor to  $V_{DD}$  for output enable active high or a 17 k $\Omega$  pull-down resistor to GND for output enable active low. See 3. "Ordering Information" on page 9.

**Table 2.  $V_C$  Control Voltage Input**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope <sup>1,2,3</sup>	$K_V$	10 to 90% of $V_{DD}$	—	45	—	ppm/V
				95		
				125		
				185		
				380		
Control Voltage Linearity <sup>4</sup>	$L_{VC}$	BSL	−5	$\pm 1$	+5	%
		Incremental	−10	$\pm 5$	+10	
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
$V_C$ Input Impedance	$Z_{VC}$		500	—	—	k $\Omega$
$V_C$ Input Capacitance	$C_{VC}$		—	50	—	pF
Nominal Control Voltage	$V_{CNOM}$	@ $f_O$	—	$V_{DD}/2$	—	V
Control Voltage Tuning Range	$V_C$		0		$V_{DD}$	V

**Notes:**

- Positive slope; selectable option by part number. See 3. "Ordering Information" on page 9.
- For best jitter and phase noise performance, always choose the smallest  $K_V$  that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ( $K_V$ ), Stability, and Absolute Pull Range (APR)" for more information.
- $K_V$  variation is  $\pm 10\%$  of typical values.
- BSL determined from deviation from best straight line fit with  $V_C$  ranging from 10 to 90% of  $V_{DD}$ . Incremental slope determined with  $V_C$  ranging from 10 to 90% of  $V_{DD}$ .

Table 3. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency <sup>1,2,3</sup>	f <sub>O</sub>	LVDS/CML/LVPECL	10	—	810	MHz
		CMOS	10	—	160	
Temperature Stability <sup>1,4</sup>		T <sub>A</sub> = -40 to +85 °C	-20 -50	— —	+20 +50	ppm
Absolute Pull Range <sup>1,4</sup>	APR		±10	—	±370	ppm
Power up Time <sup>5</sup>	t <sub>OSC</sub>		—	—	10	ms

**Notes:**

- See Section 3. "Ordering Information" on page 9 for further details.
- Specified at time of order by part number.
- Nominal output frequency set by V<sub>CNOM</sub> = V<sub>DD</sub>/2.
- Selectable parameter specified by part number.
- Time from power up or tristate mode to f<sub>O</sub>.

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option <sup>1</sup>	V <sub>O</sub>	mid-level	V <sub>DD</sub> - 1.42	—	V <sub>DD</sub> - 1.25	V
	V <sub>OD</sub>	swing (diff)	1.1	—	1.9	V <sub>PP</sub>
	V <sub>SE</sub>	swing (single-ended)	0.55	—	0.95	V <sub>PP</sub>
LVDS Output Option <sup>2</sup>	V <sub>O</sub>	mid-level	1.125	1.20	1.275	V
	V <sub>OD</sub>	swing (diff)	0.5	0.7	0.9	V <sub>PP</sub>
CML Output Option <sup>2</sup>	V <sub>O</sub>	2.5/3.3 V option mid-level	—	V <sub>DD</sub> - 1.30	—	V
		1.8 V option mid-level	—	V <sub>DD</sub> - 0.36	—	
	V <sub>OD</sub>	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	V <sub>PP</sub>
		1.8 V option swing (diff)	0.35	0.425	0.50	
CMOS Output Option <sup>3</sup>	V <sub>OH</sub>		0.8 x V <sub>DD</sub>	—	V <sub>DD</sub>	V
	V <sub>OL</sub>		—	—	0.4	
Rise/Fall time (20/80%)	t <sub>R</sub> , t <sub>F</sub>	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C <sub>L</sub> = 15 pF	—	2	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V <sub>DD</sub> - 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: V <sub>DD</sub> /2	45	—	55	%

**Notes:**

- 50 Ω to V<sub>DD</sub> - 2.0 V.
- R<sub>term</sub> = 100 Ω (differential).
- C<sub>L</sub> = 15 pF. Sinking or sourcing 12 mA for V<sub>DD</sub> = 3.3 V, 6 mA for V<sub>DD</sub> = 2.5 V, 3 mA for V<sub>DD</sub> = 1.8 V.

Table 5. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS) <sup>1,2</sup> for $F_{OUT}$ of $50 \text{ MHz} \leq F_{OUT} \leq 810 \text{ MHz}$	$\phi_J$	$K_V = 45 \text{ ppm/V}$ 12 kHz to 20 MHz	—	0.5	—	ps
		$K_V = 95 \text{ ppm/V}$ 12 kHz to 20 MHz	—	0.5	—	
		$K_V = 125 \text{ ppm/V}$ 12 kHz to 20 MHz	—	0.5	—	
		$K_V = 185 \text{ ppm/V}$ 12 kHz to 20 MHz	—	0.5	—	
		$K_V = 380 \text{ ppm/V}$ 12 kHz to 20 MHz	—	0.7	—	

**Notes:**

1. Refer to AN256 for further information.
2. For best jitter and phase noise performance, always choose the smallest  $K_V$  that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ( $K_V$ ), Stability, and Absolute Pull Range (APR)" for more information.

Table 6. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	$J_{PER}$	RMS	—	3	—	ps
		Peak-to-Peak	—	35	—	

\*Note: Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

Table 7. CLK± Output Phase Noise (Typical)

Offset Frequency	74.25 MHz 185 ppm/V LVPECL	148.5 MHz 185 ppm/V LVPECL	155.52 MHz 95 ppm/V LVPECL	Units
100 Hz	-77	-68	-77	dBc/Hz
1 kHz	-101	-95	-101	
10 kHz	-121	-116	-119	
100 kHz	-134	-128	-127	
1 MHz	-149	-144	-144	
10 MHz	-151	-147	-147	
20 MHz	-150	-148	-148	

**Table 8. Environmental Compliance and Package Information**

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Contact Pads	Gold over Nickel

**Table 9. Thermal Characteristics**

(Typical values  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5x7mm, Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still Air	—	84.6	—	$^\circ\text{C/W}$
5x7mm, Thermal Resistance Junction to Case	$\theta_{JC}$	Still Air	—	38.8	—	$^\circ\text{C/W}$
3.2x5mm, Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still Air	—	31.1	—	$^\circ\text{C/W}$
3.2x5mm, Thermal Resistance Junction to Case	$\theta_{JC}$	Still Air	—	13.3	—	$^\circ\text{C/W}$
Ambient Temperature	$T_A$		-40	—	85	$^\circ\text{C}$
Junction Temperature	$T_J$		—	—	125	$^\circ\text{C}$

**Table 10. Absolute Maximum Ratings<sup>1</sup>**

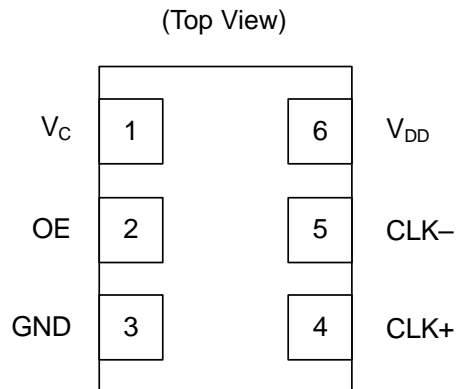
Parameter	Symbol	Rating	Units
Maximum Operating Temperature	$T_{AMAX}$	85	$^\circ\text{C}$
Supply Voltage	$V_{DD}$	-0.5 to +3.8	V
Input Voltage	$V_I$	-0.5 to $V_{DD} + 0.3$	
Storage Temperature	$T_S$	-55 to +125	$^\circ\text{C}$
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	V
Soldering Temperature (Pb-free profile) <sup>2</sup>	$T_{PEAK}$	260	$^\circ\text{C}$

Table 10. Absolute Maximum Ratings<sup>1</sup>

Parameter	Symbol	Rating	Units
Soldering Temperature Time @ T <sub>PEAK</sub> (Pb-free profile) <sup>2</sup>	t <sub>p</sub>	20–40	seconds
<b>Notes:</b> <ol style="list-style-type: none"><li>1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.</li><li>2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download from <a href="http://www.silabs.com/VCXO">www.silabs.com/VCXO</a> for further information, including soldering profiles.</li></ol>			

# Si595

## 2. Pin Descriptions



**Table 11. Si595 Pin Descriptions**

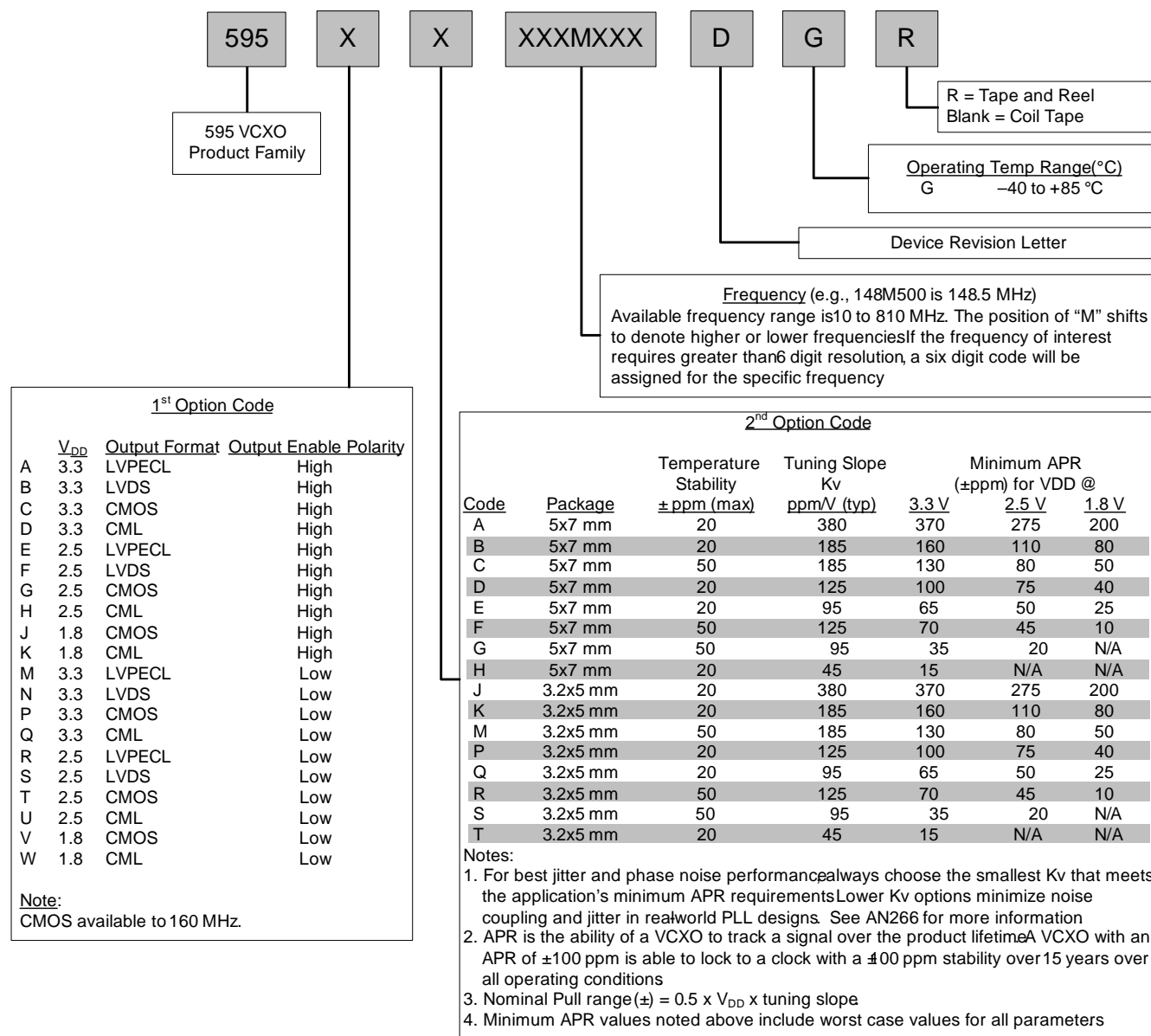
Pin	Name	Type	Function
1	V <sub>C</sub>	Analog Input	Control Voltage
2	OE*	Input	Output Enable
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK- (N/C for CMOS)	Output	Complementary Output (N/C for CMOS, do not make external connection)
6	V <sub>DD</sub>	Power	Power Supply Voltage

**\*Note:** OE pin includes a 17 kΩ resistor to V<sub>DD</sub> for OE active high option or 17 kΩ to GND for OE active low option. See 3. "Ordering Information" on page 9.



### 3. Ordering Information

The Si595 supports a variety of options including frequency, temperature stability, tuning slope, output format, and  $V_{DD}$ . Specific device configurations are programmed into the Si595 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. To access this tool refer to [www.silabs.com/oscillators](http://www.silabs.com/oscillators) and click "Customize" in the product table. The Si595 VCXO series is supplied in industry-standard, RoHS compliant, lead-free, 6-pad, 5 x 7 mm and 3.2 x 5 mm package. Tape and reel packaging is an ordering option.

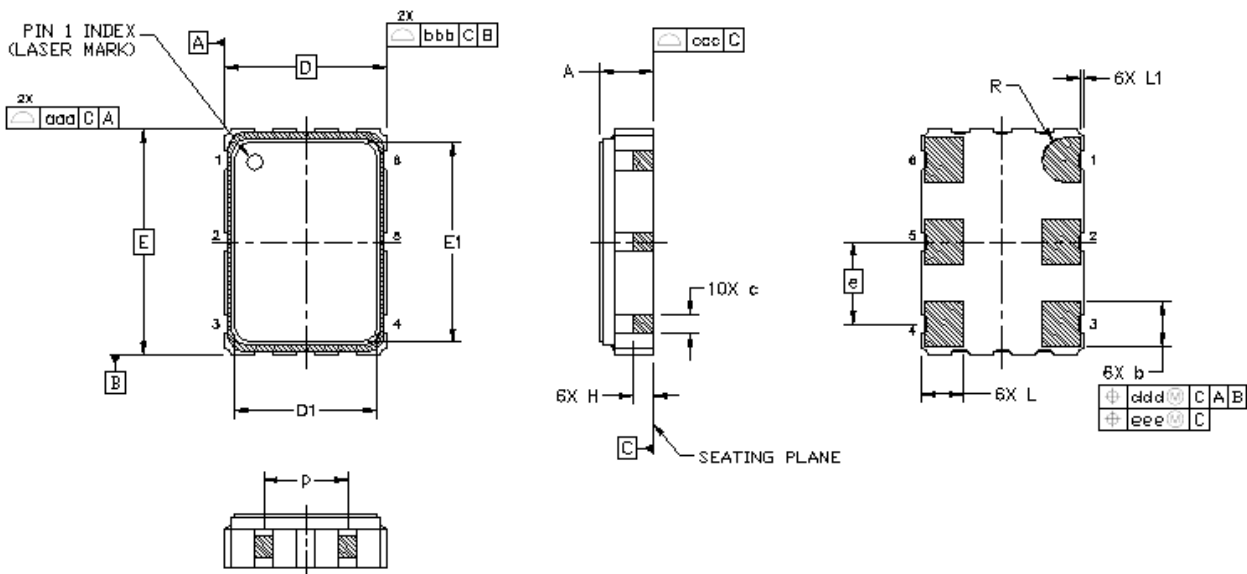


Example Part Number. 595AE148M500DGR is a 5 x 7 mm VCXO in a 6 pad package. The nominal frequency is 148.5 MHz, with a 3.3 V supply, LVPECL output, and Output Enable active high polarity. Temperature stability is specified as  $\pm 20$  ppm and the tuning slope is 95 ppm/V. The part is specified for a -40 to +85 C° ambient temperature range operation and is shipped in tape and reel format.

Figure 1. Part Number Convention

## 4. Package Outline Diagram: 5 x 7 mm, 6-pin

Figure 2 illustrates the package details for the 5 x 7 mm Si595. Table 12 lists the values for the dimensions shown in the illustration.



**Figure 2. Si595 Outline Diagram**

**Table 12. Package Diagram Dimensions (mm)**

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D	5.00 BSC		
D1	4.30	4.40	4.50
e	2.54 BSC.		
E	7.00 BSC.		
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	0.05	0.10	0.15
p	1.80	—	2.60
R	0.70 REF		
aaa	0.15		
bbb	0.15		
ccc	0.10		
ddd	0.10		
eee	0.05		
<b>Note:</b>	<ol style="list-style-type: none"> <li>All dimensions shown are in millimeters (mm) unless otherwise noted.</li> <li>Dimensioning and Tolerancing per ANSI Y14.5M-1994</li> </ol>		

## 5. PCB Land Pattern: 5 x 7 mm, 6-pin

Figure 3 illustrates the 6-pin PCB land pattern for the 5 x 7 mm Si595. Table 13 lists the values for the dimensions shown in the illustration.

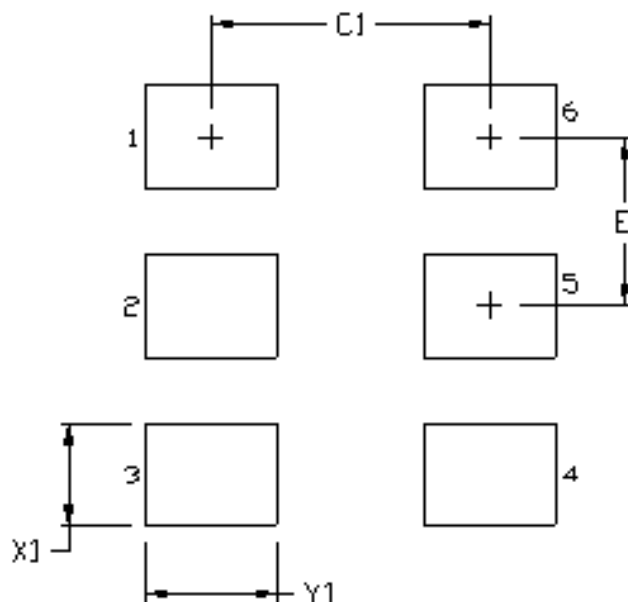


Figure 3. Si595 PCB Land Pattern

Table 13. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

**Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 6. Package Outline Drawing: 3.2 x 5 mm, 6-pin

Figure 4 illustrates the package details for the 3.2 x 5 mm Si595. Table 14 lists the values for the dimensions shown in the illustration.

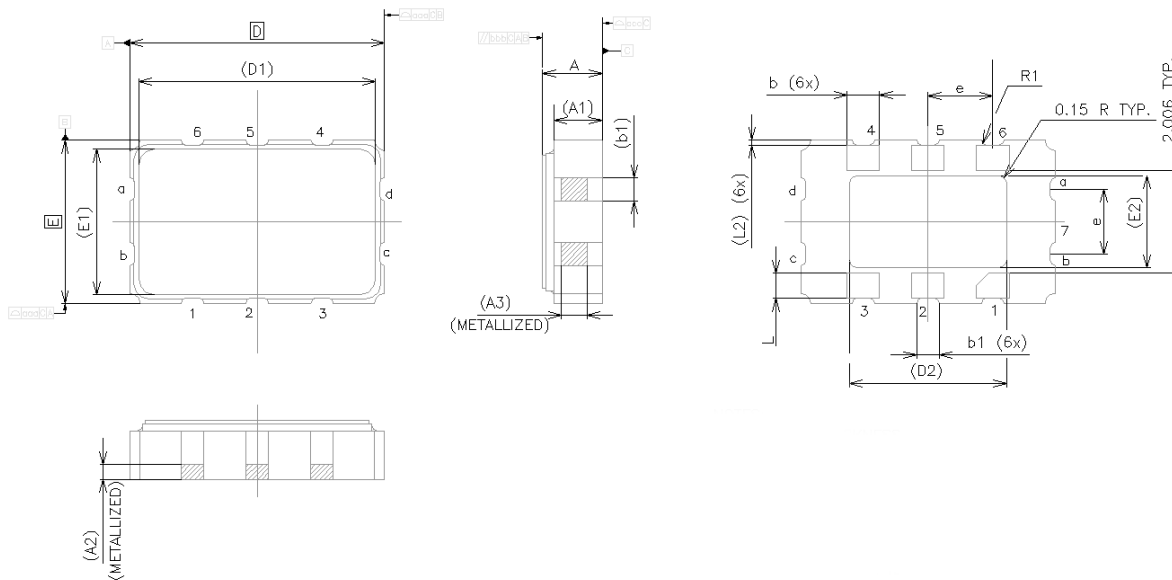


Figure 4. Si595 Outline Diagram

Table 14. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	1.02	1.17	1.32	E1	2.85 BSC		
A1	0.99	1.10	1.21	E2	1.91 BSC		
A2	0.5 BSC			L	0.35	0.45	0.55
A3	0.30 BSC			L2	0.05	0.10	0.15
b	0.54	0.64	0.74	R1	0.10 REF		
B1	0.35	0.45	0.55	aaa	0.15		
D	5.00 BSC			bbb	0.15		
D1	4.65 BSC			ccc	0.08		
D2	3.38 BSC			ddd	0.10		
e	1.27 BSC			eee	0.05		
E	3.20 BSC						

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

## 7. PCB Land Pattern: 3.2 x 5 mm, 6-pin

Figure 5 illustrates the 6-pin PCB land pattern for the 3.2 x 5 mm Si595. Table 15 lists the values for the dimensions shown in the illustration.

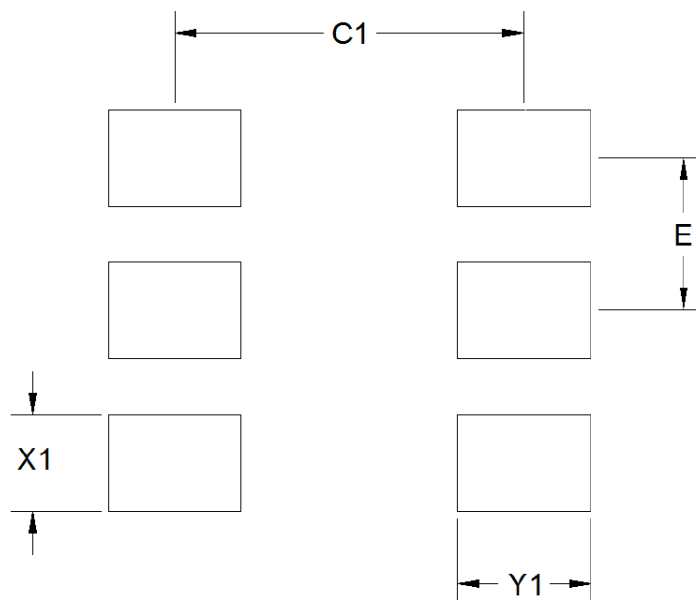


Figure 5. Si595 PCB Land Pattern

Table 15. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.91
E	1.27
X1	0.80
Y1	1.10

**Notes:**

**General**

- All dimensions shown are in millimeters (mm) unless otherwise noted.
- Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- This Land Pattern Design is based on the IPC-7351 guidelines.
- All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Solder Mask Design**

- All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu\text{m}$  minimum, all the way around the pad.

**Stencil Design**

- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- The stencil thickness should be 0.125 mm (5 mils).
- The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

- A No-Clean, Type-3 solder paste is recommended.
- The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

# Si595

## 8. Si5xx Mark Specification: 5 x 7 mm

5 x 7 mm Si595. Table 16 lists the line information.

Figure 6 illustrates the mark specification for the

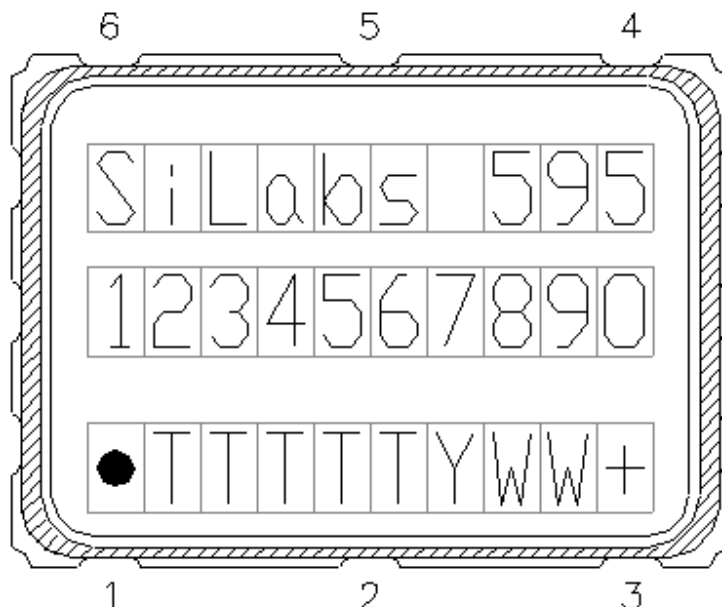


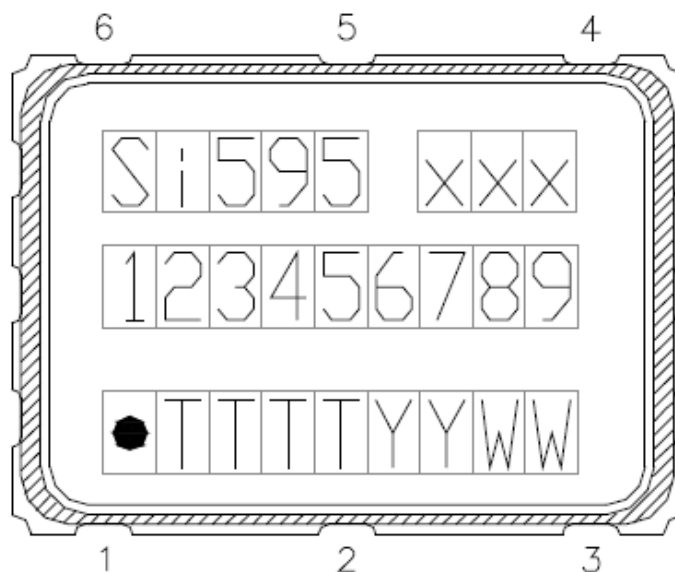
Figure 6. Mark Specification

Table 16. Si595 Top Mark Description

Line	Position	Description
1	1–10	“SiLabs”+ Part Family Number, 595 (First 3 characters in part number)
2	1–10	Si595: Option1+Option2+Freq(7)+Temp Si595 w/ 8-digit resolution: Option1+Option2+ConfigNum(6)+Temp
3	<b>Trace Code</b>	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2009 = 9)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

## 9. Si5xx Mark Specification: 3.2 x 5 mm

Figure 7 illustrates the mark specification for the 3.2 x 5 mm Si595. Table 17 lists the line information.



**Figure 7. Mark Specification**

**Table 17. Si595 Top Mark Description**

Line	Position	Description
1	1–5	“Si”+ Part Family Number, 595 (First 3 characters in part number)
	6–8	Crystal trace code (3 alphanumeric characters assigned by assembly site)
2	1–9	Si595: Option1+Option2+Freq(7) Si595 w/ 8-digit resolution: Option1+Option2+ConfigNum(6)
3	<b>Trace Code</b>	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6–7	Year (last two digits of year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

## REVISION HISTORY

### Revision 1.4

June, 2018

- Changed “Trays” to “Coil Tape” in 3. "Ordering Information" on page 9.

### Revision 1.3

December, 2017

- Added 3.2 x 5 mm package.

### Revision 1.2

- Added Table 9, “Thermal Characteristics,” on page 6.

### Revision 1.1

- Swapped D and E values in Table 12 on page 10.

### Revision 1.0

- Updated 2.5 V/3.3 V and 1.8 V CML output level specifications in Table 4 on page 4.
- Updated Si595 device to support frequencies up to 810 MHz for LVPECL, LVDS, and CML outputs.
- Separated 1.8 V, 2.5 V/3.3 V supply voltage. specifications for CML output in Table 3 on page 5.
- Updated Note 1 of Table 5 on page 5 to refer to AN256.
- Updated Table 8 on page 6 to include the "Moisture Sensitivity Level" and "Contact Pads" rows.
- Updated Figure 3 and Table 16 on page 14 to reflect specific marking information.

### Revision 0.2

- Updated Table 5, “CLK $\pm$  Output Phase Jitter,” on page 5.
  - Updated typical phase jitter from 0.6 to 0.7 ps for kV = 380 ppm/V.





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