デュアル周波数電圧制御水晶発振器（VCXO）
10 ～ 810 MHz

特長

- 任意のレートの 10 ～ 810 MHz 出力周波数で利用可能
- 選択可能な 2 つの出力周波数
- 優れたジッタ性能の第 3 世代 DSPLL®
- 内部固定基本モード水晶周波数により、高い信頼性と経年劣化の低減を実現
- CMOS、LVPECL、LVDS、および CML 出力で利用可能
- 3.3、2.5、および 1.8 V の電源オプション
- 業界標準の 5 x 7 および 3.2x5 mm パッケージ
- 鉛フリー対応 /RoHS 準拠
- –40 ～ +85 ºC 動作温度

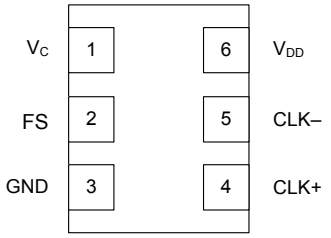
アプリケーション

- SONET/SDH （OC-3/12/48）
- ネットワーキング
- SD/HD SDI/3G SDI ビデオ
- FTTx
- クロック・リカバリおよびジッタ・クリーンアップ PLL
- FPGA/ASIC クロック生成

注文情報：
8 ページを参照してください。

ピン配置：
7 ページを参照してください。

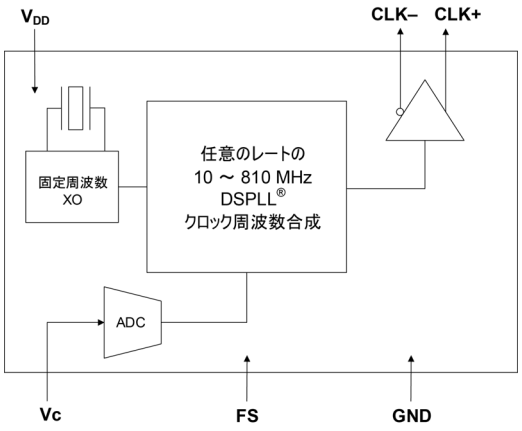
（上面図）



説明

Si596 デュアル周波数 VCXO は、Silicon Laboratories の高度な DSPLL® 回路を採用し、高周波数での低ジッタ・クロックを実現します。Si596 は、任意のレートの 10 ～ 810 MHz 出力周波数で利用可能です。出力周波数ごとに異なる水晶が必要な従来の VCXO とは異なり、Si596 は 1 つの固定水晶で広範囲の出力周波数を提供します。この IC ベースのアプローチにより、水晶共振器の高い周波数安定度と信頼性を実現します。さらに、DSPLL クロック合成は優れた電源ノイズ除去性能を提供するため、ノイズの多い環境で低ジッタ・クロック生成を簡素化できます。Si596 IC ベースの VCXO は、周波数、供給電圧、出力形式、チューニング・スロープ、絶対周波数可変範囲（APR）など、幅広いユーザ設定に合わせて工場出荷時に構成できます。カスタム発振器に伴う長いリード・タイムを排除するために、固有の構成は工場出荷時にプログラムされています。

機能ブロック・ダイアグラム



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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage[1]	V_{DD}	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	
		1.8 V option	1.71	1.8	1.89	
Supply Current	I_{DD}	LVPECL CML LVDS CMOS	— — — —	120 110 100 90	135 120 110 100	mA
Frequency Select (FS)[2]		V_{IH}	0.75 x V_{DD}	—	—	V
		V_{IL}	—	—	0.5	
Operating Temperature Range	T_A		–40	—	85	°C

Notes:
1. Selectable parameter specified by part number. See 3. "Ordering Information" on page 9 for further details.
2. FS pin includes an internal 17 kΩ pullup resistor to V_{DD}. When the FS is left floating, the pullup causes FS = 1 = second frequency selected.

Table 2. V_C Control Voltage Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope[1,2,3]	K_V	10 to 90% of V_{DD}	—	45 95 125 185 380	—	ppm/V
Control Voltage Linearity[4]	L_{VC}	BSL	–5	±1	+5	%
		Incremental	–10	±5	+10	
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
V_C Input Impedance	Z_{VC}		500	—	—	kΩ
V_C Input Capacitance	C_{VC}		—	50	—	pF
Nominal Control Voltage	V_{CNOM}	@ f_O	—	$V_{DD}/2$	—	V
Control Voltage Tuning Range	V_C		0		V_{DD}	V

Notes:
1. Positive slope; selectable option by part number. See 3. "Ordering Information" on page 9.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.
3. K_V variation is ±10% of typical values.
4. BSL determined from deviation from best straight line fit with V_C ranging from 10 to 90% of V_{DD}. Incremental slope determined with V_C ranging from 10 to 90% of V_{DD}.

Table 3. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency[1,2,3]	f_O	LVDS/CML/LVPECL	10	—	810	MHz
		CMOS	10	—	160	
Temperature Stability[1,4]		T_A = –40 to +85 ºC	–20 –50	— —	+20 +50	ppm
Absolute Pull Range[1,4]	APR		±10	—	±370	ppm
Power up Time[5]	t_{OSC}		—	—	10	ms
Settling Time After FS Change	T_{FRQ}		—	—	10	ms

Notes:
1. See Section 3. "Ordering Information" on page 9 for further details.
2. Specified at time of order by part number.
3. Nominal output frequency set by $V_{CNOM} = V_{DD}/2$.
4. Selectable parameter specified by part number.
5. Time from power up or tristate mode to f_O.

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option[1]	V_O	mid-level	V_{DD} – 1.42	—	V_{DD} – 1.25	V
	V_{OD}	swing (diff)	1.1	—	1.9	V_{PP}
	V_{SE}	swing (single-ended)	0.55	—	0.95	V_{PP}
LVDS Output Option[2]	V_O	mid-level	1.125	1.20	1.275	V
	V_{OD}	swing (diff)	0.5	0.7	0.9	V_{PP}
CML Output Option[2]	V_O	2.5/3.3 V option mid-level	—	V_{DD} – 1.30	—	V
		1.8 V option mid-level	—	V_{DD} – 0.36	—	
	V_{OD}	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	V_{PP}
		1.8 V option swing (diff)	0.35	0.425	0.50	
CMOS Output Option[3]	V_{OH}		0.8 x V_{DD}	—	V_{DD}	V
	V_{OL}		—	—	0.4	
Rise/Fall time (20/80%)	t_R, t_F	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with C_L = 15 pF	—	2	—	ns
Symmetry (duty cycle)	SYM	LVPECL: V_{DD} – 1.3 V (diff) LVDS: 1.25 V (diff) CMOS: $V_{DD}/2$	45	—	55	%

Notes:
1. 50 Ω to V_{DD} – 2.0 V.
2. R_{term} = 100 Ω (differential).
3. C_L = 15 pF. Sinking or sourcing 12 mA for V_{DD} = 3.3 V, 6 mA for V_{DD} = 2.5 V, 3 mA for V_{DD} = 1.8 V.

Table 5. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS)[1,2] for F_{OUT} of 50 MHz ≤ F_{OUT} 810 MHz	ϕ_J	Kv = 45 ppm/V 12 kHz to 20 MHz	—	0.5	—	ps
		Kv = 95 ppm/V 12 kHz to 20 MHz	—	0.5	—	
		Kv = 125 ppm/V 12 kHz to 20 MHz	—	0.5	—	
		Kv = 185 ppm/V 12 kHz to 20 MHz	—	0.5	—	
		Kv = 380 ppm/V 12 kHz to 20 MHz	—	0.7	—	

Notes:
1. Refer to AN256 for further information.
2. For best jitter and phase noise performance, always choose the smallest K_V that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K_V), Stability, and Absolute Pull Range (APR)" for more information.

Table 6. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J_{PER}	RMS	—	3	—	ps
		Peak-to-Peak	—	35	—	

***Note:** Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

Table 7. CLK± Output Phase Noise (Typical)

Offset Frequency	74.25 MHz 185 ppm/V LVPECL	148.5 MHz 185 ppm/V LVPECL	155.52 MHz 95 ppm/V LVPECL	Units
100 Hz	–77	–68	–77	
1 kHz	–101	–95	–101	
10 kHz	–121	–116	–119	
100 kHz	–134	–128	–127	dBc/Hz
1 MHz	–149	–144	–144	
10 MHz	–151	–147	–147	
20 MHz	–150	–148	–148	

Table 8. Environmental Compliance and Package Information

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solder Heat	MIL-STD-883, Method 2036
Contact Pads	Gold over Nickel

Table 9. Thermal Characteristics

(Typical values TA = 25 ºC, V_{DD} = 3.3 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
5x7mm, Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	84.6	—	°C/W
5x7mm, Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	38.8	—	°C/W
3.2x5mm, Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	31.1	—	°C/W
3.2x5mm, Thermal Resistance Junction to Case	θ_{JC}	Still Air	—	13.3	—	°C/W
Ambient Temperature	T_A		–40	—	85	°C
Junction Temperature	T_J		—	—	125	°C

Table 10. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T_{AMAX}	85	ºC
Supply Voltage	V_{DD}	–0.5 to +3.8	V
Input Voltage	V_I	–0.5 to V_{DD} + 0.3	
Storage Temperature	T_S	–55 to +125	ºC
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2500	V
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}	260	ºC

Table 10. Absolute Maximum Ratings[1]

Parameter	Symbol	Rating	Units
Soldering Temperature Time @ T_{PEAK} (Pb-free profile)[2]	t_P	20–40	seconds

Notes:
1. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
2. The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download from www.silabs.com/VCXO for further information, including soldering profiles.

2. Pin Descriptions

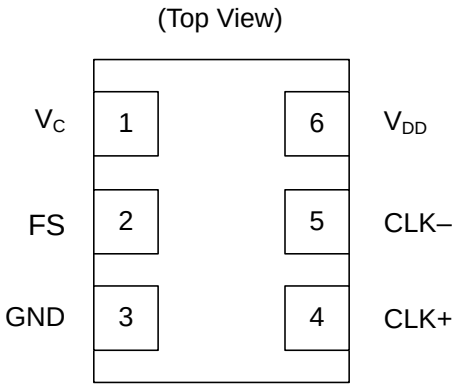


Table 11. Si596 Pin Descriptions

Pin	Name	Type	Function
1	V_C	Analog Input	Control Voltage
2	FS*	Input	Frequency Select: 0 = first frequency selected 1 = second frequency selected
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK– (N/C for CMOS)	Output	Complementary Output (N/C for CMOS, do not make external connection)
6	V_{DD}	Power	Power Supply Voltage
***Note:** FS pin includes a 17 kΩ resistor to V_{DD}. When the FS is left floating, the pullup causes FS = 1 = second frequency selected. See 3. "Ordering Information" on page 9 for details on frequency select ordering options.			

3. Ordering Information

The Si596 supports a variety of options including frequency, temperature stability, tuning slope, output format, and V_{DD}. Specific device configurations are programmed into the Si596 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. To access this tool refer to www.silabs.com/oscillators and click "Customize" in the product table. The Si596 VCXO series is supplied in industry-standard, RoHS compliant, lead-free, 6-pad, 5 x 7 mm and 3.2 x 5 mm packages. Tape and reel packaging is an ordering option.

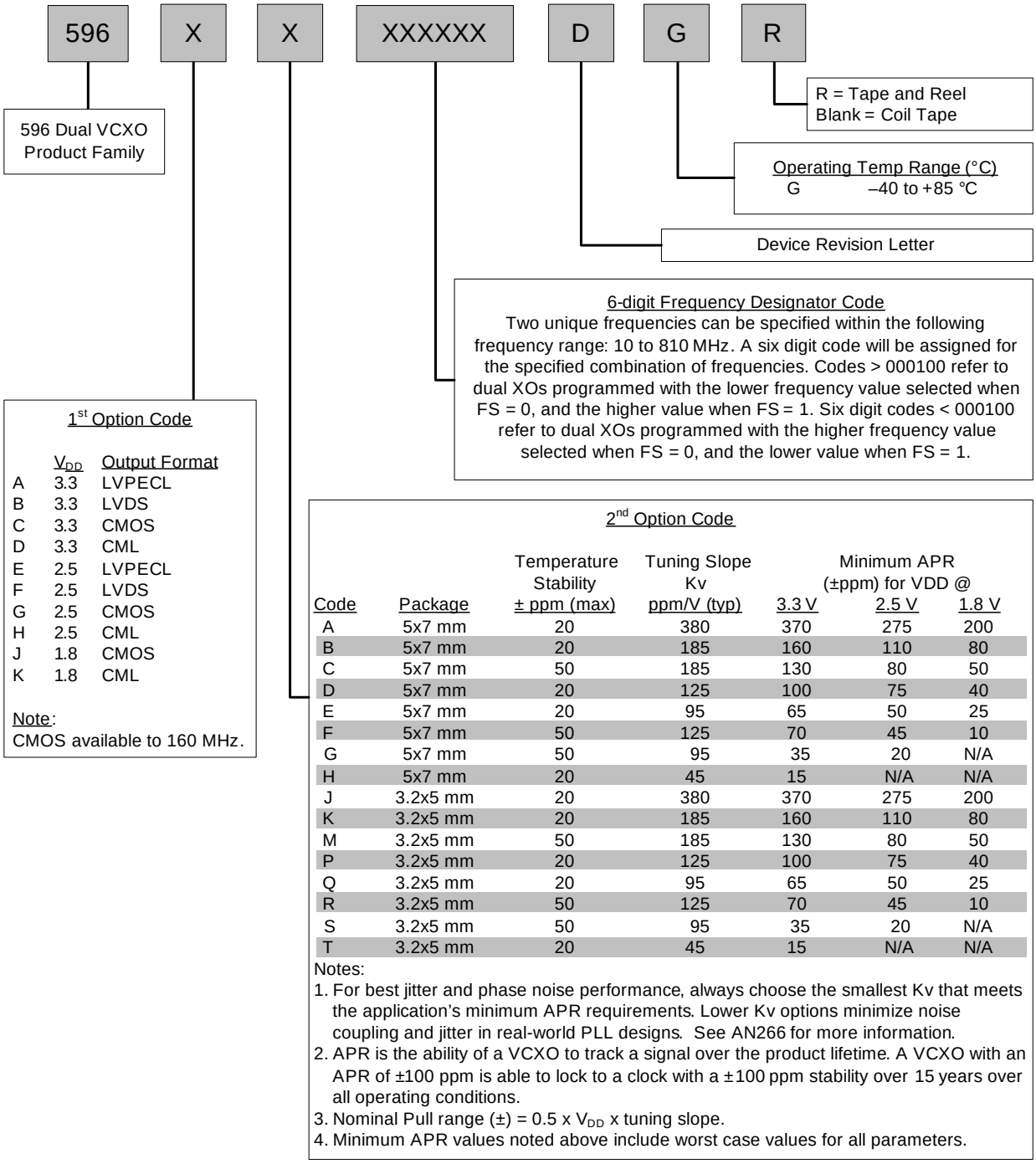


Figure 1. Part Number Convention

4. Package Outline Diagram: 5 x 7 mm, 6-pin

Figure 2 illustrates the package details for the 5 x 7 mm Si596. Table 12 lists the values for the dimensions shown in the illustration.

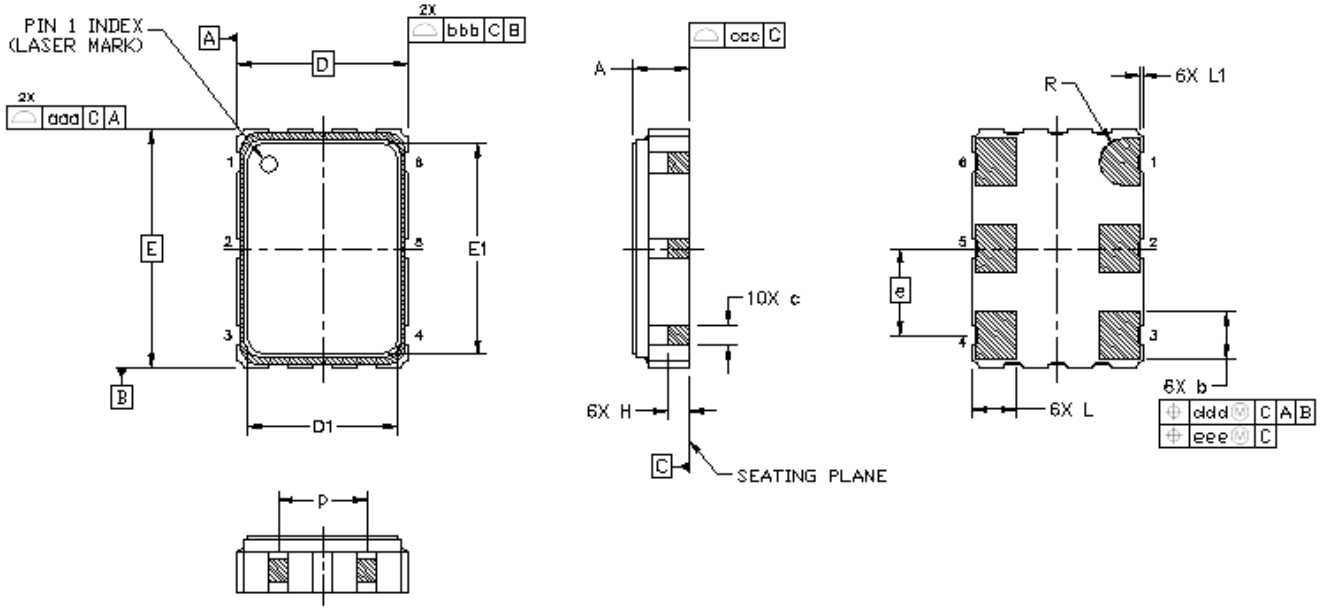


Figure 2. Si596 Outline Diagram

Table 12. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
c	0.50	0.60	0.70
D		5.00 BSC	
D1	4.30	4.40	4.50
e		2.54 BSC.	
E		7.00 BSC.	
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	0.05	0.10	0.15
p	1.80	—	2.60
R		0.70 REF	
aaa		0.15	
bbb		0.15	
ccc		0.10	
ddd		0.10	
eee		0.05	

5. PCB Land Pattern: 5 x 7 mm, 6-pin

Figure 3 illustrates the 6-pin PCB land pattern for the 5 x 7 mm Si596. Table 13 lists the values for the dimensions shown in the illustration.

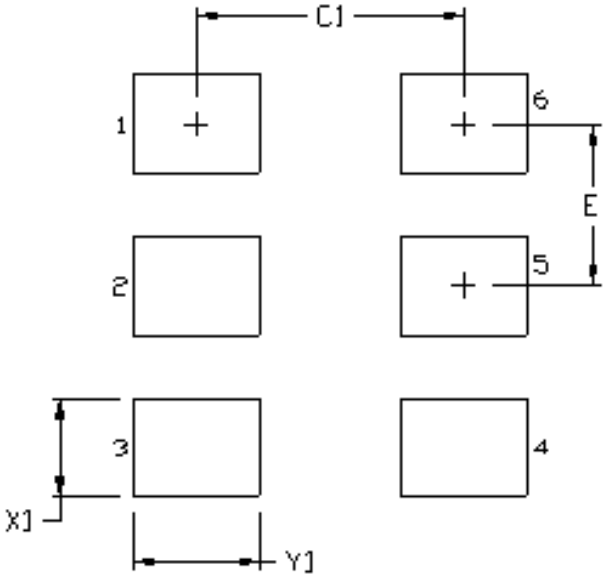


Figure 3. Si596 PCB Land Pattern

Table 13. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	4.20
E	2.54
X1	1.55
Y1	1.95

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6. Package Outline Drawing: 3.2 x 5 mm, 6-pin

Figure 4 illustrates the package details for the 3.2 x 5 mm Si596. Table 14 lists the values for the dimensions shown in the illustration.

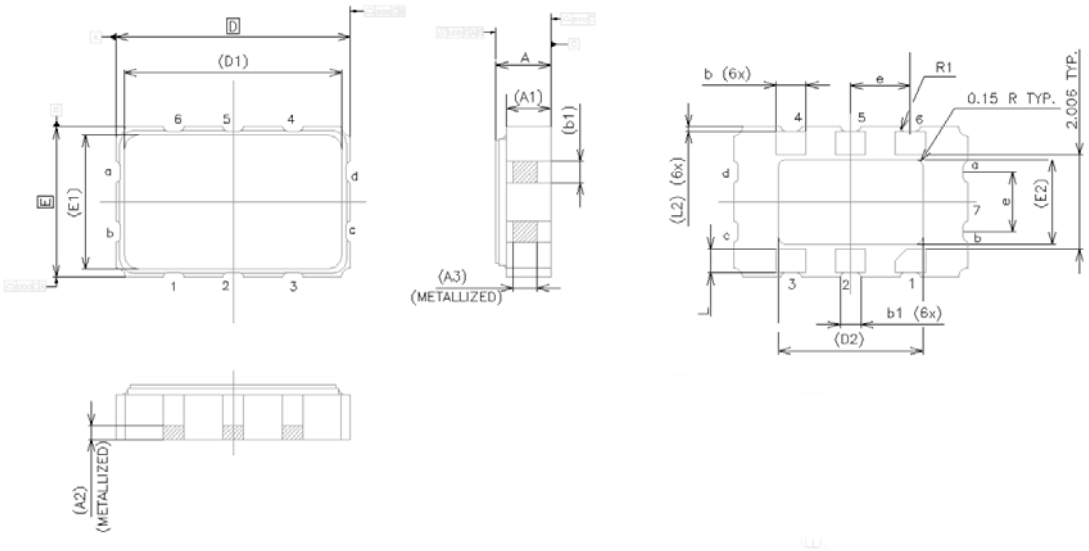


Figure 4. Si596 Outline Diagram

Table 14. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max		Dimension	Min	Nom	Max
A	1.02	1.17	1.32		E1	2.85 BSC		
A1	0.99	1.10	1.21		E2	1.91 BSC		
A2	0.5 BSC				L	0.35	0.45	0.55
A3	0.30 BSC				L2	0.05	0.10	0.15
b	0.54	0.64	0.74		R1	0.10 REF		
B1	0.35	0.45	0.55		aaa	0.15		
D	5.00 BSC				bbb	0.15		
D1	4.65 BSC				ccc	0.08		
D2	3.38 BSC				ddd	0.10		
e	1.27 BSC				eee	0.05		
E	3.20 BSC							

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7. PCB Land Pattern: 3.2 x 5 mm, 6-pin

Figure 5 illustrates the 6-pin PCB land pattern for the 3.2 x 5 mm Si596. Table 15 lists the values for the dimensions shown in the illustration.

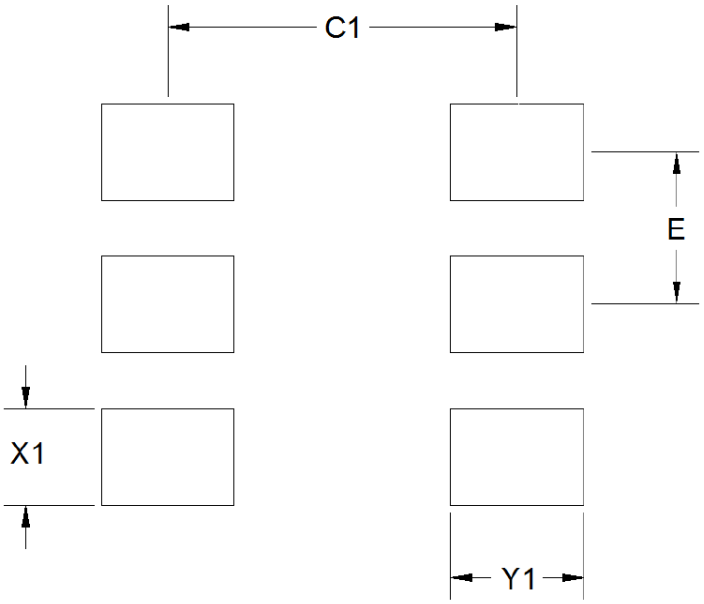


Figure 5. Si596 PCB Land Pattern

Table 15. PCB Land Pattern Dimensions (mm)

Dimension	(mm)
C1	2.91
E	1.27
X1	0.80
Y1	1.10

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8. Si596 Top Marking: 5x7 mm

Figure 6 illustrates the mark specification for the 5x7 Si596. Table 16 lists the line information.

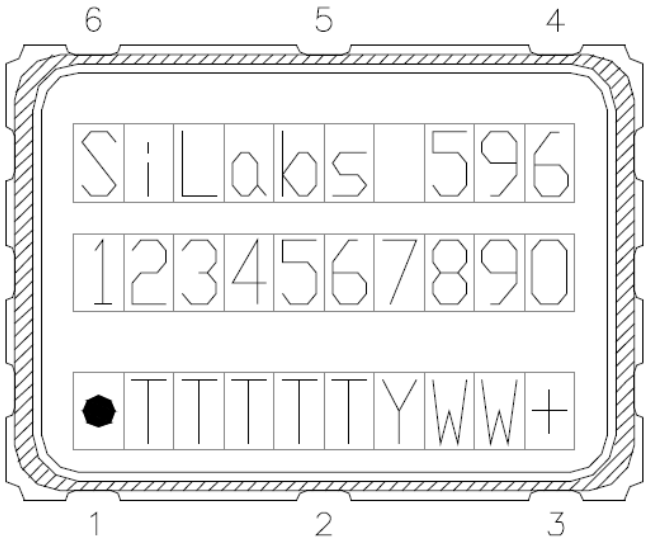


Figure 6. Mark Specification

Table 16. Si596 Top Mark Description

Line	Position	Description
1	1–10	“SiLabs”+ Part Family Number, 596 (First 3 characters in part number)
2	1–10	Si596: Option1+Option2+Freq(6)+Temp
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2009 = 9)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

9. Si596 Top Marking: 3.2x5 mm

Figure 7 illustrates the mark specification for the 3.2x5 mm Si596. Table 17 lists the line information.

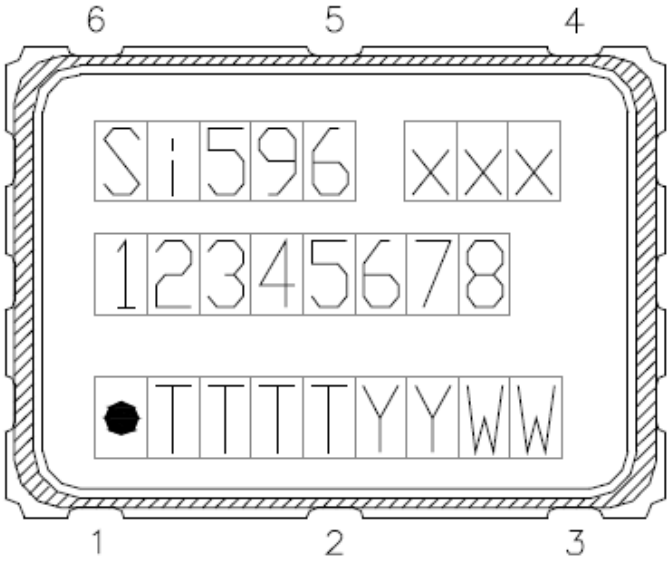


Figure 7. Mark Specification

Table 17. Si596 Top Mark Description

Line	Position	Description
1	1–5	“Si”+ Part Family Number, 596 (First 3 characters in part number)
	6-8	Crystal trace code (3 alphanumeric characters assigned by assembly site)
2	1–8	Si596: Option1+Option2+Freq(6)
3	**Trace Code**	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–5	Tiny Trace Code (3 alphanumeric characters per assembly release instructions)
	Position 6-7	Year (last two digits of year), to be assigned by assembly site (ex: 2017 = 17)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site

Revision History

Revision 1.2

June, 2018

- Changed “Trays” to “Coil Tape” in 3. "Ordering Information" on page 9.

Revision 1.1

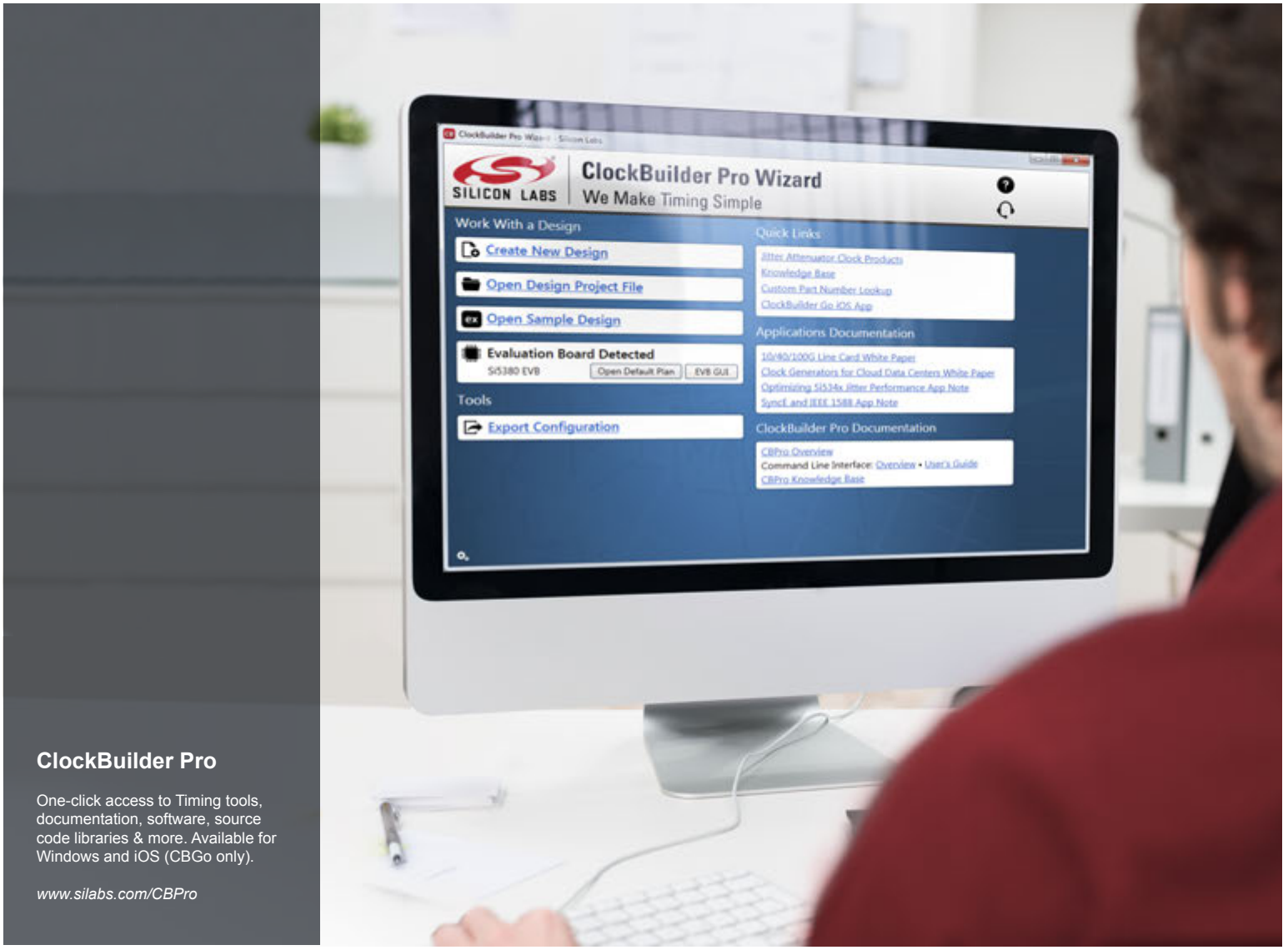
December, 2017

- Added 3.2 x 5 mm package.

Revision 1.0

June, 2016

- Initial release.



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