

# Si721x 磁場出力ホール効果磁気式位置センサー・データ・シート

Silicon Labs が提供するホール効果センサーの Si7211/2/3/4/5/6/7 ファミリーには、チョップ安定型ホール素子と、低ノイズ・アナログ・アンプ、13 ビット AD コンバータが組み込まれています。A/D 変換後、アナログで磁場データを利用できます。PWM、または SENT 形式（部品番号に応じて）で使用できます。Silicon Labs の実績ある CMOS 設計技術を活かした Si721x ファミリーにはデジタル信号処理が組み込まれ、温度およびオフセット・ドリフトを正確に補正します。

Si721x ファミリーは、既存のホール効果センサーと比較して業界最先端の感度を備えてノイズを抑え、より大きなエア・ギャップでより小型の磁石を使用できます。

最も単純な事例として、Si721x デバイスは、電源、グラウンド、単一出力ピンからなる 3 ピン SOT23 または TO92 パッケージで提供され、出力ピンの信号はアナログ、PWM、または SENT 形式の磁場に対応します。

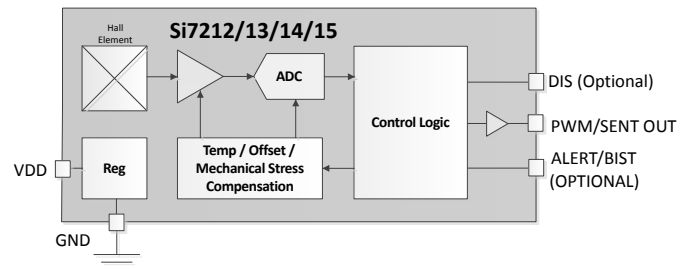
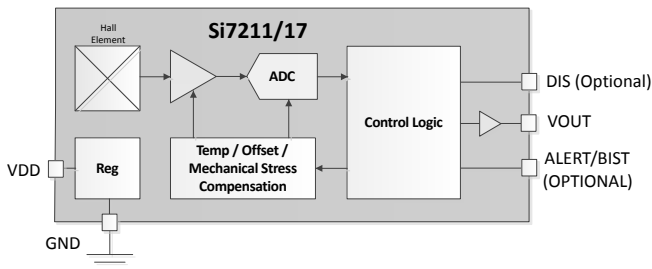
Si721x デバイスは、5 ピン SOT23 と 8 ピン DFN（近日発売）パッケージでも提供され、追加のピンは、スリープ・モード (DIS) に使用したり、内蔵セルフテスト (BISTb) 用のオンチップ・コイルを作動させるために使用することができます。

## アプリケーション

- 民生用、工業用、および車載アプリケーションで機械式位置検出
- 液面レベル検出
- 制御ノブおよびセレクタ・スイッチ
- カメラの手ぶれ補正、ズーム、オートフォーカス

## 機能

- 高感度ホール効果センサー
- 磁場に対応した低ノイズ出力
- 温度およびオフセット・ドリフト補正用統合型デジタル信号処理
- 低いスリープ・モード標準消費電流 50 nA
- 感度、出力極性、サンプル・レートを設定可能
- 温度範囲全体の感度ドリフト <  $\pm 3\%$
- 幅広い電源電圧
  - 1.7 ~ 5.5 V
  - 3.3 ~ 26.5 V
- 構成可能な出力オプション
  - アナログ
  - PWM
  - SENT
- 業界標準パッケージング
  - 表面実装 SOT-23 (3 または 5 ピン)
  - TO92 パッケージ
  - DFN パッケージ (近日発売)



# Table of Contents

<b>1. Electrical Specifications</b>	<b>3</b>
<b>2. Functional Description</b>	<b>9</b>
<b>3. Analog Output</b>	<b>10</b>
<b>4. PWM Output Description</b>	<b>11</b>
<b>5. SENT Output</b>	<b>12</b>
5.1 tSENT Status Nibble	12
5.2 SENT Data Nibbles	13
5.3 CRC Calculation	13
5.4 SENT Pause Pulse	13
5.5 SENT Frame Rate	13
5.6 BIST Activation During SENT Operation	13
<b>6. Pin Description</b>	<b>14</b>
<b>7. Ordering Guide</b>	<b>16</b>
<b>8. Package Outline</b>	<b>18</b>
8.1 SOT23 3-Pin Package	18
8.2 SOT23-5 5-Pin Package	20
8.3 TO92S 3-Pin Package	22
<b>9. Land Patterns</b>	<b>23</b>
9.1 SOT23 3-Pin PCB Land Pattern	23
9.2 SOT23-5 5-Pin PCB Land Pattern	24
<b>10. Top Marking</b>	<b>25</b>
10.1 SOT23 3-Pin Top Marking	25
10.2 SOT23-5 5-Pin Top Marking	26
10.3 TO92 Top Marking	26
<b>11. Revision History</b>	<b>27</b>

## 1. Electrical Specifications

Unless otherwise specified, all min/max specifications apply over the recommended operating conditions.

**Table 1.1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supply	$V_{DD}$	Si7211/7	2.25		5.5	V
Power Supply	$V_{DD}$	Si7212/3	1.71		5.5	V
Power Supply	$V_{DD}$	Si7214/5	3.3		26.5	V
Power Supply	$V_{DD}$	Si7216	4.0		26.5	V
Temperature	$T_A$	I grade	-40		+125	°C

**Table 1.2. General Specification<sup>1</sup>**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage High	$V_{IH}$	DIS or BIST pin	$0.7 \times V_{DD}$	-	-	V
Input Voltage Low	$V_{IL}$	DIS or BIST pin	-	-	$0.3 \times V_{DD}$	V
Input Voltage Range	$V_{IN}$	DIS or BIST pin	0		$V_{DD}$	V
Input Leakage	$I_{IL}$	DIS or BIST pin		< 0.1	1	$\mu A$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
Current Consumption Average power depends on the sample rate and percent of time spent sampling versus sleep mode or idle mode. See the selector guide for average power calculations.	I <sub>DD</sub>	Sleep mode		50		nA	
		V <sub>DD</sub> = 3.3 V, T = 25 °C				nA	
		V <sub>DD</sub> = 3.3 V, T = 70 °C			1000	nA	
		V <sub>DD</sub> = 5.5 V, T = 125 °C			5000	nA	
		Conversion in progress					
		Si7211/7			5.5	6.5	mA
		• V <sub>DD</sub> = 3.3 V			7.3	8.5	
		Si7212/3			3.5	4.5	mA
• V <sub>DD</sub> = 1.8 V			5.0	6.0			
• V <sub>DD</sub> = 5.0 V			6.8	8.0			
Si7214/5			6.5	8.5	mA		
Si7216			7	9	mA		
Idle mode						μA	
Si7212/3			600	1000			
Si7211/7			950	1150			
Si7214/5			900	1200			
Si7216			1400	1700			
Conversion Time	T <sub>CONV</sub>	First conversion when waking from idle		11		μs	
		Additional conversions in a burst		8.8		μs	
Idle Time	T <sub>IDLE</sub>	Factory programmable from 0 to 200msec ±10%. See <a href="#">Magnetic Sensors Selector Guide</a> for more details.  For Si721x analog, PWM and SENT output parts, in sleep mode (DIS high) the output is not active.		-			
Wake Up Time	T <sub>WAKE</sub>	Time from V <sub>DD</sub> > 1.7 V to first measurement			1	msec	
<b>Note:</b> 1. BIST and DIS pin specifications apply when the pin is present. 2. For high voltage parts (V <sub>DD</sub> = 26.5 V maximum), the power on ramp should be faster than 10 V per second in the start-up region from 2 to 3 V.							

Table 1.3. Output Pin Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Si7211/7</b>						
Offset <sup>1</sup>	B <sub>OFF</sub>	V <sub>DD</sub> = 2.25 - 5.5 V T = -40 to +125 °C		±300	±500	μT
		V <sub>DD</sub> = 2.25 - 3.6 V T = 0 to +70 °C			±300	μT
Ratiometric Gain Error	RGE	Change in gain as function of supply for V <sub>DD</sub> > 2.25.		±0.25		%/V
Gain Accuracy		-40 to +125 °C, V <sub>DD</sub> = 2.25- 5.5 V			12	%
		0 - 70 °C, V <sub>DD</sub> = 2.25 - 3.6 V			6	
Total Harmonic Distortion	THD	V <sub>out</sub> inside 20-80% of V <sub>DD</sub> , V <sub>DD</sub> > 2.5 V		0.15		%
Analog Noise at Output <sup>2</sup>				1		μV/rHz
Short Circuit Protection	I <sub>SS</sub>	Output shorted to ground of V <sub>DD</sub>		±15		mA
<b>Si7212/3</b>						
Output Voltage Low Open Drain or Push Pull	V <sub>OL</sub>	I <sub>OL</sub> = 3 mA V <sub>DD</sub> > 2 V			0.4	V
		I <sub>OL</sub> = 2 mA V <sub>DD</sub> > 1.7 V			0.2	V
		I <sub>OL</sub> = 6 mA V <sub>DD</sub> > 2 V			0.6	V
Leakage Output High Output Pin Open Drain	I <sub>OH</sub>				1	μA
Output Voltage High Output Pin Push Pull	V <sub>OH</sub>	I <sub>OH</sub> = 2 mA V <sub>DD</sub> > 2.25 V	V <sub>DD</sub> - 0.4			V
Slew Rate	T <sub>SLEW</sub>			5		%V <sub>DD</sub> /ns
<b>Si7214/5</b>						
Output Voltage Low	V <sub>OL</sub>	I <sub>OL</sub> = 11.4 mA V <sub>DD</sub> > 6 V			0.4	V
Safe Continuous Sink Current					20	mA
Leakage Output High Output Pin Open Drain	I <sub>OH</sub>				1	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew Rate Digital Output Mode	$T_{SLEW}$			5		$\%V_{DD}/ns$
Output Pin Shorted to VDD	$I_{SHORT}$	$V_{DD} = 12 V$ Average current as pin cycles		4		mA
<b>Si7216</b>						
Zero Field Output	$V_{OUT}$	$V_{DD} > 6 V$	2.4		2.6	V
Gain		$V_{DD} > 6 V$		125		mV/mT
<b>Note:</b>						
1. Deviation from $V_{DD}/2$ . To get voltage offset, divide by gain typically 40.96 mT/VDD.						
2. Analog noise is additive to magnetic sensor noise in RMS fashion. Generally magnetic sensor noise will dominate.						

Table 1.4. Magnetic Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	B <sub>OFF</sub>	20 mT scale Full temperature range		±250	+450, -350	μT
Gain Accuracy		0-70 °C			5	%
		Full temperature range			10	%
RMS Noise <sup>1</sup>		room Temp, 20 mT range, V <sub>DD</sub> = 5 V		30		μT rms

**Note:**

1. For a single conversion. This can be reduced by the square root of N by filtering over N samples. See ordering guide for samples taken per measurement

Table 1.5. Temperature Compensation

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Bop and Brp vs Temperature		Flat Tempco. 0-70°C		< ±0.05		%/°C
		Neodymium compensation		-0.12		%/°C
		Ceramic compensation		-0.2		%/°C

Table 1.6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Air Thermal Resistance	θ <sub>JA</sub>	JEDEC 4 layer board no airflow SOT23-5	212.8	°C/W
Junction to Board Thermal Resistance	θ <sub>JB</sub>	JEDEC 4 layer board no airflow SOT23-5	45	°C/W
Junction to Air Thermal Resistance	θ <sub>JA</sub>	JEDEC 4 layer board no airflow SOT23-3	254.6	°C/W
Junction to Board Thermal Resistance	θ <sub>JB</sub>	JEDEC 4 layer board no airflow SOT23-3	54.8	°C/W

**Note:** See [Magnetic Sensors Selector Guide](#).

Table 1.7. Absolute Maximum Ratings<sup>1</sup>

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature under Bias			-55		125	°C
Storage Temperature			-65		150	°C
Si7211/2/3/7						
Voltage on I/O Pins			-0.3		V <sub>DD</sub> +0.3	V
Voltage on V <sub>DD</sub> with Respect to GND			-0.3		6	V
ESD Tolerance		HBM			2	kV
		CDM			500	V
Si7214/5						
Voltage on Output Pin <sup>2</sup>			-21		40	V
Voltage on VDD with Respect to GND <sup>3</sup>			-21		40	V
ESD Tolerance		HBM			8	kV
		CDM			500	V
Si7216						
Voltage on Output Pin			-0.3		+5.5	V
V <sub>DD</sub> with Respect to GND			-21		+40	V
ESD Tolerance		HBM output pin			2	kV
		HBM V <sub>DD</sub>			8	kV
		CDM			500	V
<b>Note:</b>						
1. Absolute maximum ratings are stress ratings only, operation at or beyond these conditions is not implied and may shorten the life of the device or alter its performance.						
2. The output pin can withstand EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω to a local bypass cap of 0.1 μF and additional 22 Ω between the capacitor and ground.						
3. VDD can withstand automotive EMC transients per ISO 7637-2-2-11 and Ford EMC-CS-2009.1 with a current limiting resistor of 220 Ω.						



## 2. Functional Description

The Si7211/2/3/4/5/7 family of Hall Effect magnetic sensors digitize the component of the magnetic field in the z axis of the device (positive field is defined as pointing into the device from the bottom). The digitized field is then converted to an output format of analog, PWM or SENT and presented on the output pin.

**Table 2.1. Part Description**

Part Number	Description
Si7211, Si7217	Low voltage analog output
Si7212	Low voltage PWM output
Si7213	Low voltage SENT output
Si7214	High voltage PWM output
Si7215	High voltage SENT output
Si7216	High voltage $V_{DD}$ , low voltage analog out

Refer to the [Magnetic Sensors Selector Guide](#) for the two digit number after the die revision which gives more details about output, sampling frequency and other details.

Data output is always unsigned. That is, half scale ( $V_{DD}/2$  for analog out parts, 50% duty cycle for PWM output parts and 2048 (0x800) for SENT output parts) corresponds to zero field.

The parts are preconfigured for the magnetic field measurement range, idle time, temperature compensation and digital filtering and will wake into this mode when first powered. The specific configuration output type (open collector or push pull) are determined by the part number.

### 3. Analog Output

For the Si7211, the analog output is  $V_{DD}/2$  at zero field and goes from nearly zero at large negative field to nearly  $V_{DD}$  at large positive field.

$$B(mT) = (20.47 \text{ or } 204.7) \times \left( 2 \times \frac{V_{out}}{V_{dd}} - 1 \right)$$

4- and 5-pin packages also have the option of a BISTb pin. When configured and detected low, the internal coil is turned on until the pin is detected high again. Each subsequent BISTb activation flips the polarity of the coil during BIST.

For high voltage parts (Si7216), the output is ratiometric to an internally derived  $V_{DD}$  of 5V ( $\pm 5\%$ ) so long as the input  $V_{DD}$  is  $> 6$  V.

$$B(mT) = (20.47 \text{ or } 204.7) \times \left( 2 \times \frac{V_{out}}{5} - 1 \right)$$

For  $V_{DD} < 6$  V the internally derived reference drops 1 V for each 1 V drop in  $V_{DD}$  to the minimum recommended working voltage of 4.0 V.

## 4. PWM Output Description

The PWM output can be configured as open drain or push pull. High voltage parts can only be configured as open drain. The PWM duty cycle is factory configured and is normally set to in the range of 10 Hz to 1 KHz and is  $\pm 5\%$ . See ordering guide for specific part numbers..

As each measurement completes, the next PWM cycle will be updated to reflect the last measurement result. The duty cycle varies from 0 to 100% where 50% duty cycle means zero field, 0 % duty cycle generally means maximum negative field (-20.47 mT or -204.7 mT) and 100% duty cycle generally means maximum positive field (+20.47 or +204.7 mT). The high portion of the PWM is output first so that

$$B(mT) = \left(20.47 \text{ or } 204.7\right) \times \left(2 \times \frac{T_{high}}{T_{high} + T_{low}} - 1\right)$$

The host processor should look for a variation in the magnetic field to determine the entire system is working properly.

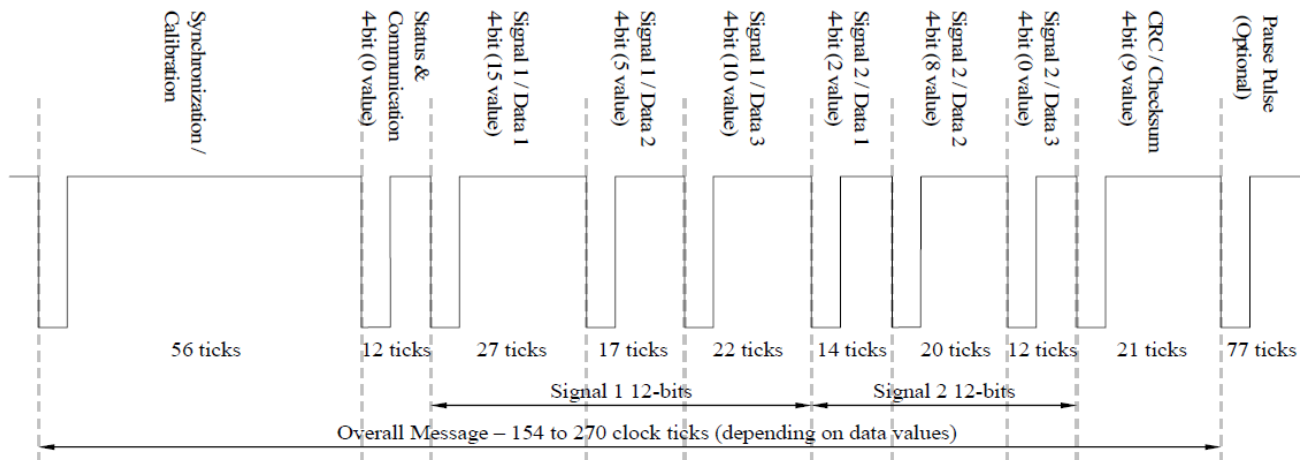
4- and 5-pin packages also have the option of a BISTb pin. When configured and detected low the internal coil is turned on until the pin is detected high again. Each subsequent BISTb activation flips the polarity of the coil during BIST.

## 5. SENT Output

The Si7213 and Si7215 output data in SENT (Single Edge Nibble transmission) format conforming to J2716 January 2010. All SENT output parts are configured as open collector.

SENT protocol messages consist of:

- A calibration/synchronization period consisting of 56 clock ticks
- A status and serial communication 4-bit nibble
- A sequence of up to six data nibbles
- A one nibble checksum
- Each nibble is 12 to 27 clock ticks
- An optional delay pause pulse



Minimum Nibble period = 36  $\mu$ sec @ 3  $\mu$ sec clock tick  
 Nibble encoded period = 36  $\mu$ sec + x\*(3  $\mu$ sec) (where x=0,1,...,15)

**Figure 5.1. SENT Timing Diagram**

As can be seen, each part of the sequence is determined by the timing between falling edges of the open drain sent output. First, a time of 56 clock ticks is produced so that the receiver can calibrate itself to the Si7213/5 speed. Then a total of 8 nibbles (4 bits per nibble) is produced. The edge to edge time of each nibble is 12 clock ticks for a data nibble of 0000b 13 ticks for a data value of 0001b and so on up to 27 ticks for a data value of 1111b.

The nominal tick time has been standardized at 5  $\mu$ sec ( $\pm$ 5%) however this is configurable.

### 5.1 tSENT Status Nibble

In the Si721x the four bit status nibble is defined as follows:

- Bit 3 and Bit 2 always transmitted as zeroes (No serial message support)
- Bit 1 and Bit 0
  - 00 Normal; No error condition
  - 01 Error condition
  - 10 Positive field BIST active
  - 11 Negative field BIST active

## 5.2 SENT Data Nibbles

The Si7213 and Si7215 are configurable to support a variety of options. The standard option follows J2716 A.3 where:

Signal	Data	Description
1	1	MSB of the magnetic field data
1	2	MidSB of the magnetic field data
1	3	LSB of the magnetic field data
2	1	MSB of an 8 bit rolling counter
2	2	LSB of an 8 bit rolling counter
2	3	An inverted copy of signal 1 data 1

For magnetic field, 3 nibbles are put together for a total 12 bit data word with values that can range from 0 to 4095. For magnetic field data, 2048 corresponds to zero field. The Si7213 can be configured for  $\pm 20.47$  mT full scale or  $\pm 204.7$  mT full scale. On the 20.47 mT full scale 1 LSB is 0.01 mT and on the 204.7 mT full scale 1 LSB is 0.1 mT.

## 5.3 CRC Calculation

The CRC is calculated based on the 6 data nibble according to  $x^4 + x^3 + x^2 + 1$  with a seed value of 0101 as per the recommendations in J2716 section 5.4.2.2. The legacy CRC calculation is not supported.

## 5.4 SENT Pause Pulse

The Si7213 and Si7215 are configurable for a pause pulse that is 12 ticks low, 256 ticks wide. However, the standard offering is no pause pulse.

## 5.5 SENT Frame Rate

For the standard offering with no pause pulse, each message will be 154 to 270 ticks in length. At a tick time of 5  $\mu$ sec this is 770 to 1350  $\mu$ sec. This gives an average frame rate of approximately 1 msec for the standard tick time of 5  $\mu$ sec. Conversion start is synchronized to the start of the synch pulse and is normally completed before the synch pulse completes so the data that is reported is the data obtained during the synch pulse time.

## 5.6 BIST Activation During SENT Operation

For 3-pin packages BIST can be activated by holding the output pin low for the entire message.

Once BIST is activated SENT messages resume 12 ticks after the SENT IO pin is detected high. Eight positive field BIST messages are followed by eight negative field BIST messages followed by a return to normal messages.

The nominal magnetic field output of the on-chip generator varies with coil current. The coil current varies with the coil resistance and power supply voltage, so the nominal magnetic field output varies according to:

$$B_{out} = B_{perVnom} \times V_{DD}$$

$B_{perVnom}$  is 1.6 mT/V

This can be used to calculate the expected magnetic field from the test coil for a given  $V_{DD}$ . This is somewhat temperature dependent, so the actual measured field will vary according to the accuracy of the part as well as temperature. Generally, as the coil is turned on and off the measured variation in field should be within  $\pm 25\%$  of expectation based on the calculated field generation.

The host processor should look for a variation in the magnetic field output to determine the entire system is working properly.

The 4- and 5-pin packages also have the option of a BISTb pin. When configured and detected low, the internal coil is turned on until the pin is detected high again. Each subsequent BISTb activation flips the polarity of the coil during BIST.

## 6. Pin Description

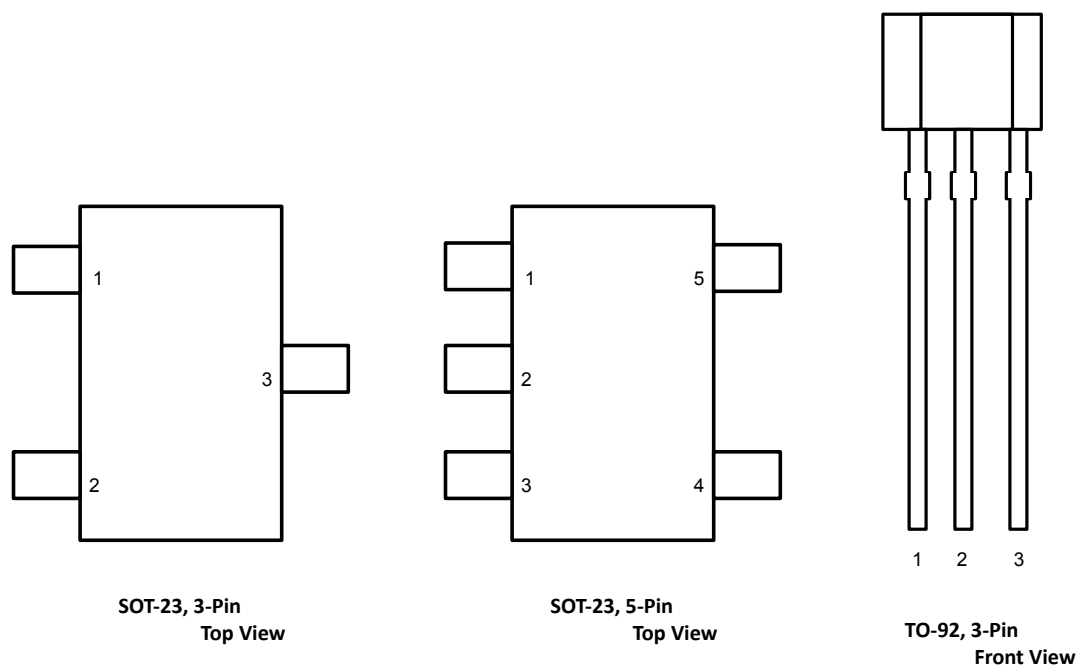


Figure 6.1. Si721x Pin Assignments

### Note:

The 3-pin option includes part numbers: Si7211/12/13/14/15/16.

The SOT-23 5 pin option include part numbers: Si7217.

Table 6.1. Si7211/12/13/14/15/16 (SOT23 3-pin Package)

Pin Name	Pin Number	Description
VDD	1	Power 2.25 to 5.5 V, 1.71 to 5.5 V, or 3.3 to 26.5 V
OUT1	2	Switch/latch output
GND	3	Ground

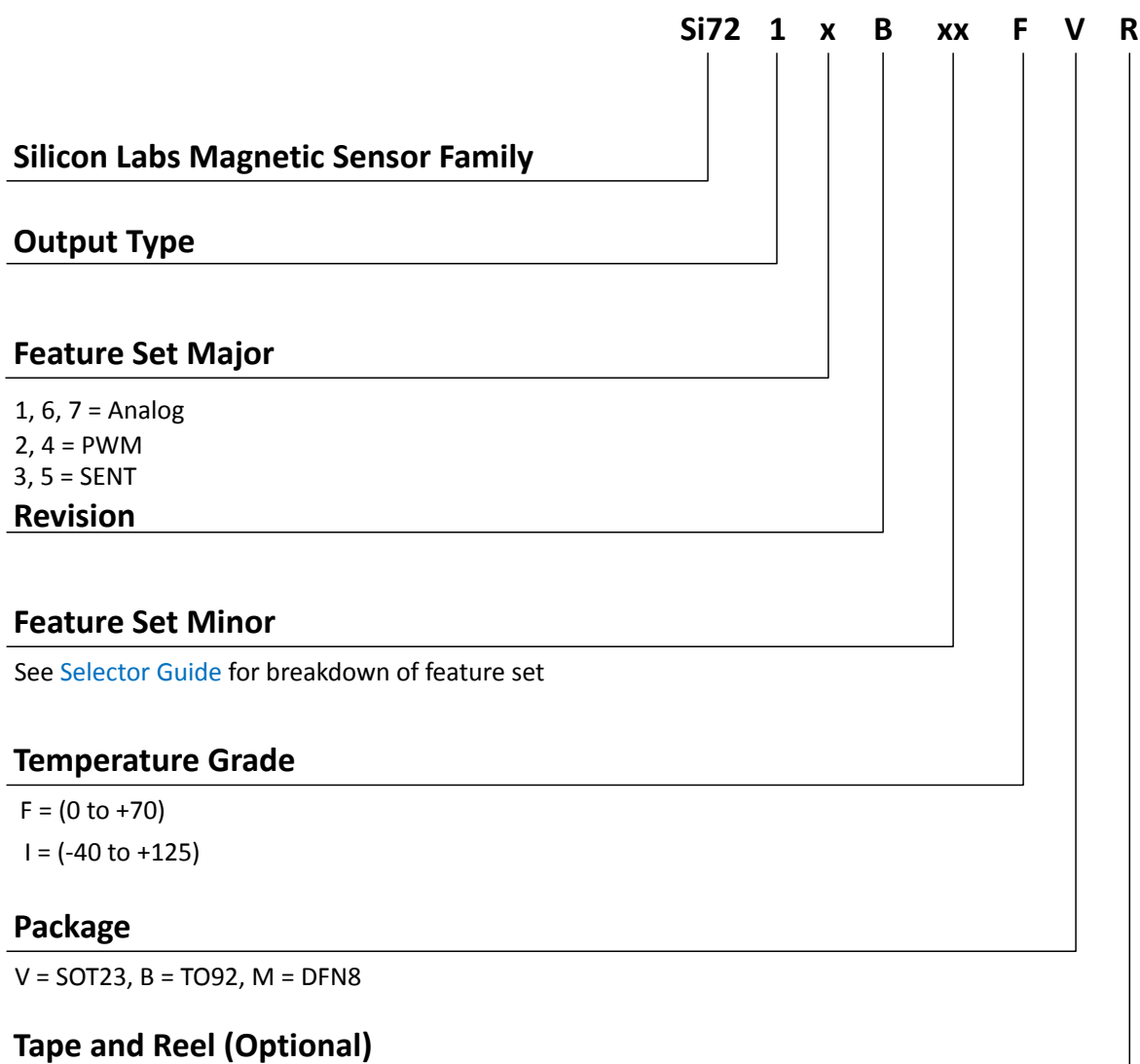
Table 6.2. Si7217 (SOT23 5-pin Package)

Pin Name	Pin Number	Description
OUT2/TAMPERb	1	OUT2/TAMPERb (tamper/high field indicator)
GND	2	Ground
DIS	3	Disables part (puts into sleep mode) when high. Measurement cycle will resume when pin goes low
VDD	4	Power 2.25 to 5.5 V
OUT1	5	Switch/latch output

**Table 6.3. Si7211 (TO-92 Package)**

Pin Name	Pin Number	Description
VDD	1	Power
GND	2	Ground
OUT1	3	Output

## 7. Ordering Guide



**Figure 7.1. Si721x Part Numbering**

**Table 7.1. Product Selection Guide**

Part Number	Output Type and Polarity	Package	Sample Rate and Scale	Temperature Compensation
<b>Analog output <math>V_{DD} = 2.25 - 5.5 V</math></b>				
Si7211-B-00-IV(R)	Analog, increasing field is increasing voltage	SOT23-3	7 kHz	No
			20 mT	
Si7211-B-00-IB	Analog, increasing field is increasing voltage	TO92	7 kHz	No
			20 mT	



Part Number	Output Type and Polarity	Package	Sample Rate and Scale	Temperature Compensation
Si7217-B-01-IV(R)	Analog, increasing field is increasing voltage	SOT23-5	7 kHz	No
			20 mT	
<b>PWM output <math>V_{DD} = 1.7 - 5.5</math> V (Default PWM speed is 250 Hz)</b>				
Si7212-B-00-IV(R)	Push pull, increasing pulse width is increasing field	SOT23-3	300 Hz	No
			20 mT	
<b>SENT output <math>V_{DD} = 1.7 - 5.5</math> V (default is 5 <math>\mu</math>sec tick time 1 kHz frame rate A.3 signaling)</b>				
Si7213-B-00-IV(R)	Open drain, increasing field gives increasing result	SOT23-3	1 kHz	No
			20 mT	
<b>Si7214 PWM output <math>V_{DD} = 3.3 - 26.5</math> V (Default PWM speed is 100 Hz)</b>				
Si7214-B-00-IV(R)*	Open drain. Increasing pulse width is increasing field	SOT23-3	150 Hz	No
			20 mT	
<b>SENT output <math>V_{DD} = 3.3 - 26.5</math> V (default is 5 <math>\mu</math>sec tick time 1 kHz frame rate A.3 signaling)</b>				
Si7215-B-00-IV(R)*	Open drain, increasing field gives increasing result	SOT23-3	1 kHz	No
			20 mT	
<b>Analog output <math>V_{DD} = 4.0</math> to <math>26.5</math> V</b>				
Si7216-B-00-IV(R)*	Analog, increasing field is increasing voltage	SOT23-3	1 kHz	No
			20 mT	
<b>*Note:</b> End of life.				

#### Additional Information

For information on the below specifications of each OPN refer to the [Magnetic Sensors Selector Guide](#):

- Current consumption
- Built in self test if applicable

All Si721x parts periodically measure the field and output the data in PWM, SENT, or analog format.

The Si721x parts are factory configurable for:

- The type of output analog, SENT, or PWM
- The amount of digital filtering applied to the samples
- The time between measurements
- The output pin can be open drain or push pull (SENT and PWM parts)
- Full scale can be programmed as 20mT or 200mT
- A temperature compensation can be applied to the field data to adjust for the variation in field with temperature for common magnet types

**Note:** North pole of a magnet at the bottom of a SOT23 package, top of a DFN 8 package(coming soon), or front of a TO92 package(coming soon) is defined as positive field.

## 8. Package Outline

### 8.1 SOT23 3-Pin Package

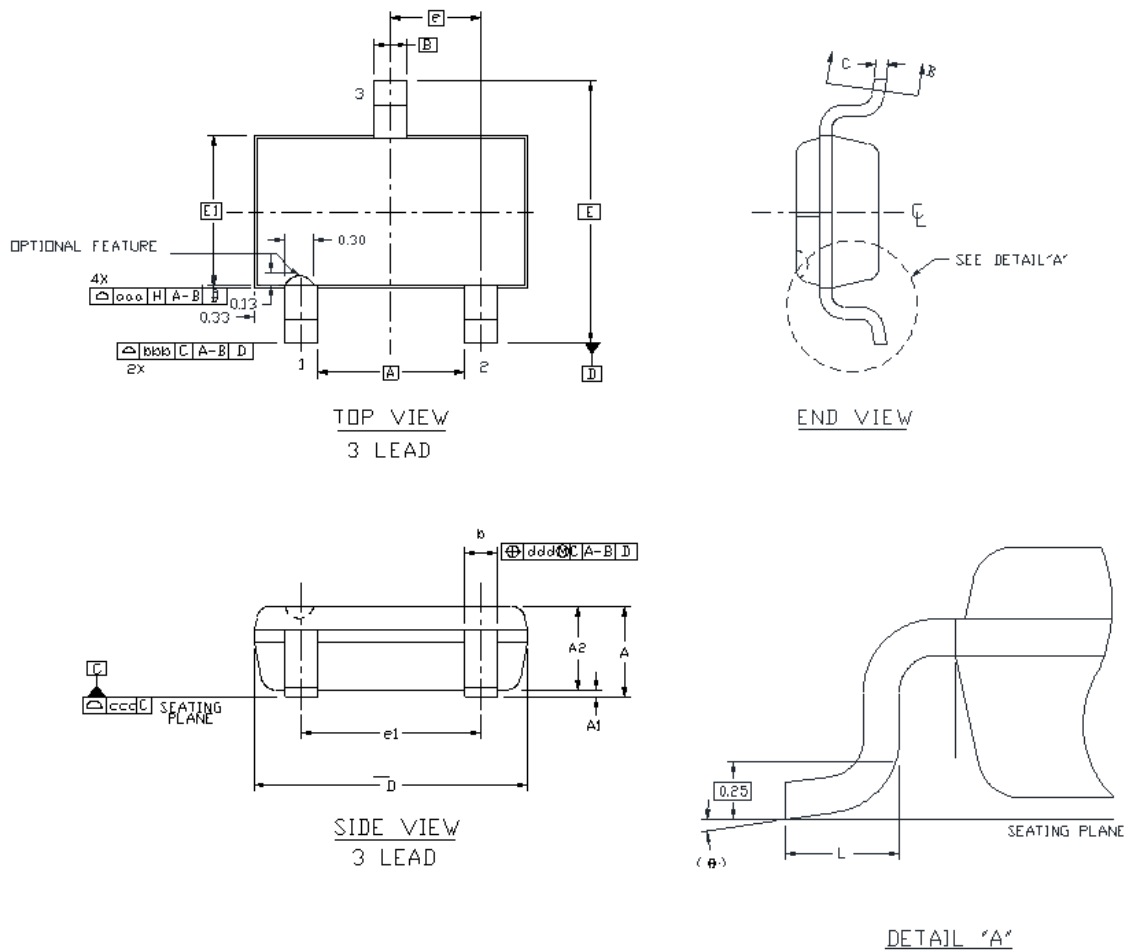


Table 8.1. SOT23 3-Pin Package Dimensions

Dimension	Min	Max
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.75 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
$\theta$	0°	8°
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.20	

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

8.2 SOT23-5 5-Pin Package

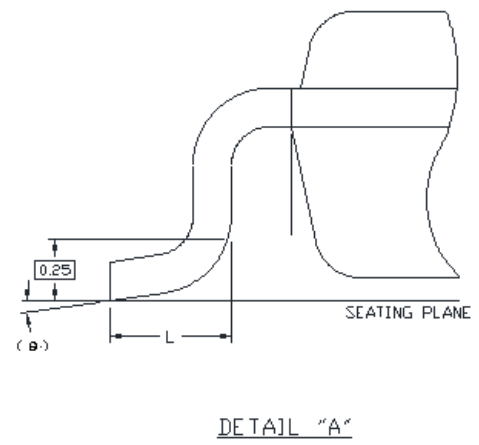
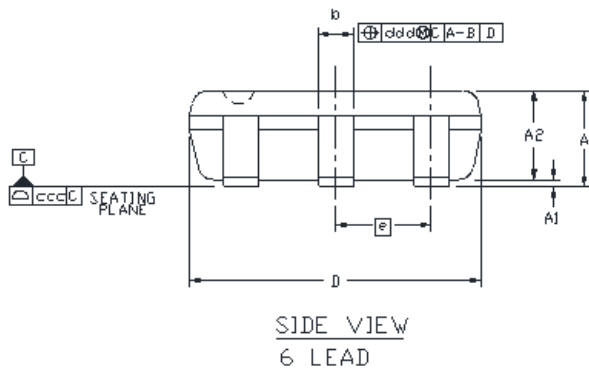
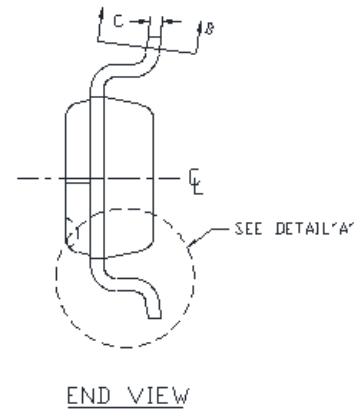
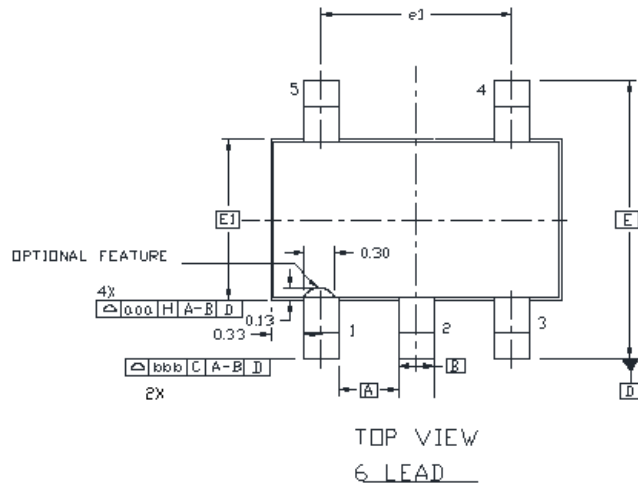


Table 8.2. SOT23-5 5-Pin Package Dimensions

Dimension	Min	Max
A	--	1.25
A1	0.00	0.10
A2	0.85	1.15
b	0.30	0.50
c	0.10	0.20
D	2.90 BSC	
E	2.75 BSC	
E1	1.60 BSC	
e	0.95 BSC	
e1	1.90 BSC	
L	0.30	0.60
L2	0.25 BSC	
$\theta$	0°	8°
aaa	0.15	
bbb	0.20	
ccc	0.10	
ddd	0.20	

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-193, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

8.3 TO92S 3-Pin Package

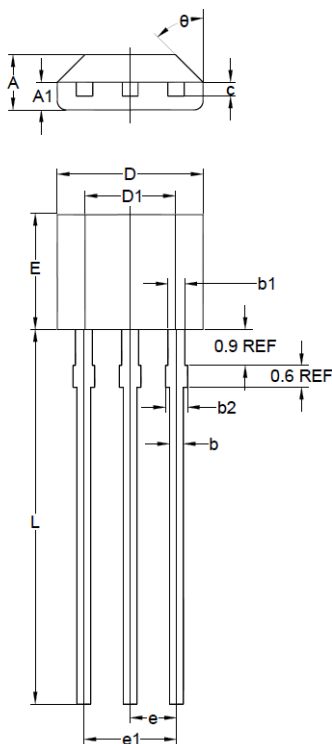


Table 8.3. TO92S 3-Pin Package Dimensions

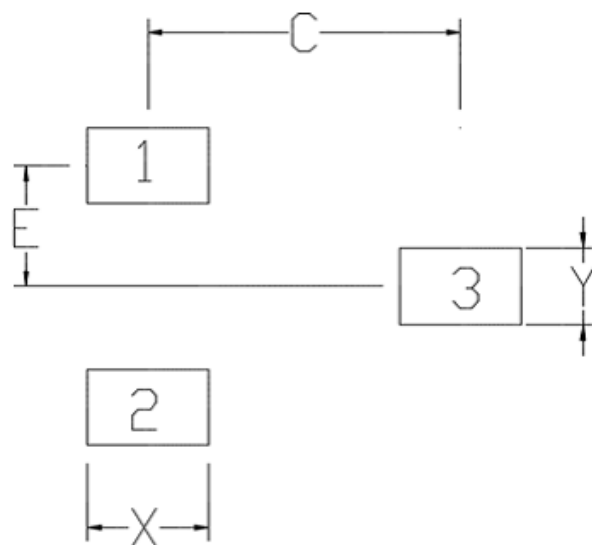
Dimension	Min	Max
A	1.42	1.62
A1	0.66	0.86
b	0.33	0.48
b1	0.40	0.51
b2	0	0.76
c	0.33	0.51
D	3.90	4.10
D1	2.28	2.68
E	3.05	3.25
e	1.27 TYP	
e1	2.44	2.46
L	15.10	15.50
$\theta$	45° TYP	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

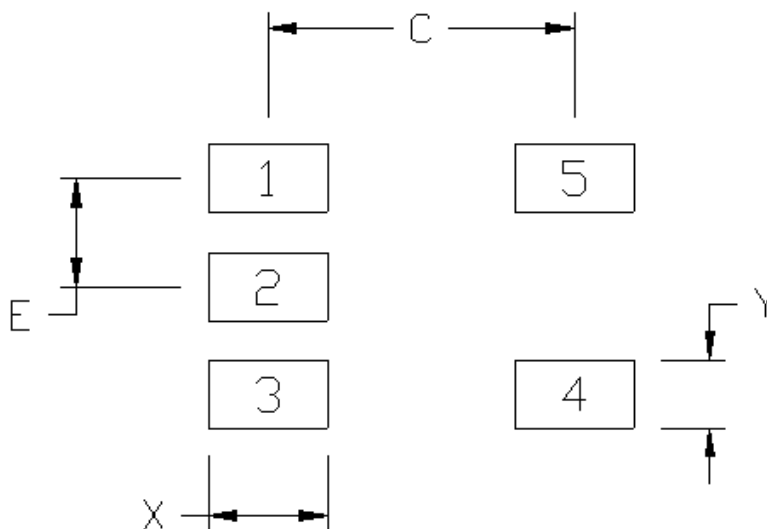
## 9. Land Patterns

### 9.1 SOT23 3-Pin PCB Land Pattern



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

**9.2 SOT23-5 5-Pin PCB Land Pattern**



Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

**Note:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

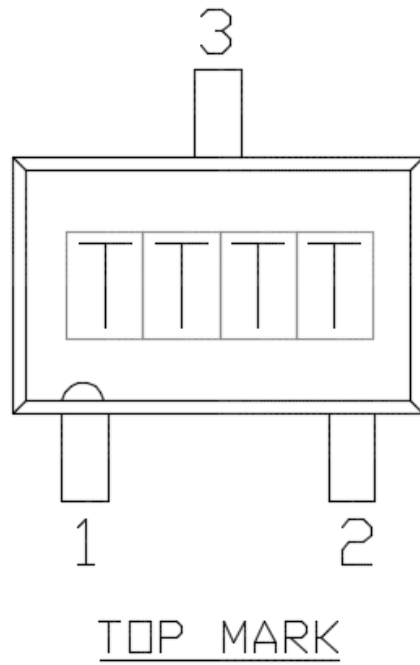
**Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.



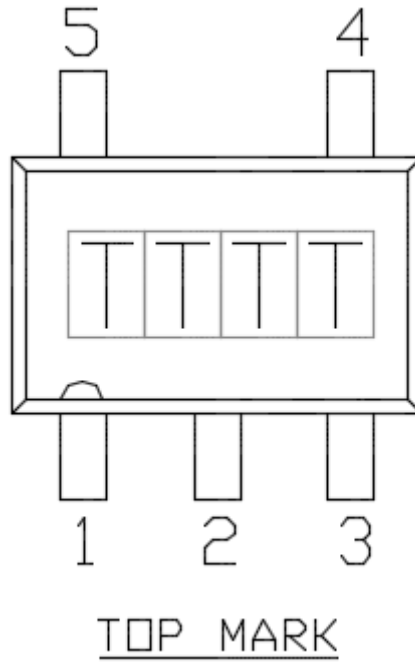
## 10. Top Marking

### 10.1 SOT23 3-Pin Top Marking



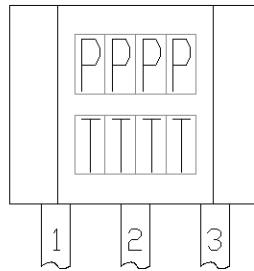
**Note:** TTTT is a manufacturing code.

### 10.2 SOT23-5 5-Pin Top Marking



**Note:** TTTT is a manufacturing code.

### 10.3 TO92 Top Marking



**Note:** TTTT is a manufacturing code. PPPP is 72xx.

## 11. Revision History

### Revision 1.3

May, 2020

- Added EOL note for Si7214/15/16 in the Ordering Guide (200324717 End of Life Notification for High Voltage Si72xx Devices).

### Revision 1.2

March, 2019

- Removed all mention of AEC-Q100 qualification in product description and feature list.

### Revision 1.1

October 11th, 2018

- Added Si7211 TO92 part number.
- Added details on Si7217 part number.
- Added specifications for Si7217.

### Revision 1.0

January 4, 2018

- Updated power numbers to be consistent with production test limits.
- Moved detailed ordering guide to a separate selection guide.
- Updated detailed description to be clearer and more accurate.

### Revision 0.9

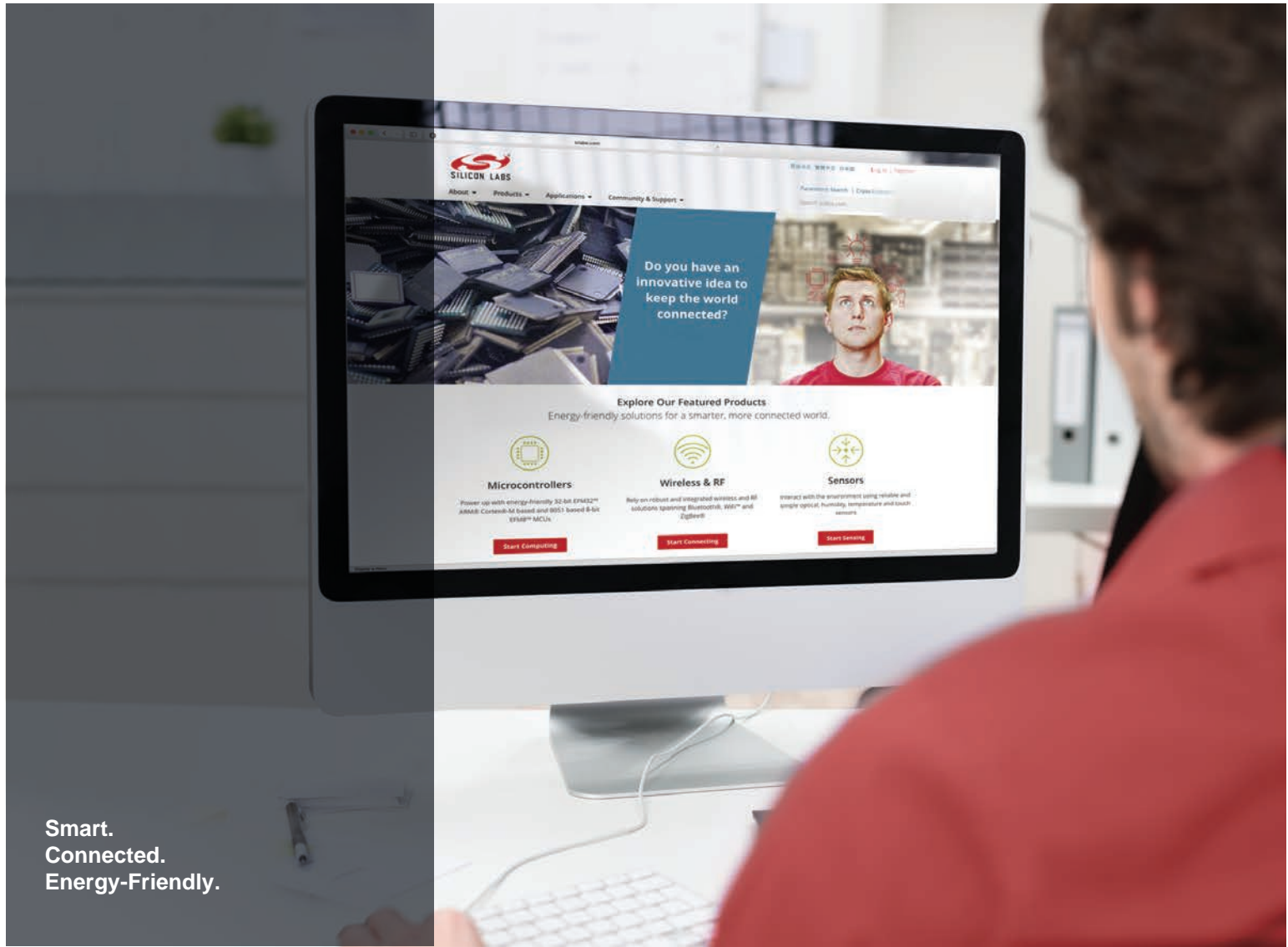
June 30, 2017

- Updated [1. Electrical Specifications](#).
- Updated [7. Ordering Guide](#).
- Minor typo corrections.

### Revision 0.1

February 1, 2016

- Initial release.



Smart.  
Connected.  
Energy-Friendly.



**Products**  
[www.silabs.com/products](http://www.silabs.com/products)



**Quality**  
[www.silabs.com/quality](http://www.silabs.com/quality)



**Support and Community**  
[community.silabs.com](http://community.silabs.com)

**Disclaimer**  
Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs may update product firmware during the manufacturing process for security or reliability reasons. Such changes will not alter the specifications or the performance of the product. Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required, or Life Support Systems without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of a Silicon Labs product in such unauthorized applications.

**Trademark Information**  
Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, ClockBuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR®, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, Gecko OS, Gecko OS Studio, ISOModem®, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri, the Zentri logo and Zentri DMS, Z-Wave®, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. Wi-Fi is a registered trademark of the Wi-Fi Alliance. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.  
400 West Cesar Chavez  
Austin, TX 78701  
USA

<http://www.silabs.com>