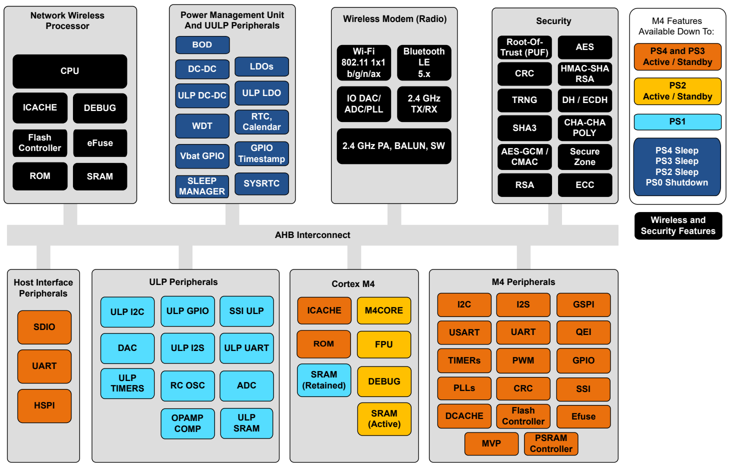
SiWG917 Wireless Module Data Sheet

Silicon Labs SiWG917 module is our lowest power Wi-Fi 6 plus Bluetooth LE 5.4, ideal for ultra-low power IoT wireless devices using Wi-Fi®, Bluetooth, Matter, and IP networking for secure cloud connectivity. It is optimal for developing battery operated devices that need long battery life. SiWG917 module includes an ultra-low power Wi-Fi 6 plus Bluetooth Low Energy (LE) 5.4 wireless CPU subsystem, and an integrated micro-controller (MCU) application subsystem, security, peripherals and power management subsystem all in a single 16 x 21.1 x 2.3 mm package. The wireless subsystem consists of a multi-threaded Network Wireless Processor (NWP) running up to 160 MHz, baseband digital signal processing, analog front end, 2.4 GHz RF transceiver and integrated power amplifier. The application subsystem consists of an ARM® Cortex®-M4 running up to 180 MHz, embedded SRAM, flash, ultra-low power sensor hub, and matrix vector processor. The ARM® Cortex®-M4 is dedicated for peripheral and application-related processing, while the NWP runs the wireless and networking stacks on independent threads, thus providing a fully integrated solution that is ready for a wide range of embedded wireless IoT applications. The modules come with modular radio type approvals for various countries, including USA (FCC), Canada (IC/ISED) and Japan (MIC), and are in compliance with the relevant EN standards (including EN 300 328 v2.2.2) for the conformity with the directives and regulations in EU and UK.

SiWG917 applications include:

- Smart Home
- Security Cameras
- HVAC
- Smart Sensors
- Smart Appliances
- Health and Fitness
- Pet Trackers
- Smart Cities
- Smart Meters
- Industrial Wearables
- Smart Buildings
- Asset Tracking
- Smart hospitals



KEY FEATURES

- Wi-Fi 6 Single Band 2.4 GHz 20 MHz 1x1 stream IEEE 802.11 b/g/n/ax
- Bluetooth LE 5.4
- Single chip Matter Over Wi-Fi Solution
- ARM® Cortex® M4 Processor with FPU subsystem up to 180 MHz with rich set of Digital and Analog Peripherals.
- Wi-Fi 6 Benefits: TWT for improved efficiency and longer battery life, MU-MIMO/OFDMA for Higher Throughput, network capacity and low latency
- Best in Class Device and Wireless Security
- WLAN Tx power up to +17.5 dBm with integrated PA
- Bluetooth LE Tx power up to +17 dBm with integrated PA
- WLAN Rx sensitivity as low as -95.5 dBm
- Wi-Fi 4 Standby Associated mode current: 71 µA @ 1-second listen interval
- Embedded Flash option up to 8 MB/ optional external Flash up to 16 MB
- Embedded PSRAM option up to 2 MB/ optional external PSRAM option up to 16 MB
- Ultra-low power sensor hub peripherals
- Matrix Vector Processor (MVP)
- Embedded Wi-Fi, Bluetooth LE, Matter, and networking stacks supporting wireless coexistence
- Three software-configurable MCU application memory options for sharing the RAM between the wireless, system, and application (192/256/320 KB)
- Operating temperature: -40 to +85 ºC
- Operating supply range: 3.0 to 3.63 V
- Supply voltage for GPIOs: 1.71 to 3.63 V

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1. Feature List

- **Microcontroller**
  - ARM® Cortex® M4 core with up to 180 MHz, 225 DMIPS performance
  - Integrated Floating Point Unit (FPU) and Nested Vectored Interrupt Controller (NVIC).
  - Serial Wire Debug (SWD) and Joint Test Action Group (JTAG) debug options
  - Internal and external oscillators with Phase Locked Loops (PLLs)
  - In-Flash Application Programming (IAP), In-System Programming (ISP), and Over-the-Air (OTA) NWP Firmware Upgrade
  - Power-On Reset (POR), Brown-Out and Black-out Detect (BOD)[1] with separate thresholds
  - M4 has two dedicated Quad Serial Peripheral Interface (QSPI) controllers: one for Pseudo Static Random Access Memory (PSRAM) and one for Flash
- **Matrix Vector Processor (MVP)**[1]
  - Co-processor for offloading matrix math operations
  - Delivers faster Machine Learning (ML) inference with lower power consumption
  - Performs Real and Complex Matrix and Vector operations, providing manifold computing efficiency
- **Memory**
  - Embedded Static Random Access Memory (SRAM) up to 672 KB total for Application and Network Wireless Processor
  - On-chip SRAM of 192, 256, or 320 KB for M4 Application Processor based on the memory configuration
  - Support for Flash up to 8 MB (in-package), or Optional External Flash up to 16 MB.[1]
  - Support for PSRAM option up to 2 MB (in-package), Optional External PSRAM up to 16 MB[1]
- **Digital Peripherals**[1]
  - Secure Digital Input Output (SDIO) 2.0 secondary
  - 1x Universal Synchronous/Asynchronous Receiver Transmitter (USART)
  - 2x Universal Asynchronous Receiver Transmitter (UART)
  - 3x Synchronous Serial Interface (SSI)
  - 1x General SPI (GSPI)
  - 1x Host SPI (HSPI)[1]
  - 3x Inter-Integrated Circuit (I2C)
  - 2x Inter-IC Sound Bus (I2S)
  - Pulse Width Modulation (MCPWM)
  - Quadrature Encoder Interface (QEI)
  - Timers: 4x 16/32-bit, 1x 24-bit, Watchdog Timer (WDT), Real Time Clock (RTC)
  - Up to 43 General Purpose Input Outputs (GPIOs) with GPIO multiplexer
- **Analog Peripherals**[1]
  - 12-bit 16-ch, 2.5 Msps Analog to Digital Converter (ADC)
  - 10-bit Digital to Analog Converter (DAC)
- **Security**
  - Secure Boot
  - Secure firmware upgrade through boot-loader, Secure OTA
  - Secure Key storage and HW device identity with PUF
  - Secure Zone
  - Encrypted Execute in Place (XiP) from Flash/ PSRAM
  - Secure Attestation
  - Hardware Accelerators: Advanced Encryption Standard (AES) 128/256/192, Secure Hash Algorithm (SHA) 256/384/512, Hash Message Authentication Code (HMAC), Random Number Generator (RNG), Cyclic Redundancy Check (CRC), SHA3, AES-Galois Counter Mode (GCM), Cipher based Message Authentication Code (CMAC), Cha-Cha-poly, True Random Number Generator (TRNG)
  - Software Implementation: RSA, ECC
  - Anti Rollback
  - Debug Lock
- **Wi-Fi** [1]
  - Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
  - Support for 20 MHz channel bandwidth for 802.11n and 802.11ax.
  - Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi STA + BLE
  - Wi-Fi 6 Features: Individual Target wake-up time (iTWT), Broadcast TWT (bTWT), Intra PPDU power save, SU extended range (ER), Dual Carrier Modulation (DCM), DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Re-use, BSS Coloring, and NDP feedback up to 4 antennas
  - Transmit power up to +17.5 dBm with integrated PA
  - Receive sensitivity as low as -95.5 dBm
  - Data Rates: 802.11b: 1, 2, 5.5, 11 Mbps; 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
  - Operating Frequency Range [MHz]: 2412-2462 (North America, default), 2412-2472 (Europe, and other countries where applicable), 2412-2484 (Japan)
  - PTA Coexistence with Zigbee/Thread/Bluetooth
- **Bluetooth**
  - Transmit power up to +17 dBm with integrated PA
  - Receive sensitivity — LE 1 Mbps: -94 dBm, LR 125 kbps: -105.5 dBm
  - Operating Frequency Range: 2.402 GHz - 2.480 GHz
  - Supports Bluetooth® Low Energy (LE): High Speed (1 Mbps and 2 Mbps) and Long Range (LE Coded PHYs, 125 kbps and 500 kbps; these are referred to as "LR" throughout this data sheet)
  - Advertising extensions
  - Data length extensions

- **Analog Peripherals (cont.)**[1]
  - 3x Op-amps
  - 2x Comparators
  - Temperature Sensor
- **Embedded Bluetooth Stack**
  - Support GAP profile
  - Support GATT profile
  - Support SMP
  - Support LE L2CAP
- **WiSeConnect SDK Features** [1]
  - Simplified and Unified DX for Wi-Fi API and Platform APIs
  - Simplifies application development and presents clean and standardized APIs
  - Universal Configurator (UC) enables componentization, simplifying configuration of peripherals and examples
  - BSD and ARM IoT-compliant socket API
  - Available through Simplicity Studio and Github
- **Intelligent Power Management**
  - Power optimizations leveraging multiple power domains and partitioned sub systems
  - Many system-, component-, and circuit-level innovations and optimizations
  - Multiple Power states: PS4 / PS3 / PS2 / PS1[1] / PS0
  - Voltage & Frequency Scaling for MCU
  - Application-based Gear Shifting (switches from one power state to another based on processing requirements) for MCU
  - Deep sleep mode with only timer active – with and without RAM retention
- **Ultra-low Power Sensor Hub System**[1]
  - Offloads Sensor data collection without a need for MCU to be active
  - Extends battery life and recharging interval for IoT Sensors
- **MCU Sub-System Power Consumption**
  - Active current as low as 40.4 µA/MHz @ 20 MHz in low-power mode
  - Active current as low as 70.5 µA/MHz @ 180 MHz in high performance mode
  - Deep sleep mode current: ~4.5 µA
  - Voltage & frequency scaling
  - Deep sleep mode with only timer active – with and without RAM retention
- **Wireless Sub-System Power Consumption**
  - • Wi-Fi 4 Standby Associated mode current: 71 µA @ 1-second beacon listen interval
    - Wi-Fi 1 Mbps Listen current: 16.5 mA
    - Wi-Fi LP mode Rx current: 22 mA
    - Deep sleep current ~4.5 µA, Standby current (352 KB RAM retention) ~11 µA
- **Operating Range**
  - Operating supply range: 3.0 to 3.63 V
  - Supply voltage for GPIOs: 1.71 to 3.63 V
  - Operating temperature: -40 to +85 ºC
- **Bluetooth (cont.)**
  - LE Secure connections
  - LE channel selection algorithm 2 (CSA#2)
  - LL Privacy 1.2
  - LE dual role
  - BLE acceptlist
  - 2 Simultaneous BLE Connections (2 Peripheral, 2 Central, or 1 Central & 1 Peripheral)
- **Ultra-low Power (ULP) Peripherals**
  - ULP I2C
  - ULP I2S
  - ULP UART
  - ULP GPIO
  - ULP Timers
  - ULP ADC
  - ULP DAC
  - ULP UDMA
  - ULP SSI Primary
- **RF & Modem Features**
  - Integrated baseband processor with calibration memory
  - Integrated RF transceiver, high-power amplifier, balun and T/R switch
- **Embedded Wi-Fi Stack**[1]
  - Support for Embedded Wi-Fi STA mode, Wi-Fi access point mode, and concurrent (AP+STA) mode
  - Supports advanced Wi-Fi security features: WPA personal, WPA2 personal, WPA3 personal, WPA/WPA2 enterprise in STA mode
  - Networking: Integrated IPv4/IPv6 stack, TCP, UDP, ICMP, ICMPv6, ARP, DHCP Client/Server, DHCPv6 Client/Server, DNS Client, SSL3.0/TLS1.3 Client, SNTP, mDNS, SNI
  - Applications: HTTP/s Client, HTTP/s Server, MQTT/s Client, AWS Client, Azure Client
  - Sockets: BSD sockets, IoT sockets
  - Over-the-Air (OTA) firmware update
  - Provisioning using Wi-Fi AP or BLE
- **Software and Regulatory Certifications**
  - Wi-Fi Alliance: Wi-Fi 4, Wi-Fi 6
  - Matter Certification
  - Bluetooth SIG Qualification
  - Regulatory certifications: FCC (USA), IC/ISED (Canada), CE (EU), UKCA (UK), MIC (Japan), KC (South Korea), NCC (Taiwan), SRRC (China), ACMA (Australia), RSM (New Zealand)
- **Advanced Software Features**[1]
  - FreeRTOS, Zephyr
  - Amazon AWS Cloud Connectivity, Microsoft Azure Cloud Connectivity
  - SensorHub (SensorHub framework which enables easier integration of new sensors)

- **Supported Protocols**
  - Bluetooth Low Energy (BLE) 5.4
  - Wi-Fi 6 (802.11 b/g/n/ax)
- **Advanced Software Features (cont.)**[1]
  - SoC communication to external host via Co-Processor Communication (CPC) - Supported host interfaces are SDIO/SPI/UART
  - Dual-Host: Support both embedded TCP-IP and TCP-IP by-pass simultaneously
- **Dimensions**
  - 16 x 21.1 x 2.3 mm

Note:

1. For information about software roadmap features, lists of available features and profiles, and certification, contact Silicon Labs or refer to the Release Notes and Reference Manual.
2. All power and performance numbers are under ideal conditions.

2. Ordering Information

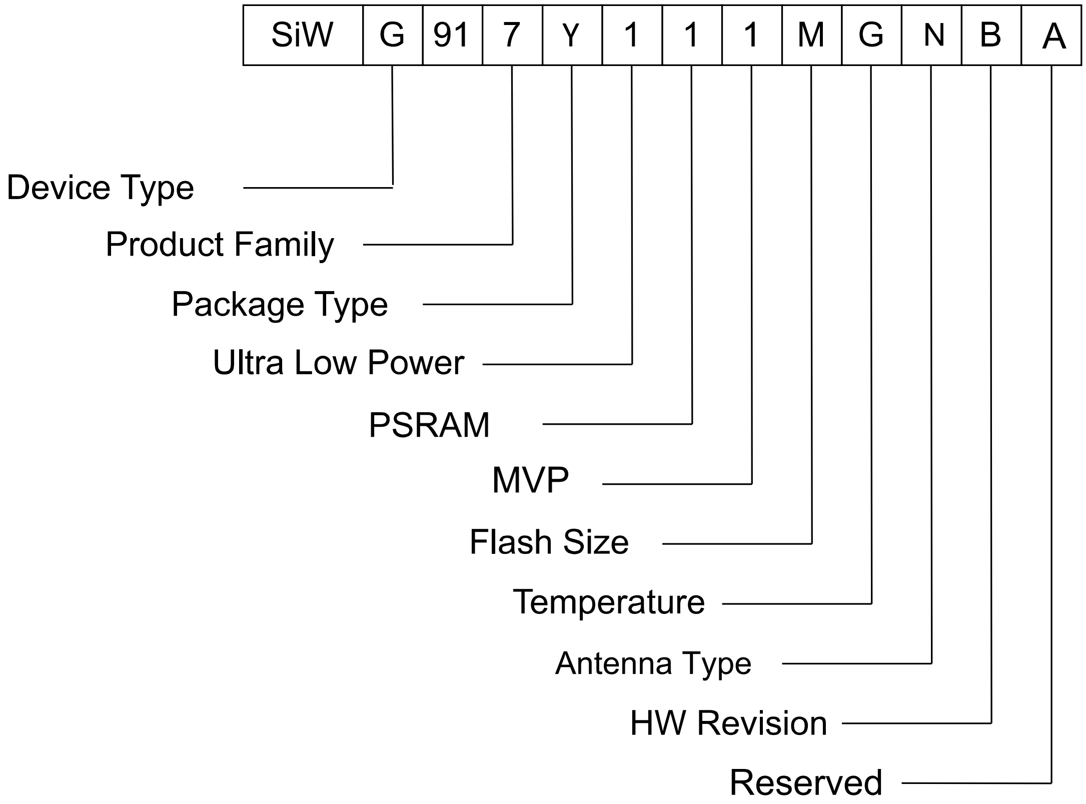


Figure 2.1. Ordering Guide

Table 2.1. Orderable Part Number (OPN) Decoder

Field	Options
Device Type	**T**: RCP (Transceiver) **N**: NCP **G**: SoC
Product Family	**7**: Ultra-low power
Package Type	**Y**: PCB Modules
Ultra-low Power	**1**: ULP Features enabled
PSRAM	**0**: No PSRAM Support **1**: External PSRAM **2**: 2 MB In-package PSRAM
MVP	**0**: MVP features disabled **1**: MVP Features enabled
Flash Size	**L**: 4 MB In-package Flash **M**: 8 MB In-package Flash
Temperature	**G**: -40 to +85 °C

Field	Options
Antenna Type	**N**: No Antenna **A**: Built-in Antenna
HW Revision	**B**: Revision B
Reserved	**A**: Reserved

Table 2.2. Part Ordering Options

Module OPN	Protocol Stack	Freq Band	Antenna	MVP	Flash/ PSRAM	GPIO	Temp Range (°C)	Packaging
SiWG917Y110LGNBA	BLE 5.4 Wi-Fi 6	2.4 GHz	No Antenna	No	4 MB flash	43	-40 to +85	Tape and Reel
SiWG917Y111MGNBA	BLE 5.4 Wi-Fi 6	2.4 GHz	No Antenna	Yes	8 MB flash	43	-40 to +85	Tape and Reel
SiWG917Y121MGNBA	BLE 5.4 Wi-Fi 6	2.4 GHz	No Antenna	Yes	8 MB flash, 2 MB PSRAM	43	-40 to +85	Tape and Reel
SiWG917Y110LGABA	BLE 5.4 Wi-Fi 6	2.4 GHz	Built-in Antenna	No	4 MB flash	43	-40 to +85	Tape and Reel
SiWG917Y111MGABA	BLE 5.4 Wi-Fi 6	2.4 GHz	Built-in Antenna	Yes	8 MB flash	43	-40 to +85	Tape and Reel
SiWG917Y121MGABA	BLE 5.4 Wi-Fi 6	2.4 GHz	Built-in Antenna	Yes	8 MB flash, 2 MB PSRAM	43	-40 to +85	Tape and Reel

Note:

1. Devices are shipped without firmware loaded. For custom parts with pre-loaded firmware, please contact Silicon Labs.
2. Throughout this document, the modules are referred to by their ordering codes above, or by their model names of SiW917Y1GN and SiW917Y1GA, respectively for the hardware variants with no antenna and with integral antenna, or by their marketing/friendly name of SiWG917.

Table of Contents

3. Applications

Smart Home

Smart Locks, Motion/Entrance Sensors, Water Leak sensors, Smart plugs/switches, Light Emitting Diode (LED) lights, Door-bell cameras, Washers/Dryers, Refrigerators, Thermostats, Consumer Security cameras, Voice Assistants, etc.

Other Consumer Applications

Toys, Anti-theft tags, Smart dispensers, Weighing scales, Fitness Monitors, Blood pressure monitors, Blood sugar monitors, Portable cameras, etc.

Other Applications (Medical, Industrial, Retail, Agricultural, Smart City, etc.)

Healthcare Tags, Industrial Wearables, Infusion pumps, Sensors/actuators in Manufacturing, Electronic Shelf labels, Agricultural sensors, Product tracking tags, Smart Meters, Parking sensors, Street LED lighting, Automotive After-market, Security Cameras, Gateways, etc.

4. Block Diagrams

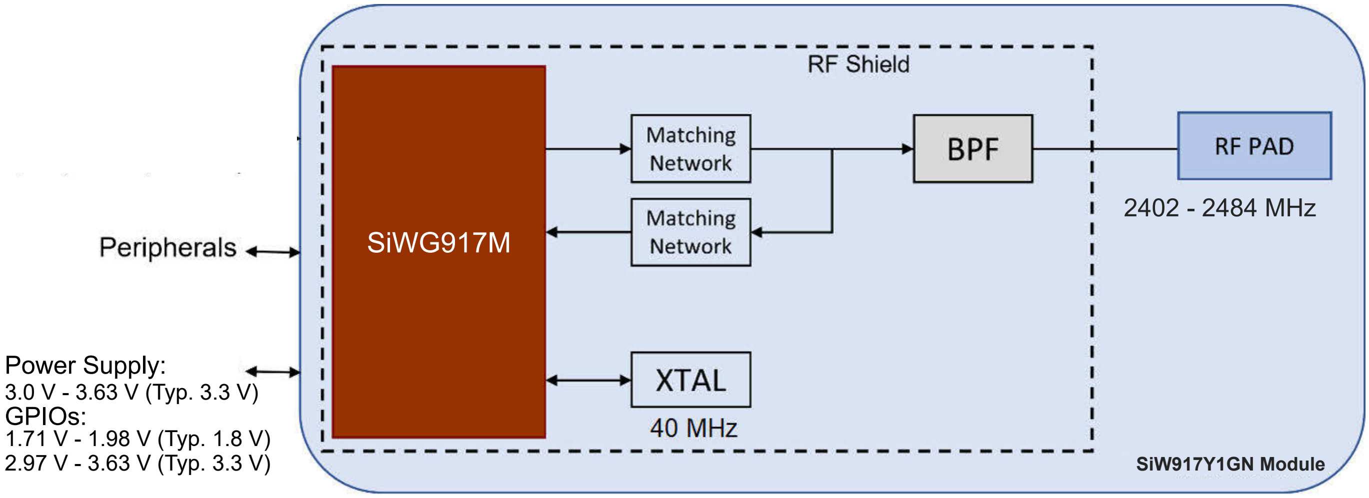


Figure 4.1. SiW917Y1GN (Without Antenna) Module Block Diagram

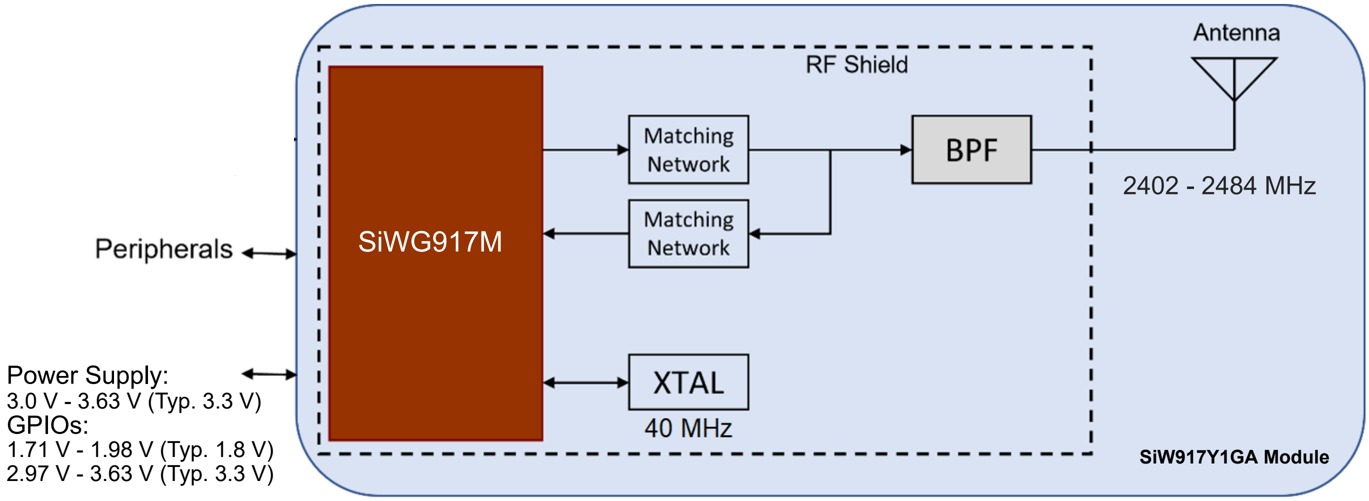


Figure 4.2. SiW917Y1GA (With Antenna) Module Block Diagram

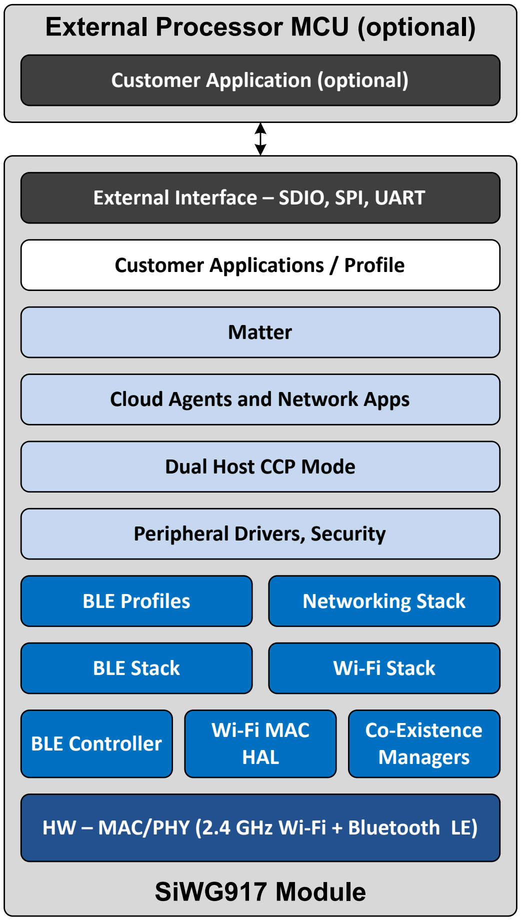


Figure 4.3. SiWG917 SoC Software Architecture

5. System Overview

5.1 Introduction

The SiWG917 Modules includes two processors: An ARM Cortex-M4 running up to 180 MHz and a Network Wireless Processor (NWP) 4- Threaded processor running up to 160 MHz. The Cortex-M4 is dedicated for peripheral and application related processing, whereas all the networking and wireless stacks run on independent threads of the NWP. In addition, in adherence to the Secure Execution Environment architecture, the NWP subsystem also acts as the secure processing domain and takes care of secure boot, secure firmware update, and provides access to security accelerators and secure peripherals through pre-defined APIs. The bus matrices of a Cortex M4 and NWP are separate and asynchronous. Though the two processors are present in a single chip, it is ensured that the NWP Networking, Security, and Wireless subsystem is completely separated from the ARM Cortex-M4 based application subsystem. Thus, these two processors have separate power, clocks/PLLs, bus-matrices, and memory. This provides two key advantages: programming, operating and power-state independence between the two processors and enhanced security by restricting access to the NWP subsystem.

SiWG917 modules are based on Silicon Labs' SiWG917M ultra-low-power, single spatial stream, 802.11 b/g/n/ax + BLE 5.4 Convergence SoC. The SiWG917 module provides low-cost CMOS integration of a multi-threaded MAC processor, baseband digital signal processing, analog front-end, crystal oscillator, calibration eFuse, 2.4GHz RF transceiver, integrated power amplifier, matching network, bandpass filter (BPF), and Quad-SPI Flash thus providing a fully-integrated solution for a range of hosted and embedded wireless applications. With Silicon Labs' embedded four-threaded processor and on-chip ROM and RAM, these chipsets enable integration into low cost and zero host load applications. With an integrated PMU and support for a variety of digital peripherals, SiWG917 modules enable very low-cost implementations for wireless hosted and embedded applications. It can be connected to a host processor through SDIO, SPI or UART interfaces. Wireless firmware upgrades and provisioning are supported.

5.2 ARM Cortex M4

The ARM Cortex-M4 is the main application processor in the SiWG917M embedded SoC. It is a high-performance 32-bit processor designed by ARM for the microcontroller market. It is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The M4 processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and Single Instruction Multiple Data (SIMD) multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division. The Cortex M4 microcontroller integrated into SiWG917M embedded SoC supports the following features:

- FPU and NVIC with 64 levels of interrupt priority
- Debug port with both JTAG as well as SWD interface; comprehensive debug functionality including data matching for a watch-point generation
- To provide optimal power vs performance tradeoff, unique gear-shifting is available for the Cortex-M4 that enables optimal power consumption based on the required performance. The available power-states are Power State 4 (PS4) at up to 180 MHz, Power State 3 (PS3) at up to 90 MHz, and Power State 2 (PS2) at up to 32 MHz. More details are provided in Section 5.5.4 Power States .
- Architectural clock gates are included to minimize dynamic power dissipation.
- The Network Wireless Processor and Cortex-M4 communicate through thread to thread interrupting and memory.
- On-chip M4 SRAM of 192/256/320 KB based on the SiWG917M embedded SoC chip configuration
- 8 KB is present in the ULP peripheral subsystem. This memory is present on the S-bus of the Cortex-M4 and is primarily used by the ULP MCU peripherals like ULP I2S, etc.
- 64 KB of ROM which hold the Cortex-M4 peripheral drivers
- 16 KB of instruction cache enabling XIP with external quad/octal SPI Single Data Rate (SDR) flashes
- Based on the SiWG917M embedded SoC package configuration, up to 8 MB of in-package QSPI flash is available for the Cortex-M4. This flash can be shared with the NWP in common flash mode.
- eFuse of 32 bytes (available for customer applications)
- 225 Dhrystone million instructions per second (DMIPS) performance

The Cortex-M4 core includes the following core peripherals:

Nested Vectored Interrupt Controller

The NVIC is an embedded interrupt controller that supports low latency interrupt processing.

Floating-Point Unit

The FPU provides IEEE754-compliant operations on single-precision, 32-bit, floating-point values. It supports addition, subtraction, multiplication, division and square root.

5.2.1 Memory Architecture

There are on chip Read Only Memory (ROM), Random Access Memory (RAM) and off chip FLASH connectivity. Sizes of ROM/RAM/FLASH will vary depending on the chip configuration.

Highlights:

- Unified memory architecture - software can partition the memory between code and data usage
- Multiport - RAMs support multi port access - allowing simultaneous access from different primaries (I, D, DMAs) to non overlapping regions without any cycle penalty
- ROM/RAMs are tightly coupled to the M4 processor I/D buses to reduce the latency and power

The Cortex-M4 processor has following memory:

- On-chip M4 SRAM of 192/256/320 KB based on the chip configuration
- 8 KB is present in the Ultra-low-power(ULP) peripheral subsystem. This memory is present on the S-bus of the Cortex-M4 and is primarily used by the ULP MCU peripherals like ULP I2S, ADC, DAC etc.
- 64 KB of ROM which holds the M4 peripheral drivers and bootloader.
- 16 KB of Instruction cache (I cache) enabling eXecute In Place (XIP) with external quad/octal SPI SDR flashes.
- Based on the package configuration up to 8 MB of "in-package" Quad SPI flash is available for the M4. This flash can be shared with the NWP in common flash mode
- eFuse of 32 bytes (available for customer applications)
- 16 KB of Data cache (D cache) enabling data fetching with PSRAM and Instruction cache (I cache) to execute code from PSRAM
- Flash Memory:
  - Based on the package configuration (OPN) up to 8 MB of "in-package" Quad SPI flash is available.
  - In addition, IC can support external flash option
    - IC has the support for 2-flash configuration
      - Common flash: Flash is common for both Cortex M4 and NWP
      - Dual Flash: Separate flash can be used for Cortex M4 and NWP

5.2.1.1 Flash Architecture

Details for Flash Architecture are explained in the Flash Memory Section of the Reference Manual.

5.2.1.2 SRAM Memory Sharing between Cortex M4 and Network Wireless Processor

A configurable SRAM feature for different processors can reduce the total on-chip memory requirement while addressing the memory requirements for different product modes.

The 91x SoC architecture allows different memory sizes allocated to the Cortex M4 and NWP processors based on the chip configuration at bootup time. The allocated memory will run on the respective processor clock. Through the efficient hardware design, memory sizes are divided and accessible by multiple processors in a single cycle using tightly coupled interfaces (TCM).

On-chip SRAM memory can be allocated to the two processors in four chunks: 352 KB, 64 KB, 64 KB, and 192 KB. The 352 KB chunk is always allocated to the NWP processor while the 192 KB chunk is always allocated to the Cortex M4. The remaining two 64 KB chunks can be allocated to either the Cortex M4 or the NWP processor. For example, if the NWP processor requires more than 352 KB, and the M4 does not need all 320 KB, an additional 64 KB or 128 KB can be allocated to the NWP.

Thus the available options are for the NWP to use 352, 416, or 480 KB SRAM, with the M4 using 320, 256, or 192 KB of SRAM, respectively.

Memory configuration between the MCU and Wireless Sub-system is shown in Table 5.14 Possible Memory Configurations between MCU and Wireless Sub-system on page 54.

The NWP and M4 memory architecture is shown in Figure 5.1 NWP and M4 shared SRAM memory architecture on page 16. NWPSS is the Network Wireless Processor subsystem and M4SS is the Cortex M4 subsystem

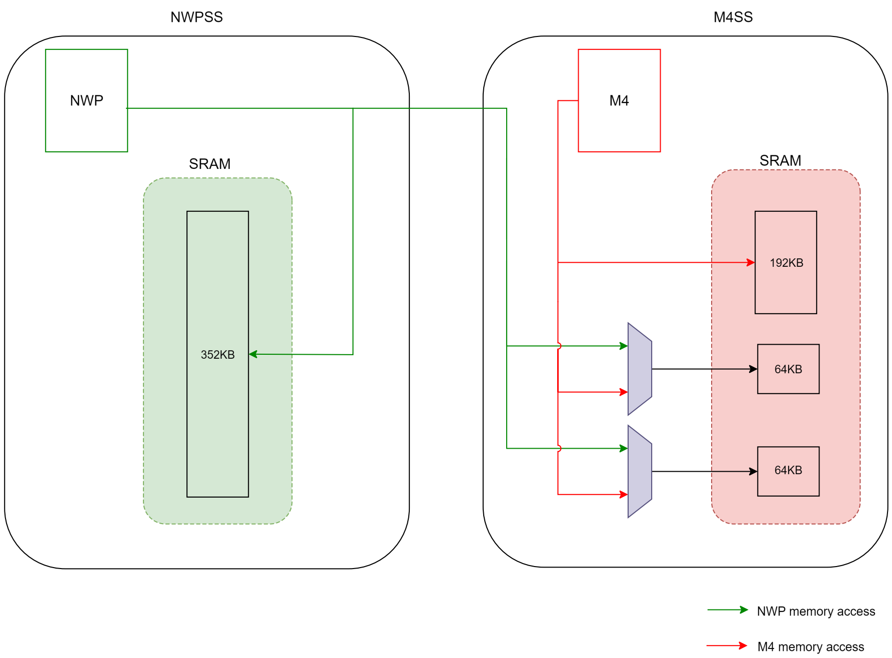


Figure 5.1. NWP and M4 shared SRAM memory architecture

5.3 Advanced Peripheral Bus (APB)

- The APB is part of the AMBA 3 protocol family.
- It provides a low-cost interface that is optimized for minimal power consumption and reduced interface complexity.
- The APB interfaces to any peripherals that are low-bandwidth and do not require the high performance of a pipelined bus interface.
- The APB has unpipelined protocol.
- All signal transitions are only related to the rising edge of the clock to enable the integration of APB peripherals easily into any design flow.
- Every transfer takes at least two cycles.
- It can be used to provide access to the programmable control registers of peripheral devices.

5.4 Interconnect

The following are the buses and bridges that form the interconnect in SiWG917 module. MCU refers to the Cortex-M4, and NWP refers to the Network Wireless Processor.

- High Performance (HP) MCU AHB Interconnect Matrix (ICM)
- MCU AHB-to-APB dual bridge
- MCU AHB-to-ULP MCU synchronous AHB bridge
- ULP MCU AHB ICM
- ULP MCU AHB-to-APB bridge
- MCU AHB - NWP AHB bridge
- High Performance NWP AHB ICM
- NWP AHB-to-APB dual bridge

The High-performance MCU AHB ICM is a multilayer interconnect implementation of the AHB protocol designed for higher performance and higher frequency systems.

Address Mapping

The Table 5.1 MCU AHB Secondary Address Mapping on page 18 has the base addresses of memories and high-speed peripherals.

Table 5.1. MCU AHB Secondary Address Mapping

Block Name	Size	Start Address
Memories		
LP SRAM	320 KB	0x0000_0000
ROM	64 KB	0x0030_0000
AHB Peripherals		
QSPI 1 Direct Access Mode	32 MB	0x0800_0000
QSPI 1 Indirect Access Mode	256 KB	0x1200_0000
QSPI 2 Direct Access Mode	32 MB	0x0A00_0000
QSPI 2 Indirect Access Mode	256 KB	0X1204_0000
SDIO/HSPI Secondary	64 KB	0x2020_0000
Icache	64 KB	0x2028_0000
GPDMA	512 KB	0x2108_0000
ULPSS AHB Bridge	256 KB	0x2404_0000
APB Bridge	64 MB	0x4400_0000
NWP AHB Bridge	512 MB	0x0010_0000 / 0x0040_0000 / 0x0060_0000 / 0x0400_0000 / 0x1000_0000 / 0x2010_0000 / 0x2040_0000 / 0x2100_0000 / 0x2200_0000 / 0x4000_0000
MVP Secondary	256 KB	0x2400_0000

The Table 5.2 MCU APB Peripherals Address Mapping on page 19 has the base addresses of all low-speed MCU peripherals.

Table 5.2. MCU APB Peripherals Address Mapping

Peripheral	Base Address
PERIPHERAL Power Domain	
UART0 (USART0 in asynchronous mode)	0x4400_0000
USART0 (USART0 in synchronous mode)	0x4400_0100
I2C0	0x4401_0000
SSI_MST	0x4402_0000
UDMA	0x4403_0000
DCACHE	0x4404_0000
SSI_SLV	0x4501_0000
UART1	0x4502_0000
GSPI	0x4503_0000
CONFIG_TIMER	0x4506_0000
CRC	0x4508_0000
HWRNG	0x4509_0000
I2C1	0x4704_0000
I2S0	0x4705_0000
QEI	0x4706_0000
MCPWM	0x4707_0000
Peripherals part of ALWAYS ON Domain	
VIC	0x4611_0000
ROM_PATCH	0x4612_0200
EGPIO	0x4613_0000
REG_SPI	0x4618_0000
PMU	0x4600_0000
PAD_CFG	0x4600_4000
MISC_CFG	0x4600_8000
EFUSE	0x4600_C000

The Table 5.3 ULP MCU APB Peripherals Address Mapping on page 20 has the base addresses of all low-speed ULP MCU peripherals.

Table 5.3. ULP MCU APB Peripherals Address Mapping

Peripheral	Starting Address
ULP_I2C	0x2404_0000
ULP_I2S	0x2404_0400
SSI_ULP	0x2404_0800
ULP Config	0x2404_1400
ULP_UART	0x2404_1800
ULP_TIMER	0x2404_2000
AUX ADC DAC Controller	0x2404_3800
NPSS_APB	0x2404_8000
ULP_EGPIO	0x2404_C000
IPMU Reg Access SPI	0x2405_0000
ULP Memory	0x2406_0000
ULP_UDMA	0x2407_8000

5.5 Power Architecture

The Power Control Hardware implements the control sequences for transitioning between different power states (Active/Standby/Sleep/Shutdown) and the power control for different group of peripherals. In addition, wakeup from any of the Standby/Sleep/Shutdown states based on hardware events or peripheral interrupts is supported. The Standby and Shutdown states can be reached from Active mode only through a Wait for Interrupt (WFI) instruction. Wakeup from Standby/Sleep/Shutdown states is through a hardware event or interrupt (Peripheral or External).

5.5.1 Highlights

- Two integrated buck switching regulators enable efficient Voltage Scaling across wide operating mode currents.
- High performance and ultra-low-power MCU peripheral subsystems and buses.
- Multiple voltage domains with independent voltage scaling of each domain.
- Fine grained power-gating including peripherals, buses and pads, thereby reducing power consumption when the peripheral/buses/pads are inactive.
- Multiple active states using "gear-shifting" approach based on processing requirements, thereby reducing power consumption for low-power applications.
- Flexible switching between different active states with controls from software.
- Hardware based wakeup from Standby/Sleep/Shutdown states.
- All the peripherals are clock gated by default, thereby reducing the power consumption in inactive state.
- Timer-based wakeup configurable by software before going into sleep.

5.5.2 Power Domains

All the applications, high-speed interfaces, and peripherals are segregated into multiple power domains to achieve lower current consumption when they are inactive. At reset, all the domains are powered ON.

Table 5.4 List of Power Domains on page 21 describes the different group of peripherals for which power is controlled through software.

Table 5.4. List of Power Domains

S.No	Section	Domain Name	Functionality of the Power Domain
1	APPLICATIONS	DEBUG_FPU	Debug Functionality for Cortex-M4, Floating Point Unit for Cortex-M4
		ROM	ROM Core/Interface
		SRAM	SRAM Banks
2	HIGH SPEED INTERFACE	QSPI_ICACHE	Quad/Octal 1 SPI SDR Flash Interface and ICache for the Cortex-M4 Processor, QSPI2 PSRAM interface, DCACHE
3	HP-PERIPHERALS	PERI_EFUSE	SPI/Synchronous Serial Interface (SSI) Primary, I2C, USART, Micro-DMA Controller, UART, SPI/SSI Secondary, Generic-SPI Primary, Config Timer, Random-Number Generator, CRC Accelerator, I2C, I2S Primary/Secondary, QEI, MCPWM and EFUSE for configuration information , MVP
		DMA	General Purpose DMA Controller
		SDIO-SPI	SDIO 2.0 Secondary, HSPI Secondary.
4	HIGH SPEED FLASH MEMORY	FLASH-LDO	Low DropOut (LDO)-FL 1.8 for Flash Memory
5	HIGH-FREQ-PLL	PLL-REGISTERS	PLL Programming Registers for High frequency clocks.
6	ULP-PERIPHERALS	DMA	Micro-DMA Controller
		ADC-DAC	ADC and DAC Controller
		I2C	I2C Primary/Secondary
		SSI	SPI/SSI Primary
		UART	UART
		TIMER	Timers

S.No	Section	Domain Name	Functionality of the Power Domain
7	UULP-PERIPHERALS	WDT	Watch Dog Timer
		TS	Temperature Sensor Controller
		PS	Process Sensor Controller
		RTC	Real-Time Clock, MCU System Real Time Clock (SYSRTC)
		STORAGE-DOMAIN1	Storage Flops - Set1. Contains 8 bytes
		STORAGE-DOMAIN2	Storage Flops - Set2. Contains 8 bytes
		STORAGE-DOMAIN3	Storage Flops - Set3. Contains 16 bytes
		SLEEP-FSM	Finite State Machine (FSM) for Sleep/Wakeup
		CLOCK-CALIB	Calibration block for Sleep Clock.
		BBFFS	Programming Registers which can be retained during sleep.
		DS-TIMER	DEEP SLEEP Timer.
		TIMESTAMP	Timestamping Controller.
		LP-FSM	Low-Power (LP) FSM
		RETEN	Retention Flops which can be retained during sleep.
8	Analog-PERIPHERALS	Aux-ADC	Auxiliary ADC
		Aux-DAC	Auxiliary DAC
		BOD	Brown-Out Detector

The SRAM is also segregated into multiple power domains to achieve lower current consumption per the memory requirement. The power for the SRAM domains in active states can be controlled in the following manners:

- **Deep-Sleep with RAM Retention:** SRAM domains as described in the table below can be powered down for unused SRAM sections. This is configurable on a bank granularity. The RAM contents of powered down sections are not retained.
- **Deep-Sleep without RAM Retention:** No SRAM contents are retained, and the SRAM is not accessible in this state.

Table 5.5 Segregation of Power Domains for SRAM (328 KB) on page 22 describes the segregation of power domains for SRAM (328 KB).

Table 5.5. Segregation of Power Domains for SRAM (328 KB)

S.No	Section	Domain Name	Functionality of the Power Domain
1	LP-SRAM	LP-SRAM-1	4 KB of SRAM (1x Banks)
		LP-SRAM-2	4 KB of SRAM (1x Banks)
		LP-SRAM-3	4 KB of SRAM (1x Banks)
		LP-SRAM-4	4 KB of SRAM (1x Banks)
		LP-SRAM-5	16 KB of SRAM (1x Banks)
		LP-SRAM-6	32 KB of SRAM (2x Banks)
		LP-SRAM-7	64 KB of SRAM (4x Banks)
		LP-SRAM-8	64 KB of SRAM (4x Banks)
		LP-SRAM-9	64 KB of SRAM (4x Banks)
		LP-SRAM-10	64 KB of SRAM (4x Banks)

S.No	Section	Domain Name	Functionality of the Power Domain
2	ULP-SRAM	ULP-SRAM-1	2 KB of SRAM (1x Banks)
		ULP-SRAM-2	2 KB of SRAM (1x Banks)
		ULP-SRAM-3	2 KB of SRAM (1x Banks)
		ULP-SRAM-4	2 KB of SRAM (1x Banks)

5.5.3 Voltage Domains

All the applications, high-speed interfaces, and peripherals are segregated into multiple voltage domains to configure the operating voltages in different power states. This section describes the voltage domains and voltage source options available for each domain. These are configured based on the power state in which the device is operating. The voltage for each domain can be shut-off during sleep by configuring the source to SoC LDO (This supply is turned OFF during Sleep).

Table 5.6 List of Voltage Sources on page 24 lists the different voltage sources and the possible output voltages of each source at different power states. The voltage sources are described in detail in 5.5.8 Power Management.

Table 5.6. List of Voltage Sources

S.No	Voltage Source	Possible Output Voltage
1	SoC LDO	1.15 V 1.05 V
2	SC-DC 1.05	1.05 V
3	LDO 0.75 V	0.75 V

Table 5.7 List of Voltage Domains on page 24 lists the different voltage domains and the possible voltage sources for each domain.

Table 5.7. List of Voltage Domains

S.No	Voltage Domain	Functionality	SoC LDO	SC-DC 1.05 V	LDO 0.75 V
1	PROC-DOMAIN	M4 processor, DEBUG_FPU,	Yes	Yes	Yes
2	HIGH-VOLTAGE-DOMAIN	ICACHE, HIGH-SPEED-INTERFACES, HP-PERIPHERALS, DCACHE	Yes	No	No
3	LOW-VOLTAGE-LPRAM-16KB	LP-SRAM-1, LP-SRAM-2, LP-SRAM-3, LP-SRAM-4,	Yes	Yes	No
4	LOW-VOLTAGE-LPRAM	ROM LP-SRAM-5, LP-SRAM-6, LP-SRAM-7, LP-SRAM-8, LP-SRAM-9, LP-SRAM-10,	Yes	Yes	No
5	LOW-VOLTAGE-ULPPERIPH	ULP-PERIPHERALS	Yes	Yes	No
6	LOW-VOLTAGE-ULPRAM	ULP-SRAM	Yes	Yes	No
7	LOW-VOLTAGE-UULPPERIPH	UULP-PERIPHERALS	No	Yes	No

5.5.4 Power States

The power states available in different power modes (PS0, PS1, PS2, PS3, PS4) are listed below

- Reset State
- Active States
  - Power State1 (PS1)
  - Power State2 (PS2)
  - Power State3 (PS3)
  - Power State4 (PS4)
- Standby States
  - PS2-STANDBY
  - PS3-STANDBY
  - PS4-STANDBY
- Sleep States
  - PS2-SLEEP
  - PS3-SLEEP
  - PS4-SLEEP
- Shutdown States
  - Power State0 (PS0)

After reset, the M4 processor starts in the PS4 state which is the highest activity state where the full functionality is available. The other active states (PS2/PS3) will have limited functionality or processing power.

A transition from active states (PS2/PS3/PS4) to any other state (Sleep/Standby) can only be triggered by software.

A transition from Standby/Sleep/Shutdown states can be triggered by an enabled interrupt as configured by software before entering these states.

A transition from Standby/Sleep to active state is possible from where these states are entered.

There are different wakeup sources available in each Standby/Sleep/Shutdown state.

Figure 5.2 Power States on page 26 shows the transitions between different power states.

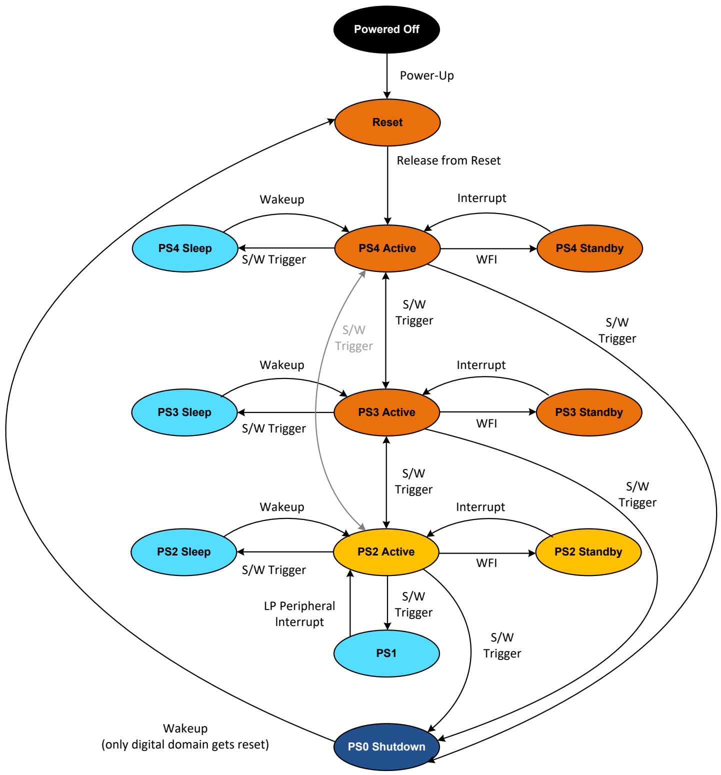


Figure 5.2. Power States

Note: A wakeup event from PS0 does not trigger a full system reset. Instead, only the digital domain is reset.

5.5.4.1 PS4

This is an active state where the complete functionality is available. The CPU, peripherals, and SRAM operate on the SoC LDO supply at voltage of 1.15 V.

The functionalities available in this state are mentioned below:

- Maximum CPU operating frequency of 180 MHz. The CPU can operate on the HIGH-FREQ-PLL output clocks.
- APPLICATIONS - DEBUG, FPU, ICACHE, and ROM.
- HIGH SPEED INTERFACE - as listed in Table 5.4 List of Power Domains on page 21.
- HIGH SPEED FLASH MEMORY - as listed in Table 5.4 List of Power Domains on page 21.
- HIGH-FREQ-PLL - as listed in Table 5.4 List of Power Domains on page 21.
- All the peripherals consisting of HP-PERIPHERALS, ULP-PERIPHERALS, Ultra Ultra Low Power (UULP-PERIPHERALS), and Analog-PERIPHERALS - as listed in the power domains section above.
- All GPIOs: 30 (GPIO) + 10 (ULP_GPIO) + 3 (UULP_VBAT_GPIO)
- Complete SRAM of up to 328 KB (320 KB Low Power (LP) - SRAM and 8 KB ULP-SRAM).

5.5.4.2 PS3

This is an active state where the complete functionality is available, similar to PS4 state, but it operates at a lower voltage, thereby reducing current consumption. The CPU, peripherals, and SRAM operate on the SoC LDO supply with output voltage of 1.05 V. The Maximum CPU frequency is limited to 90 MHz in this state.

5.5.4.3 PS2

This is an active state where a limited set of functionality is available, and the device operates at a much lower voltage compared to PS3/PS4, thereby achieving lower current consumption. The CPU, peripherals, and SRAM can operate at different voltages and are configurable by software before entering this state.

The functionalities available in this state are mentioned below:

- CPU operating frequency depends on the voltage source selected for PS2 state. The CPU operates on the ULP-Peripheral AHB Interface clock.
  - If LDO 0.75 V is used, maximum frequency is 20 MHz.
  - If SC-DC 1.05 V is used, maximum frequency is 32 MHz.
- APPLICATIONS - DEBUG, FPU, and ROM.
- Limited peripherals consisting of ULP-PERIPHERALS, UULP-PERIPHERALS and Analog-PERIPHERALS - as listed in Table 5.4 List of Power Domains on page 21.
- 13 GPIOs are available - 10 (ULP_GPIO) + 3 (UULP_VBAT_GPIO)
- Total SRAM of up to 328 KB (320 KB Low Power (LP)-SRAM and 8 KB ULP-SRAM).

5.5.4.4 PS1

This state can be entered from PS2 only through a software instruction. The CPU is power-gated, and a limited set of peripherals are active. The peripheral interrupts are used as wakeup sources or to trigger sleep once the peripheral functionality is complete. The peripherals and SRAM operate at the same voltage as the PS2 state. The peripherals need to be configured by the software for the defined functionality in the PS2 state before entering this state.

The functionalities available in this state are mentioned below:

- Limited peripherals consisting of ULP-PERIPHERALS, UULP-PERIPHERALS, and Analog-PERIPHERALS - as listed in Table 5.4 List of Power Domains on page 21.
- 13 GPIOs are available - 10 (ULP_GPIO) + 3 (UULP_VBAT_GPIO)
- SRAM of 320 KB (Low Power (LP)-SRAM) can be retained in this state.
- SRAM of 8 KB (ULP-SRAM) is active for peripheral functionality.

5.5.4.5 STANDBY

This includes multiple states: PS4-STANDBY, PS3-STANDBY, and PS2-STANDBY. These are standby states entered from PS4/PS3/PS2 states through a WFI instruction. CPU is clock gated in this state. The STANDBY states allow for much faster wake times compared to PSx-SLEEP, PS1, and PS0.

All the interrupts in the NVIC table will act as a wakeup source in the PS4-STANDBY and PS3-STANDBY states. Wakeup sources for the PS2-STANDBY state are defined in the wakeup sources section below. See Section 5.5.6 Wakeup Sources for details.

5.5.4.6 SLEEP

This includes multiple states: PS4-SLEEP, PS3-SLEEP, and PS2-SLEEP. These sleep states can be entered from the PS4, PS3, and PS2 states respectively through a software instruction.

The status of resources in this state are as follows:

- UULP-PERIPHERALS and Analog-PERIPHERALS are available and are configured before entering this state.
- 3 GPIOs are available - 3 (UULP_VBAT_GPIO)
- SRAM can be retained.

Wakeup sources for these states are defined in Section 5.5.6 Wakeup Sources. While transitioning from sleep to active state, all the configuration related to peripheral registers are set to default.

5.5.4.7 PS0

This is a shutdown state entered from PS2, PS3, or PS4 state through a software instruction. The CPU is power-gated, and a much smaller set of peripherals are available.

The status of resources in this state are

- UULP-PERIPHERALS and Analog-PERIPHERALS are available and are configured before entering this state.
- 3 GPIOs are available - 3 (UULP_VBAT_GPIO)
- SRAM can not be retained.

5.5.5 Memory Retention in Sleep / Shutdown States

The following table indicates the SRAM banks and Backup Register Array which can be retained in each Sleep/Shutdown state.

Table 5.8. SRAM in Different States

S.No	Power State	LP-SRAM (320 KB)	ULP-SRAM (8 KB)	Backup Register Array (32 bytes)
1	PS4-SLEEP	Yes	Yes	Yes
2	PS3-SLEEP	Yes	Yes	Yes
3	PS2-SLEEP	Yes	Yes	Yes
4	PS1	Yes	Yes	Yes
5	PS0	No	No	Yes

5.5.6 Wakeup Sources

The following table indicates the wakeup sources available in Standby/Sleep/Shutdown states.

Table 5.9. List of Wakeup Sources in Different States

Wakeup Source	PS4 / PS3 STANDBY	PS2 STANDBY	PS4 / PS3 SLEEP	PS2 SLEEP	PS1	PS0
UULP VBAT GPIO	Yes	Yes	Yes	Yes	No[1]	Yes
Watch-Dog Interrupt	Yes	Yes	Yes	Yes	No[1]	Yes
Analog Comparator	Yes	Yes	No	No	No[1]	No[1]
BOD	No[1]	No[1]	No[1]	No[1]	No[1]	No[1]
ULP-Peripheral SDC	Yes	Yes	No	No	Yes	No
Network Wireless Processor Interrupt	Yes	No	Yes	No[1]	No[1]	No[1]
Deep-Sleep Timer Interrupt	No	No	Yes	Yes	No[1]	Yes
Alarm Interrupt	Yes	Yes	Yes	Yes	No[1]	Yes
Second Based Interrupt	Yes	Yes	Yes	Yes	No[1]	Yes
SysRTC	Yes	Yes	Yes	Yes	No[1]	Yes
ULP-Peripheral GPIO Group Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral GPIO Pin Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral SPI/SSI Primary Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral I2S Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral I2C Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral UART Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral ADC/DAC Interrupt	Yes	Yes	No	No	Yes	No
ULP-Peripheral DMA Interrupt	Yes	Yes	No	No	No[1]	No
ULP-Peripheral Timer Interrupt	Yes	Yes	No	No	No[1]	No

1. Supported in hardware, but not supported in SDK available as of data sheet release date.
2. For information about software roadmap features, contact Silicon Labs or refer to SDK Release Notes.

5.5.7 System Power Supply Configurations

SiWG917 module support highly flexible power supply configurations for various application scenarios. Two application scenarios are listed below.

- 3.3 V single supply - A single 3.3 V supply derived from the system PMU can be input to all I/O supplies.
- 1.8 V and 3.3 V supply - A 1.8 V supply derived from the system PMU can be input to all I/O supplies except VBATT. A 3.3 V supply derived from system Power Management Unit (PMU) can be fed to the power amplifier supply pin VBATT.

5.5.8 Power Management

The SiWG917 module have an internal power management subsystem, including DC-DC converters and linear regulators. This subsystem generates all the voltages required by the module to operate from a wide variety of input sources.

- Input voltage (3.3 V) on pin VBATT
- Input voltage (1.8 V or 3.3 V) on pin IO_VDD, SDIO_IO_VDD and ULP_IO_VDD
- Input voltage (1.8 V) on pin FLASH_IO_VDD
- Nominal Output - 1.8 V and 48 mA maximum load on pin 1V8_LDO

5.6 Digital and Analog Peripherals and Interfaces

In addition to the wireless interfaces, the SiWG917 provides a rich set of peripherals and interfaces - both digital and analog - thus enabling varied systems and applications. The following are the categories of the peripherals and interfaces, description of each category, and list of the peripherals in that category.

5.6.1 Digital Peripherals and Interfaces

5.6.1.1 I^2C

- Up to three I^2C primary/secondary controllers - two in MCU HP peripherals and one in the MCU ULP subsystem
- I^2C standard compliant bus interface with open-drain pins
- Configurable as Primary or Secondary
- Four speed modes: Standard Mode (100 kbps), Fast Mode (400 kbps), Fast Mode Plus (1 Mbps), and High-Speed Mode (3.4 Mbps)
- 7 or 10-bit addressing
- 7 or 10-bit combined format transfers
- Support for Clock synchronization and Bus Clear
- Programmable SDA Hold time

The I^2C controllers also support additional features listed below to reduce the load on the M4 processor:

- Integrated transmit and receive buffers with support for DMA
- Bulk transmit mode in I^2C Secondary mode
- Interrupt based operation (polled mode also available)

5.6.1.2 UART/USART

- Up to two UART and one USART controllers
- 9-bit serial data support
- Multi-drop RS485 interface support
- 5, 6, 7, and 8-bit character encoding with even, odd, and no parity
- 1, 1.5 (only with 5 bit character encoding) and 2 stop bits
- Hardware Auto flow control (RTS/CTS)

The UART controllers also support additional features which are listed below and which help in achieving better performance and reducing the burden on the M4 processor:

- Programmable fractional baud rate support
- Programmable baud rate supporting up to 5 Mbps
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Prioritized interrupt identification

The following features are supported by the USART controller in the MCU HP peripherals (USART0):

- Support for both synchronous and asynchronous modes.
- Supports full duplex and half duplex (single wire) mode of communication.
- 5-8 bit wide character support.
- Supports programmable baud rates up to 20 Mbps in synchronous mode
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events.

The UART controller in the MCU ULP subsystem (ULP_UART) supports the following additional power-save features:

- After the DMA is programmed in PS2 state for UART transfers, the MCU can switch to PS1 state (M4 processor is turned off) while the UART controller continues with the data transfer
- In PS1 state (ULP Peripheral mode) the UART controller completes the data transfer and, triggered by the peripheral interrupt, shifts to the PS2 active state.

5.6.1.3 I^{2}S / PCM

- Up to two I^{2}S controllers
- Each I^{2}S supports PCM mode of operation
- The I2S0 supports two stereo channels while the ULP_I2S and the NWP/Security subsystem I^{2}S support one stereo channel
- Programmable audio data resolutions of 12, 16, 20, 24, and 32 bits.
- Supported audio sampling rates are 8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96, and 192 kHz
- Support for primary and secondary modes
- Full duplex communication due to the independence of transmitter and receiver

The PCM mode of operation supports the following additional features:

- Mono audio data is supported
- Supports two modes for data transmission with respect to the Frame Synchronization signal – the MS bit is transmitted in the same clock cycle that the Frame Synchronization signal is asserted or one clock cycle after the Frame Synchronization signal is asserted
- Programmable FIFO thresholds with maximum FIFO depth of 8 and support for DMA
- Supports generation of interrupts for different events

The I^{2}S in the MCU ULP subsystem supports the following additional power-save features:

- After the DMA is programmed in PS2 state for I^{2}S transfers, the MCU can switch to PS1 state (M4 processor is turned off) while the I^{2}S controller continues with the data transfer
- In PS1 state (ULP Peripheral mode) the I^{2}S controller completes the data transfer and, triggered by the Peripheral Interrupt, shifts to the PS2 active state.

5.6.1.4 Quadrature Encoder Interface (QEI)

- Tracks encoder wheel position
- Programmable for 1x, 2x, or 4x position counting. Increments/decrements depending on direction.
- Index counter for revolution counting
- Velocity capture using built-in timer
- Supports position counter reset for rollover/underflow or index pulse
- Position, index, and velocity compare registers with interrupts
- Supports logically swapping the A and B inputs
- Accepts decoded signal inputs (clock and direction) in timer mode

5.6.1.5 Motor Control PWM (MCPWM)

- Part of the MCU HP peripheral subsystem
- Supports up to eight PWM outputs with four duty cycle generators, with PWM outputs designed to be used in pairs
- Complementary and independent output modes are supported
- Dead time insertion in complementary mode
- Manual override option for PWM output pins. Output pin polarity is programmable
- Supports generation of interrupt for different events
- Supports two hardware fault input pins
- Special event trigger for synchronizing analog-to-digital conversions

5.6.1.6 Synchronous Serial Interface (SSI) Primary

- Up to two Synchronous Serial Interface (SSI) primaries
- The SSI_MST provides an option to connect up to four secondaries and supports single, dual, and quad modes.
- The SSI_ULP supports single-bit mode and can be connected to only one secondary
- Programmable receive sampling delay

In addition to the above features, the SSI primaries reduce the load on the M4 processor by supporting the features below:

- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events
- Programmable division factor for generating SSI clock out

The SSI_ULP supports the following additional power-save features:

- After the DMA is programmed in the PS2 state for SSI transfers, the MCU can switch to PS1 state (M4 processor is turned off) while the SSI primary continues with the data transfer.
- In PS1 state (ULP Peripheral mode), the SSI primary completes the data transfer and, triggered by the peripheral interrupt, shifts to the PS2 active state.

5.6.1.7 Synchronous Serial Interface (SSI) Secondary

- Support for SSI Primaries which comply with Motorola SPI, TI SSP and National Semiconductors Microwire protocols
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Supports generation of interrupt for different events

5.6.1.8 Secure Digital I/O (SDIO) Secondary Interface

- Full throughput with SDIO 1.2 as well as with SDIO 2.0
- Supports up to 50 MHz
- Supports full-speed and high speed modes
- Supports SD-1 bit and SD-4 bit modes
- Supports only function 1
- Supports interrupt for host abort, CRC Error, CMD52 and CMD53 interrupts
- Supports single as well as multiple block transfers for CMD53 access
- Supports CMD52 while CMD53 data transfer is in progress
- Supports CMD52 Abort
- Supports Read Wait
- Does not support Suspend/Resume
- Provides primary and secondary interfaces on system side AHB Bus
- Supports CIS memory configuration during boot up
- Supports system soft reset from host

There is a constraint on the minimum SoC clock relative to SDIO clock. SoC clock has to be a minimum half of SDIO clock. This constraint is due to the synchronization mechanism used between the SoC clock domain and SDIO clock domain.

5.6.1.9 HSPI Secondary

- 4-pin serial interface
- Supports 8-bit and 32-bit data
- Supports frequencies up to 100 MHz
- SPI clock can be at the max 4 times higher than AHB clock
- Support for DMA
- Supports AHB interface for accessing data from SoC
- Supports system soft reset from external host

5.6.1.10 State Configurable Timer (SCT)

- Supports 1 configurable input and 2 output signals.
- Supports two 16-bit configuration timer
- The timers accept clocks or events as input tick.
- Wide range of features like starting the counter, stopping the counter, continuing the counter from the stopped value, halt, increment the counter and capturing the events
- Support for PWM signals as output with any cycle/pulse length and superimpose a waveform on the PWM signal.
- Support for DMA flow control
- Generates interrupt for different events

5.6.1.11 CRC Accelerator

- Part of MCU HP peripheral subsystem
- Support for one 32 bit polynomials
- Support for one 32 bit stream-in data widths
- Supports DMA flow control

5.6.1.12 Enhanced GPIO (EGPIO)

- Two EGPIO controllers - one in MCU HP and MCU ULP subsystem
- Supports various alternate functions like set, clear, toggle on all the pins
- Option to program Mode for each GPIO pin independently
- Supports edge and level detection based interrupt generation

5.6.1.13 Generic SPI (GSPI) Primary

- Part of MCU HP peripheral subsystem
- Supports single bit SPI primary mode.
- Support for Mode-0 and Mode-3 (Motorola)
- Supports both Full speed and High speed modes
- SPI clock out is programmable to meet required baud rates
- Support for full duplex mode
- Connect up to three SPI peripheral devices
- Support byte swapping during read and write operation
- Support up to 32 KB of read data from a SPI device in a single read operation
- Programmable FIFO thresholds with maximum FIFO depth of 16 and support for DMA
- Generates interrupt for different events

5.6.1.14 Hardware Random Number Generator (HRNG)

- Part of MCU HP peripheral subsystem
- Supports 32-bit True Random Number Generator
- Supports 32-bit Pseudo Random Number Generator
- Option to selectively enable these random number generators

5.6.1.15 General Purpose DMA (GPDMA)

- Two primaries interface over AHB bus
- Supports 8 channels
- Linked-list based descriptors
- Has two AHB primaries for parallel data transfer. The Primary is selectable for descriptor fetch, per channel and per source and destination
- Dynamically configurable FIFO for 8 channels
- Programmable source and destination burst sizes
- Programmable beats per bursts
- Source and Destination address alignment
- Programmable Transfer Types: Memory to Memory, Memory to Peripheral and Peripheral to Memory
- Programmable priority encoded arbiter
- Supports generation of interrupt for different events
- Support for DMA squash
- Support for memory Zero Fill and One Fill

5.6.1.16 Micro DMA (μDMA)

- Supports 32 channels
- Each DMA channel has dedicated handshake signals and programmable priority level
- Supported transfer types: memory-to-memory, memory-to-peripheral, peripheral-to-memory
- Supports multiple DMA cycle types and transfer data widths
- Programmable number of transfers in a single DMA cycle
- Average throughput is four cycles per one word reading
- Each DMA channel can access a primary, and alternate, channel control data structure
- Supports generation of interrupt for different events
- Support half-word (16 bit) and word (32 bit) size transfers

5.6.1.17 eFuse Controller

- Provides 32 bytes eFuse as one-time programmable memory locations
- Supports eFuse programming and read operations
- Supports memory mapped and FSM based read operation

5.6.1.18 SPI Flash Controllers

A serial flash device is a non-volatile memory that can be electrically erased and reprogrammed. It is used for storing executable code or data readily available for M4/NWP processor. After power-up, the executable code is read by the M4/NWP processor from the serial flash and then executed. The code in the serial flash is write-protected and cannot be altered.

Serial flash memories are controlled by many kinds of serial interface protocols (SPI, SSP, SSI, SMI, etc.). The SiWG917M supports SPI based flash. SPI flash memory is a secondary device.

To access it, dedicated QSPI flash controller is present which is Primary.

SiWG917M has a QSPI flash controller which has 2/4/8 - wired interface for serial access of data from flash. The QSPI controller can be used in either single, dual, quad or octal modes with support for SDR to read the processor's instructions and for data transfers to/from the flash. The controller supports inline decryption of encrypted instructions read from the flash before they are passed on to the M4/NWP processor's instruction cache. Instructions are read using the Direct Access mode while data transfers use the Indirect Access mode in case of the flash. The QSPI controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with flash ICs. The Direct Access mode is used to read instructions and data directly from flash. It supports inline decryption using an AES engine for the instructions or data transfer with flash. The Indirect Access mode is used to read and write data/instructions from flash. The two modes - Direct Access and Indirect Access - can be used to access the same flash or two different flashes (using CSN0 and CSN1) at a time by enabling hardware controlled mode. The QSPI controllers have independent AHB secondaries for these modes of access.

SiWG917M can use a single common SPI flash for executing instructions by both NWP and M4 processors. Each processor has dedicated QSPI flash controller. Dynamic arbitration has taken place between two controllers without any processor intervention for executing instructions from common flash. Arbitration multiplexes the two SPI interfaces into a single SPI interface connected to the flash. The flash memory is partitioned into two parts dedicated to each processor respectively.

There are two flash configurations available, as shown in the figures below.

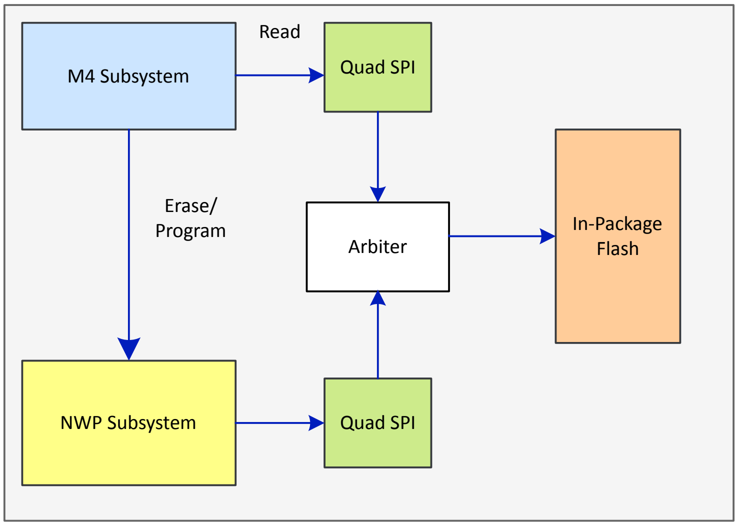


Figure 5.3. Common Flash Configuration

In the common flash configuration, flash is shared between both NWP and M4 processors. flash Initialization, configuration, program and erase can be done only by NWP processor. M4 processor can do only instruction fetching in direct access mode. Flash memory is divided into two regions, one each for the processor. M4 can only read M4 assigned memory region. NWP has no restriction and it can access complete flash memory.

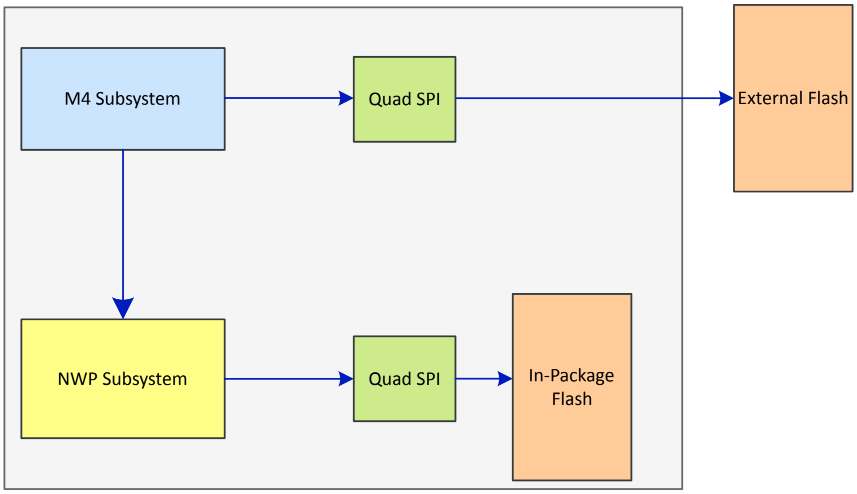


Figure 5.4. Dual Independent Flash Configuration

In the dual flash configuration, each processor has its own dedicated flash memory. In this configuration, M4 can access complete flash memory. M4 can perform flash initialization, configuration, programming and erase.

The features of the SPI flash primary controller are given below.

- Supports Single/Dual/Quad/Octal (S/D/Q/O) modes for reading M4/NWP processor instructions and data transfers to/from flash.
- Support for SPI Mode-0 and Mode-3
- Support for SDR mode flash

- Supports both 8 and 16-bit flash commands.
- Support both 24 and 32-bit addressing modes
- Supports inline decryption (AES) in XTS/CTR mode with 128-bit and 256-bit key sizes while reading encrypted instructions from the flash
- Supports up to two flashes connected to CSN0 and CSN1
- Direct Access Mode:
  - Instructions are read from flash using the Direct Access mode which does not need any processor involvement after the initial configuration of the controller. The read command used for this mode is programmable depending on the flash used.
  - Direct Access mode supports Wrap / Incremental / Single read operations.
  - Supports prefetch option - enabling this option makes the SPI controller prefetch the next instruction before the request is posted on the internal AHB bus. If the address for the next instruction is different from the prefetch address, the instruction is scrapped.
  - Supports continuous fetch option to reduce instruction fetch delay from flash - this option makes the SPI controller to post the Command and Address only once on the bus to read contiguous instructions by controlling only the CSN.
  - Supports programmable CSN high time.
- Indirect Access Mode:
  - Configuration of flash and reading/writing data from/to the flash uses the Indirect Access mode which requires the M4/NWP processor to program the SPI flash controller for each access.
  - Supports reading of up to 32 KB of data from flash in a single read operation.
  - In addition to 24 and 32-bit addressing, the SPI controller supports 9, 10 and 16-bit addressing in this mode.
- Common flash mode - flash can be accessed by both MCU and NWP simultaneously
- Clock Configuration
  - Support for selection of source clock between AHB bus clock and PLL clock.
  - Support for even division factors up to 64 to generate the SPI clock from the source clock.
- Transmission of Extra-byte after the address phase is supported. The contents of this byte are programmable. There is also an option to only transmit the first nibble of the extra byte and maintain a Hi-z on the bus for the next nibble.
- Each phase of a Read operation (Command, Address, Dummy Byte, Extra Byte, Read Data) can be in any of the S/D/Q/O modes depending on the flash requirements.
- The number of dummy bytes is programmable and can be programmed as per the instruction and the mode of operation.
- Supports DMA flow control and programmable FIFO thresholds
- Supports interrupt generation based on different events
- Supports dual flash mode - reading of data from two flashes simultaneously
- Supports flash Write Protect

The SPI controller in the MCU has been designed with programmable options for most of the single and multi-bit operations so that it can interface with flash ICs from multiple vendors.

Note: The QSPI controller interface is available only for interface to serial flash devices. It cannot be used as a general SPI peripheral.

5.6.1.19 SPI PSRAM Controllers

For applications that require additional RAM, an additional external RAM can be added in the form of pseudo static RAM (PSRAM). The PSRAM is an additional RAM of size that is selected e.g. 2/4/8/16 MB.

PSRAM memory is a QSPI secondary device. M4 microcontroller communicates with the PSRAM through dedicated Quad SPI Primary controller.

SiWG917M has SPI PSRAM controller which has 2/4/8 - wired interface for serial access of data from PSRAM. Dedicated SPI controllers are present for PSRAM. It can be used in either Single, Dual or Quad modes with support for SDR to read the M4 processor's instructions and for data transfers to/from the PSRAM. The controller supports inline decryption of encrypted instructions read from the PSRAM before they are passed on to the M4 processor's Instruction Cache. The SPI controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with PSRAM ICs. The Direct Access mode is used to read instructions and read/write data directly to/from PSRAM. It supports inline decryption using an AES engine for the instructions or data transfer with PSRAM. The Indirect Access mode is used to read and write data/instructions from PSRAM. The two modes - Direct Access and Indirect Access - can be used to access the same PSRAM or two different PSRAM (using CSN0 and CSN1) at a time by enabling hardware controlled mode. The SPI controllers have independent AHB secondaries for these modes of access.

The features of SPI PSRAM Primary controller is given below.

- Supports Single/Dual/Quad (S/D/Q/O) modes for reading M4 processor instructions and data transfers to/from PSRAM.
- Support for SPI Mode-0.
- Supports full duplex mode in single-bit SPI mode. Support for HOST SPI secondary interface.
- Support for SDR mode PSRAMs
- Supports both 8 and 16-bit PSRAM commands.
- Support both 24 and 32-bit addressing modes
- Supports only AES CTR mode encryption and decryption of PSRAM data with 128-bit and 256-bit key sizes
- Supports up to two PSRAMs connected to CSN0 and CSN1
- Supports Direct mode write
- Supports semi direct mode read operation for PSRAM
- Direct Access Mode:
  - Data transfer from/to PSRAM using the Direct Access mode which does not need any M4 processor involvement after the initial configuration of the controller. The read/write command used for this mode is programmable depending on the PSRAM used.
  - Direct Access mode supports Wrap / Incremental / Single read operations.
  - Supports prefetch option - enabling this option makes the SPI controller prefetch the next instruction before the request is posted on the internal AHB bus. If the address for the next instruction is different from the prefetch address, the instruction is scrapped.
  - Supports continuous fetch option to reduce instruction fetch delay from PSRAM - this option makes the SPI controller to post the Command and Address only once on the bus to read contiguous instructions by controlling only the CSN.
  - Supports programmable CSN high time.
- Indirect Access Mode:
  - Configuration of PSRAM and reading/writing data from/to the PSRAM uses the Indirect Access mode which requires the M4 processor to program the SPI controller for each access.
  - Supports reading of up to 32 KB bytes of data from PSRAM in a single read operation.
  - In addition to 24 and 32-bit addressing, the SPI controller supports 9, 10 and 16-bit addressing in this mode.
- Clock Configuration
  - Support for selection of source clock between AHB bus clock and PLL clock.
  - Support for even division factors up to 64 to generate the SPI clock from the source clock.
- Each phase of a Read operation (Command, Address, Dummy Byte, Extra Byte, Read Data) can be in any of the S/D/Q/O modes depending on the PSRAM requirements.
- The number of dummy bytes is programmable and can be programmed as per the instruction and the mode of operation.
- Supports DMA flow control and programmable FIFO thresholds
- Supports configurable memory ranges on which we can save code in encrypted form and the execution will happen with inline decryption.
- Supports dual PSRAM mode - reading and writing from/to two PSRAM simultaneously
- Supports interrupt generation based on different events

The SPI controllers in the MCU have been designed with programmable options for most of the single and multi-bit operations so that it can interface with PSRAM ICs from multiple vendors.

5.6.1.20 FLASH and PSRAM Supply Connections

There are four unique configuration options for flash and PSRAM connection to the SiWG917

1. In-package Flash/PSRAM
2. Only external Flash
3. In-package PSRAM and External Flash
4. In-package Flash and External PSRAM

For these combinations, either the in-package Flash LDO supply or an external supply can be used. The flash supply, PSRAM supply and I/O supply configurations are different for each case.

Table 5.10. PSRAM and Flash Package Options

Mode	Configuration	GPIO pins	Suggested OPNs
Mode1	In-package Flash	0:5	SiWG917Y110LGNBA, SiWG917Y111MGNBA, SiWG917Y110LGABA, SiWG917Y111MGABA
Mode2	In-package PSRAM, on-module Flash	0:5 (PSRAM), 46:51 (Flash, GPIOs Reserved for on-module Flash usage only)	SiWG917Y121MGNBA, SiWG917Y121MGABA
Mode3	N/A	N/A	Applicable only to SiWG917M IC
Mode4	N/A	N/A	Applicable only to SiWG917M IC
Mode5	In-package Flash, External PSRAM	0:5 (NWP Flash), 46:51 (PSRAM, GPIOs Reserved for PSRAM usage only) OR 52:57 (PSRAM, GPIOs Reserved for PSRAM usage only)	SiWG917Y110LGNBA, SiWG917Y111MGNBA, SiWG917Y110LGABA, SiWG917Y111MGABA
Mode6	In-package Flash, External Flash	0:5 (NWP Flash), 46:51 (M4 Flash, GPIOs Reserved for Flash usage only)	SiWG917Y110LGNBA, SiWG917Y111MGNBA, SiWG917Y110LGABA, SiWG917Y111MGABA

Examples of supported flash and PSRAM devices are given in Table 5.11 Flash on page 40 and Table 5.12 PSRAM on page 40. For the latest up-to-date list of supported devices and additional modes of operation, please refer to AN1494: SiWx917 External Flash and PSRAM Application Note.

Note: GPIOs 46-51 and GPIOs 52-57 are reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO. GPIOs 0-5 are internal only and not exposed on the module.

Table 5.11. Flash

S.No.	Vendor	Part #	Flash Density (in Mbit)	Vcc	Bus Width
1	GigaDevice	GD25LE32E	32	1.65 to 2.0 V	1/2/4-bit
2	GigaDevice	GD25LE64E	64	1.65 to 2.0 V	1/2/4-bit
3	Macronix	MX25R3235F	32	1.65 to 3.6 V	1/2/4-bit
4	Macronix	MX25U3235F	32	1.65 to 2.0 V	1/2/4-bit
5	Macronix	MX25R8035F	8	1.65 to 3.6 V	1/2/4-bit
6	Macronix	MX25U8033F	8	1.65 to 2.0 V	1/2/4-bit

Table 5.12. PSRAM

S.No.	Vendor	Part #	PSRAM Density (in Mbit)	Vcc	Bus Width
1	AP memory	APS1604M-SQR	16	1.65 to 1.95 V	1/2/4-bit
2	AP memory	APS6404L-SQRH	64	1.65 to 1.95 V	1/2/4-bit
3	AP memory	APS6404L-3SQR-ZR	64	2.7 to 3.6 V	1/2/4- bit
4	AP memory	APS1604M-3SQR-ZR	16	2.7 to 3.6 V	1/2/4 -bit

Table 5.13. Estimated Deepsleep/DTIMs Current with PSRAM for Different Input Supply Options

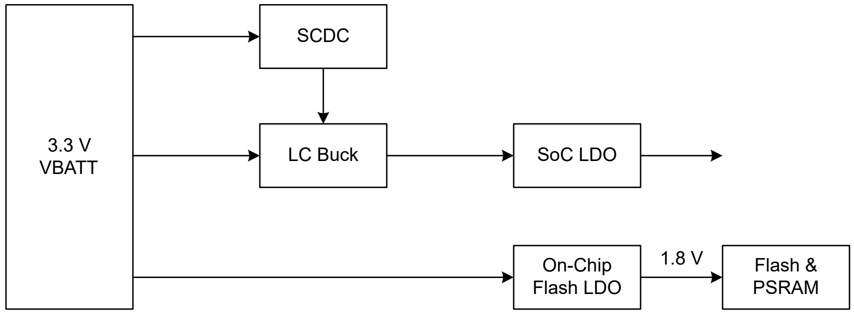
Options	Buck	SoC LDO	Flash LDO / PSRAM	Description	Estimated Deepsleep Current with PSRAM (for VBATT = 3.3 V)	Estimated DTIM-10 Standby Current with PSRAM (for VBATT = 3.3 V)	Estimated DTIM-3 Standby Current with PSRAM (for VBATT = 3.3 V)
1	In-package	In-package	In-package	Single VBATT supply is connected to Chip VBATT to be connected to LC Buck input and LC Buck output is 1.45 V LC Buck output (1.45 V) is connected to SoC LDO and its output is 1.05 V VBATT input is connected to Flash LDO and its output is 1.8 V In deep sleep mode: Keep LC buck in PFM mode, and SoC LDO output at 0.9 V	350 uA	390 uA	435 uA
2	In-package	In-package	External	VBATT to be connected to LC Buck input, LC Buck output is 1.45 V Connect external 1.8 V supply to PSRAM and IO supplies. Connect on-chip Flash LDO to in-package flash In deep sleep mode: Program Buck output as 0.9 V and keep SoC LDO in Bypass mode (SoC LDO output is 0.9 V) Switch-off on-chip Flash LDO	225 uA	265 uA	310 uA
3	External	In-package	External	Connect external BUCK output (1.45 V) to SoC LDO, and its output is 1.05 V Connect external 1.8 V supply to PSRAM, flash and IOs In deep sleep mode: Keep SoC LDO output to 0.9 V	75 uA	115 uA	160 uA

Op-tions	Buck	SoC LDO	Flash LDO / PSRAM	Description	Estimated Deepsleep Current with PSRAM (for VBATT = 3.3 V)	Estimated DTIM-10 Standby Current with PSRAM (for VBATT = 3.3 V)	Estimated DTIM-3 Standby Current with PSRAM (for VBATT = 3.3 V)
4*	In-package	In-package	External with pull up on CS pin	VBATT to be connected to LC Buck input, LC Buck output is 1.45 V Connect external 1.8 V supply to PSRAM and IOs. Connect on-chip Flash LDO to in-package flash Connect weak pull up on external PSRAM CS pin In deep sleep mode: Switch off on-chip LC Buck, Flash LDO, and SoC LDO	40 uA + weak pull up current	80 uA + weak pull up current	125 uA + weak pull up current
Note: *Option4 is recommended to achieve minimum deep sleep currents while retaining the PSRAM contents.							

Options 1 through 4 are shown in the following diagrams. Different blocks shown in the diagrams have the following purposes:

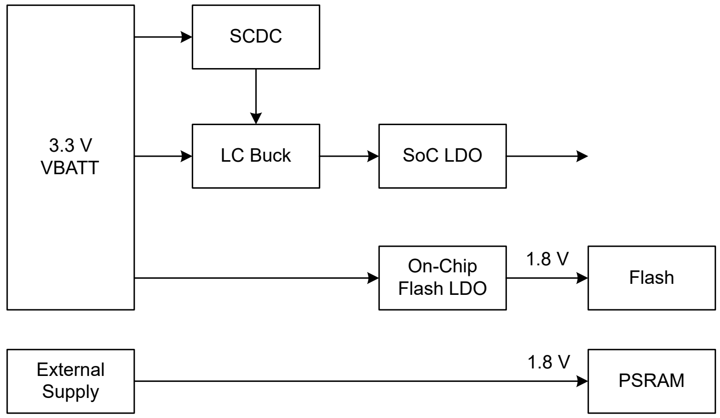
- VBATT - 3.3 V supply pin.
- SCDC - This block generates a 1.05 V voltage rail which supplies the sleep state machine, always-ON domains and other internal digital blocks.
- SoC LDO - This block generates the supply voltage for many of the digital blocks on chip. Output varies based on power state.
- Flash LDO - This block generates a 1.8 V supply for in-package and/or external flash and PSRAM.
- LC Buck - This block generates a 1.45 V supply rail for RF circuits and the SoC LDO.

Option 1: All supplies are In-package



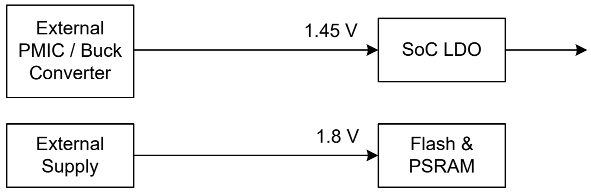
In this configuration, the on-chip LC Buck converter powers the SoC LDO, and the on-chip Flash LDO is used as a 1.8 V supply to both flash and PSRAM.

Option 2: PSRAM supply is External and other supplies are In-package



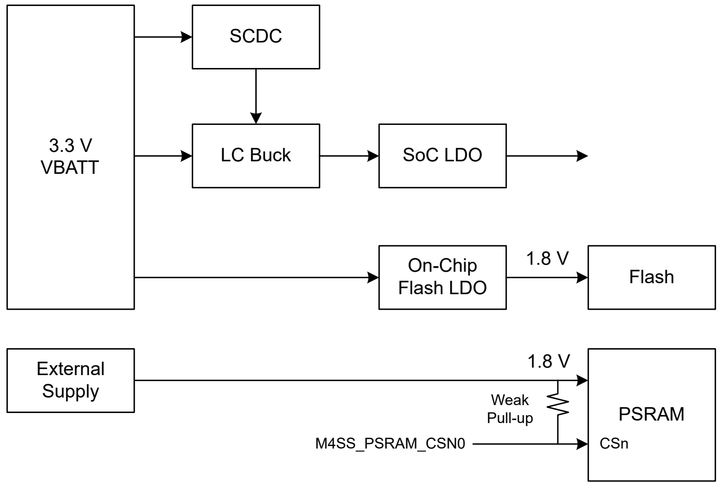
In this configuration, the on-chip LC Buck converter powers the SoC LDO, the on-chip Flash LDO is used as a 1.8 V supply to flash, and an external 1.8 V supply is connected to the PSRAM.

Option 3: External Buck and flash / PSRAM supplies



In this configuration, an external PMIC or Buck DCDC converter powers the SoC LDO,and an external 1.8 V supply is connected to flash and PSRAM.

Option 4: PSRAM supply is External with weak pull-up on CS pin and other supplies are on-chip



In this configuration, the on-chip LC Buck converter powers the SoC LDO, the on-chip Flash LDO is used as a 1.8 V supply to flash, and an external 1.8 V supply is connected to the PSRAM. Additionally the PSRAM chip select (CSn) has an external weak pull-up resistor to the supply.

5.6.1.21 Watchdog Timer

The WatchDog Timer is used to generate an interrupt on timeout and a reset in case of system failure which can be caused by an external event like ESD pulse or due to a software failure. Also the Interrupt can be used as a Wakeup source for transitioning from SLEEP/STANDBY to ACTIVE states.

- Independent watchdog timer.
- Interrupt is generated before the system reset is applied which can be used as a wakeup source.
- Generates reset upon Lockup indication from M4 processor.
- Configurable low frequency clock (RC and Xtal).
- Configurable timeout period.
- Able to operate when CPU is in SLEEP state during power-save applications
- Individually controllable power domain for low-power applications.

5.6.1.22 Calendar

Calendar block acts a RTC with time in seconds, minutes, hours, days, months, years and centuries. The real-time can also be read through APB with accuracy less than a second by reading the millisecond count value and further less also by reading the number of counts of APB clock in 1 millisecond of RTC clock. Accuracy is high.

- Calendar block can provide a seconds trigger and also a msec trigger.
- Calendar block takes care of no. of days in each month and also leap years. It can count up to 4 centuries.
- Real time is readable through APB and also programmable through APB.

5.6.1.23 General Purpose Timers

The MCU Timer block supports four 32 bit timers, which can be used to generate various timing events for the software. Each of the four timers can be independently programmed to work in periodic or one-shot mode and can be configured either as a microsecond timer or as a counter.

- Four independent 32 bit timers
- Supports per timer enable and disable.
- Option to configure each timer as a 32 bit counter or 32 bit microsecond timer.
- Supports 1 µs mode and 256 µs modes per timer.
- Accounts for integral and fractional value of the time units programmed.
- Microsecond timer supports two modes:
  - 1 microsecond mode: The time unit is 1 µs. Number of microseconds required to be counted has to be programmed.
  - 256 microsecond mode: The time unit is 256 µs. Number of 256 µs units required to be counted has to be programmed. This is useful when the timer is being used for counting large time values and microsecond based tracking not required.
- One shot and periodic modes per timer.
- Option to interrupt the M4 processor on timeout.

5.6.1.24 Secure Storage

The Block is used for storing configuration values with data protection feature.

- MCU has 3 set's for storage block
  - First chunk is 64 bits
  - Second chunk is 64 bits
  - Third Chunk is 128 bits
- Each chunk is a power domain.
- Secure mode is available for first and second Chunk.
- Storage space can be used for storing Configuration values

5.6.1.25 MVP

The Matrix Vector Processor (MVP) offloads floating point operations, particularly matrixed complex floating point multiplies and additions. The MVP was designed to offload the major computations of the Angle-of-Arrival (AoA) MUSIC algorithm, although the architecture can generally be used to offload other heavily floating-point computational problems such as Machine Learning (ML), Eigen, or BLAS acceleration.

- Instruction Set Architecture (ISA)
  - General purpose instruction set tailored towards algorithms built out of ALU, loop, and load/store instructions
  - Enables many high-level array functions, e.g.:
    - Matrix multiplication
    - Element-wise matrix multiplication
    - Matrix addition
    - Power series generation
    - Convolution
  - Program flexibility allows efficient iteration over N-dimensional array elements, including in-place processing of special matrix views:
    - Element-wise negate / conjugate
    - Transpose / adjoint / reverse
    - Matrix blocks (i.e., rectangular parts of matrix)
    - Matrix slices (i.e., taking rows, columns, or elements uniformly spaced within a matrix)
    - Row-major or column-major ordering
- Arithmetic Logic Unit (ALU)
  - Support for floating point real and complex numbers
    - Partial integer input support
      - Floating-point output operands, interpreted as 16-bit real or 32-bit complex number (16-bit real and 16-bit imaginary)
      - Register bank to hold all input/output operands
    - Includes 8 registers for temporary storage and/or accumulation
  - Hardware to support 1 complex floating point multiply-accumulate (MAC) per cycle
    - Four single-precision floating-point multipliers
    - Four single-precision floating-point adders
    - 6x performance of Cortex M33 FMAC operations
  - Operations supported at a rate of one operation per cycle:
    - Complex addition, multiplication, and MAC operations
    - Parallel real multiplication and MAC
    - Parallel real addition
    - Sum of 4 reals
    - Squared-magnitude of complex/real
    - Integer-to-float conversion
    - Conditional computation
  - Input transformations (per real/complex part of each input)
    - Negation (complex conjugate)
    - Zero-masking (real/imaginary part decomposition)
- Load/Store Unit (LSU)
  - Controls data streaming from memory-to-ALU and vice versa
  - Pipelined architecture to support two simultaneous 32-bit memory reads and one 32-bit memory write per cycle
  - Supports signed / unsigned 8-bit integer conversion for both load and store operations
  - Memory Access Ports
    - Used by load / store unit for handling accesses to external (system) memory addresses
    - Three independent 32-bit AHB manager ports for supporting 2 read channels and 1 write channel simultaneously
- Sequencer
  - Coordinates all MVP blocks to execute a sequence of instructions provided via the programming interface
  - Handles array iteration according to instruction sequence and static array configuration
  - Handles loop iteration according to instruction sequence and static loop configuration

- Programming interface
  - Control registers for starting / stopping engine
  - Status registers about ongoing and finished instruction sequences
    - Fault status
    - Useful information for debug
  - Breakpoint and stepping controls for debug
  - Interrupts and faults
    - Instruction sequence completion
    - Bus faults
    - Loop faults
    - Array faults
  - Array configuration registers
  - Loop configuration registers
  - Instruction queue registers
    - Array iteration
    - ALU operations
    - Looping

5.6.1.26 SYSRTC

The SYSRTC (System Real Time Clock) is a highly configurable RTC capable of serving multiple cores. It contains up to 2 groups, where the number of capture and compare channels within each group is parametrized individually. Each group has its own interrupt and configuration registers. The main idea is to save power by letting all groups share a single counter.

- 32-bit counter
- 32 kHz / 1 kHz intended operation
- Low energy mode and wake-up
- Up to 2 groups
- 1-2 compare channels per group
- 0-1 capture channel per group
- Optional debug halting
- Optional alternate interrupt/wake-up per group
- Software Reset

5.6.2 Analog Peripherals and Interfaces

5.6.2.1 Analog to Digital Converter (ADC)

The ADC provides up to 12 bits of resolution at 2.5 Msps

- 12 bit ADC Output in 2's complement representation
- Programmable clock divider for ADC_CLK
- GPIOs in High Power mode for ADC Operation
  - Signal Ended Mode
    - 18 External configuration selection
    - 5 Internal configuration selection
      - Internal Temperature sensor
      - 3 Opamp Outputs
      - DAC output for internal reference
  - Differential Mode
    - 9 external differential mode configuration selection
    - 4 Internal configuration selection.
      - 3 Opamp Outputs
      - DAC output for internal reference
- GPIOs in Low Power mode for ADC Operation
  - Signal Ended Mode
    - 12 External configuration selection.
  - Differential Mode
    - 6 external differential mode configuration selection.
- 10 MHz to 32 KHz allowed ADC_CLK
- Configurable DMA to support 16 channels for storing AUXADC data in ULP SRAM.
- Measurement range 0 to AUXADC_VREF (1.8 V to 3.3 V)

The ADC has five modes of operation:

- Single ended input with noise averaging
- Single ended input without noise averaging
- Differential input with noise averaging
- Differential input without noise averaging
- Shutdown mode

5.6.2.2 Digital to Analog Converter (DAC)

DAC can take 10 bit digital inputs and convert them into analog voltage within range 5*vdd/36 to 31*vdd/36. Vdd can vary from 1.8 volts to 3.63 volts.

- 10-bit resolution
- Single ended DAC
- Max sampling frequency is 5 MHz for DAC_CLK
- Supports Operational mode and Shutdown modes
- DAC performance not guaranteed below -20 °C

5.6.2.3 OPAMP

- 3 general purpose Operational Amplifiers (OPAMP) offering rail-to-rail inputs and outputs.
- Each of the three opamps has 2 inputs (inp, inn) and 1 output.
- opamps can take inputs from GPIOs and their outputs can be seen on GPIOs
- configured in either low power mode or high power mode
- opamps can be configured as:
  - Unity gain amplifier
  - Trans-Impedance Amplifier(TIA)
  - Non-inverting Programmable Gain Amplifier (PGA)
  - Inverting Programmable Gain Amplifier
  - Non-inverting Programmable hysteresis comparator
  - Inverting Programmable hysteresis comparator
  - Cascaded Non-Inverting PGA
  - Cascaded Inverting PGA
  - Two opamps Differential Amplifier
  - Instrumentation Amplifier

5.6.2.4 Analog Comparators

Analog comparators peripheral consists of two analog comparators, a reference buffer, a scaler and a resistor bank. Both comparators can take inputs from GPIOs.

The comparator compares analog inputs p and n to produce a digital output, cmp_out according to:

p > n, cmp_out = 1

p < n, cmp_out = 0

The following cases of comparison are possible

- Compare external pin inputs
- Compare external pin input to internal voltages.
- Compare internal voltages.

The inputs of 2 comparators can be programmed independently. The reference buffer, scaler and resistor bank are shared between the two comparators and can be enabled only when at least one of the comparators is enabled.

5.6.2.5 Temperature Sensor

An BJT based temperature sensor is included on the device.

The BJT based sensor works for a temperature range from -40 °C to 125 °C across the supply range 1.8 V to 3.63 V. It outputs a digital word with a resolution of nearly 1 degree C. The conversion time is 2 clock cycles of ADC after turning ON the temperature sensor.

The temperature reading of the sensor is accessed by configuring the ADC inputs to temperature sensor.

5.7 Bootloader

The Bootloader controls the initial operation of the device after any form of reset. The Bootloader supports Flash programming and initial startup of the application code. Bootloader supports following features:

- Two Bootloaders - Security Bootloader and Application Bootloader
- Support for ISP (In-System Programming) through multiple interfaces - UART, SPI and SDIO
- Auto-detection of ISP interface. The host interfaces are the external peripheral interfaces over which Bootloader can receive commands or firmware when in ISP mode. The Bootloader supports UART, SPI and SDIO interfaces. Bootloader in ISP mode waits for data on any of these interfaces and can automatically detect which interface the data is being received.
- Support for secure boot
- Support for secure firmware upgrade using PUF based Roots-of-Trust (RoT)
- Anti-rollback protection. This feature prevents the firmware version from being downgraded. A new firmware is allowed to be upgraded only if it is be equal to or greater than the current firmware.
- Secure Key Management and Protection
- Support for different flash protection levels and write-protected Flash
- Encrypted XIP from Flash
- Fail-proof migration of current active firmware to new (update) firmware
- Public key cryptography (digital signature) based authentication

The SiWG917M includes two Bootloaders - Security Bootloader and Application Bootloader. The Security Bootloader runs on the Network Wireless Processor and the Application Bootloader runs on the Cortex M4 processor. On any reset, execution will always start in Security Bootloader, which is responsible for all security features, ISP and firmware upgrades. Once the Security Bootloader finishes its tasks, it enables the Application Bootloader. The Application bootloader will load and execute the application and also execute wakeup sequence on wakeup from sleep.

The following are the sources, which can trigger the Bootloader:

- Primary reset (RESET_N)
- Power on reset (POC_IN)
- Watchdog reset
- Black out monitor
- Reset request through SYSRESETREQn bit in the Cortex-M4 processor
- Wake-up from Sleep

5.8 Security

5.8.1 Security Features

- Secure Boot
- Secure OTA Firmware update
- TRNG: Generates high-entropy random numbers based on RF noise, increasing the effort/time needed to expose secret keys
- Secure Zone
- Secure Key storage : HW device identity and key storage with PUF
- Debug Lock
- Anti Rollback : Firmware downgrade to a lower version is prohibited through OTP to prevent the use of older, potentially vulnerable FW version
- Encrypted XIP from flash with XTS/CTR mode
- Secure Attestation : Allows a device to authenticate its identity using a cryptographically signed token and exchange of secret keys
- Hardware Accelerators: AES128/256/192, SHA256/384/512, HMAC, RNG, CRC, SHA3, AES-GCM/ CMAC, ChaCha-poly
- Software Implementation: RSA and ECC

5.8.2 Secure Boot

Key Features

- Ensures your device runs authentic code in the boot and OTA update to eliminate malware insertion threats
- Secure Immutable Bootloader in ROM.
- Authenticates signatures of all other SW using public keys.
- Protocol and Application flash images can be encrypted with separate keys.

On reset, the Security Bootloader configures the hardware based on the configuration present in the eFuse. It also passes the required information from the eFuse to the Application Bootloader. The Security Bootloader validates the integrity and authenticity of the firmware in the Flash and invokes the Application Bootloader. It detects and prevents execution of unauthorized software during the boot sequence. The Bootloader uses public & private key based digital signatures to recognize authentic software. The Security Bootloader provides provision for inline execution (XIP) of encrypted firmware from Flash. The Bootloader provides 3 flash protection levels which can be used to secure different sections of the Flash for different purposes:

- Protection level 1: Stored at manufacturing, not allowed to modify by the Security Bootloader
- Protection level 2: Allowed to modify by the Bootloader only, usually used to maintain secure information used/consumed by Bootloader
- Protection level 3: Allowed to modify by the Bootloader only, usually used to maintain protected firmware images. (Minimum 8 MB of flash is required for complete NWP image protection. For 4 MB flash OPNs, only partial protection is available for NWP image).

The protection levels are written to Flash during the manufacturing process. The write-protection feature prevents the application program from changing the Flash protection levels.

The Security configurations can be enabled or disabled during the manufacturing process.

5.8.3 Encrypted XiP

The Security Bootloader provides provision for inline execution (XIP) of encrypted firmware from flash.

- Execute SW directly from flash instead of copying it into RAM
- Images are saved in encrypted format and decrypted using device-specific PUF intrinsic keys while executing
- In-line decryption based on-the-fly AES engine (based on PUF keys)
- XTS/CTR modes supported

5.8.4 Secure Firmware Upgrade

Secure firmware upgrade via host interface :

The secure firmware upgrade feature of the Bootloader checks the authenticity of the new firmware image along with its integrity. The Bootloader automatically detects the host interface in use and configures the host interface hardware accordingly. The Bootloader updates the image only after successfully validating the authenticity and integrity of the image. It prevents downgrade to a lower version of firmware using the anti-rollback feature, if it is enabled. The Bootloader also supports transparent migration to a wirelessly updated image and protection against failures by providing recovery mechanisms.

Secure OTA :

- Secure OTA update to eliminate malware insertion threats.
- Wireless and Application image transfer over the air.
- Network Wireless processor authenticates the signatures of OTA image using public keys
- Bootloader copies the OTA image to primary firmware location upon successful authentication .

5.8.5 Secure Zone

Key Features

- Secure Zone is a hardware enforced isolation between the NWP core from the Application (M4) core.
- No access to the:
  - NWP processor
  - NWP address space memory (except misc-registers that are used for bootloader command exchanges)
  - NWP HW registers from external peripherals and host interfaces
- Secure zone protects NWP internal keys (for example, secure boot keys), customer application keys, and certificates residing in the NWP by restricting direct access from the application M4 core.
- Secure zone can be enabled during the manufacturing process, at the user's discretion, by setting the secure_isolation_enabled OTP/MBR bit

When Secure Zone is enabled, the Host Processor cannot reconfigure interfaces that are controlled by the NWP by default. For instance, ISP interfaces such as UART, SPI, and SDIO will be mutually exclusive between the NWP and M4 when secure zone is enabled. This is because secure zone will not allow Host processor to program the registers (in NWP space) to get control of those interfaces. In such cases, configurations in MBR defines the default ownership of the interface.

5.8.6 In-System Programming (ISP)

In System Programming (ISP) is programming or reprogramming of the flash through a boot loader using UART (GPIO_8 and GPIO_9), SPI (GPIO_25 to GPIO_29), or SDIO (GPIO_25 to GPIO_30) interfaces. This can be done after the part is integrated on the end-user board. The boot loader can be requested to boot in ISP mode by pulling down the JTAG_TDO_SWO pin. This pin has to be left unconnected during reset for the boot loader to bypass ISP and execute the code that is present in flash. ISP mode can be used to reprogram the flash, if the application code uses JTAG pins for functional use. On boot up, if the application code goes into a state where the JTAG interface is not functioning, ISP mode can be used to gain control and to reprogram the flash.

5.8.7 Debug Lock

Key Features

- Debug ports are disabled in HW by default.
- It can be enabled in SW using cryptographically secure host interface commands validated by immutable bootloader
- It allows the device's JTAG ports to be locked and unlocked.

5.9 Debug Support

MCU implements complete hardware debug solution. This provides high system visibility of the M4 processor and memory through either a traditional JTAG port or a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

In Serial Wire Viewer (SWV) mode, a one-bit serial protocol is used and this reduces the number of output signal to one. When combining SWV with Serial-Wire debug protocol, the Text Data Output (TDO) pin normally used for Joint Test Action Group (JTAG) protocol can be shared with SWV.

The Embedded Trace Macrocell (ETM) provides high bandwidth instruction trace via four dedicated trace. The MCU_CLK_OUT frequency must be in the range of 40 MHz to 90 MHz to Instruction trace using ETM component.

5.10 WLAN

- Compliant to single-spatial stream IEEE 802.11 b/g/n/ax with single band (2.4 GHz) support
- Support for 20 MHz channel bandwidth for 802.11n and 802.11ax.
- Operating Modes: Wi-Fi 4 STA, Wi-Fi 6 (802.11ax) STA, Wi-Fi 4 AP, Enterprise STA, Wi-Fi 6 STA + Wi-Fi 4 AP, Wi-Fi STA + BLE
- Wi-Fi 6 Features: Individual Target wake-up time (iTWT), Broadcast TWT (bTWT),SU extended range (ER), DCM (Dual Carrier Modulation), DL MU-MIMO, DL/UL OFDMA, MBSSID, BFRP, Spatial Re-use, BSS Coloring, and NDP feedback up to 4 antennas
- Integrated PA
- Data Rates — 802.11b: up to 11 Mbps; 802.11g: up to 54 Mbps; 802.11n: MCS0 to MCS7; 802.11ax: MCS0 to MCS7
- Operating Frequency Range [MHz]: 2412-2462 (North America, default), 2412-2472 (Europe, and other countries where applicable), 2412-2484 (Japan)

5.10.1 MAC

- Conforms to IEEE 802.11b/g/n/j/ax standards for MAC
- Hardware accelerators for AES
- WPA, WPA2, WPA3 and WMM support
- AMPDU aggregation for high performance
- Firmware downloaded from host based on application
- Hardware accelerators for DH (for WPS) and ECDH

5.10.2 Baseband Processing

- Supports 11b: DSSS for 1, 2 Mbps and CCK for 5.5, 11 Mbps
- Supports all OFDM data rates
  - 802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps
  - 802.11ax, 802.11n: MCS 0 to MCS 7
- High-performance multipath handling in OFDM, DSSS, and CCK modes

5.11 Bluetooth

Key Features

- Transmit power up to +17 dBm with integrated PA
- Receive sensitivity — LE 1 Mbps: -94 dBm, LE 2 Mbps: -91.5 dBm, LR 500 kbps: -101.5 dBm, LR 125 kbps: -105.5 dBm
- Operating Frequency Range: 2.402 GHz - 2.480 GHz
- Supports Bluetooth® Low Energy (LE): High Speed (1 Mbps and 2 Mbps) and Long Range (LE Coded PHYs, 125 kbps and 500 kbps; these are referred to as "LR" throughout this data sheet)
- Extended Advertising
- Extended Advertising scanning
- Periodic Advertising
- Periodic Advertising scanning
- Periodic Advertising list
- Periodic advertising synchronization
- Data length extensions
- LL privacy 1.2
- LE Secure connections
- LE channel selection algorithm 2 (CSA#2)
- LE dual role
- BLE acceptlist
- Two simultaneous BLE connections (2 peripheral or 2 central, or 1 central and 1 peripheral)
- BLE Mesh (4 nodes) for limited switch use case.

5.11.1 MAC

Link Manager

- Creation, modification & release of physical links
- Connection establishment between Link managers of two Bluetooth devices
- Link supervision is implemented in Link Manager
- Link power control is done depending on the inputs from Link Controller
- Enabling & disabling of encryption & decryption on logical links
- AES hardware acceleration

Link Controller

- Encodes and decodes header of BLE packets
- Manages flow control, acknowledgment, re-transmission requests, etc.
- Stores the last packet status for all physical transports
- Indicates the success status of packet transmission to upper layers
- Indicates the link quality to the LMP layer

Device Manager

- Executes HCI Commands
- Controls Scan & Connection processes
- Controls all BLE Device operations except data transport operations
- BLE Controller state transition management
- Anchor point synchronization & management
- Scheduler

5.11.2 Baseband Processing

- Supports BLE 1 Mbps, 2 Mbps and long range 125 kbps, 500 kbps

5.12 RF Transceiver

- The SiWG917 features two highly configurable RF transceivers supporting WLAN 11b/g/n/ax and Bluetooth LE wireless protocols. Both RF transceivers together operating in multiple modes covering High Performance (HP) and Low Power (LP) operations. List of operating modes are given in next section.
- It contains two fully integrated fractional-N frequency synthesizers having reference from internal oscillator with 40 MHz crystal. One of the synthesizer is a low power architecture which also caters single-bit data modulation feature for Bluetooth LE protocols.

5.12.1 Receiver and Transmitter Operating Modes

The available radio operating modes are

- WLAN HP TX - WLAN High-Performance Transmitter
- WLAN HP RX - WLAN High-Performance Receiver
- WLAN LP RX - WLAN Low-Power Receiver
- BLE HP TX - Bluetooth LE High-Performance Transmitter
- BLE HP RX - Bluetooth LE High-Performance Receiver
- BLE LP TX - Bluetooth LE Low-Power Transmitter
- BLE LP RX - Bluetooth LE Low-Power Receiver

Note: All the TX / RX modes are automatically controlled by radio firmware and not individually selectable.

5.13 Embedded Wi-Fi Software

- The wireless software package supports Embedded Wi-Fi (802.11 b/g/n/ax) Client mode, Wi-Fi Access point mode (up to 4 clients), and Enterprise Security in client mode.
- The software package includes complete firmware and application profiles.
- It has a wireless coexistence manager to arbitrate between protocols.

5.13.1 Security

Wireless software supports multiple levels of security capabilities available for the development of IoT devices.

- Accelerators: AES128/256
- WPA/WPA2/WPA3-Personal, WPA/WPA2/WPA3 Enterprise for Client

5.14 Low Power Modes

It supports Ultra-low power consumption with multiple power modes to reduce system energy consumption.

- Voltage and Frequency Scaling
- Deep sleep (ULP) mode with only the sleep timer active – with and without RAM retention
- Wi-Fi standby associated mode with automatic periodic wake-up
- Automatic clock gating of the unused blocks or transit the system from Normal to ULP mode.

5.14.1 ULP Mode

In Ultra Low Power mode, the deep sleep manager has control over the other subsystems and M4 processors and controls their active and sleep states. During deep sleep, the always-on logic domain operates on a lowered supply and a low-frequency clock to reduce power consumption. The ULP mode supports the following wake-up options:

- Timeout wakeup - Exit sleep state after programmed timeout value.
- GPIO Based Wakeup: Exit sleep state when GPIO goes High/Low based on programmed polarity.
- Analog Comparator Based wakeup - Exit sleep state on an event at the analog comparator.
- RTC Timer wakeup - Exit Sleep state on timeout of RTC timer
- WatchDog Interrupt based wakeup - Exit Sleep state upon watchdog interrupt timeout.

5.15 Wireless Subsystem Memory

5.15.1 On-Chip Memory

The Network Wireless Processor has the following memory:

- On-chip SRAM of 480/416/352 KB based on chip configuration
- 448 KB of ROM which holds the Secure primary bootloader, Network Stack, Wireless stacks and security functions
- 16 KB of Instruction cache enabling eXecute In Place (XIP) with quad SPI flash memory.
- eFuse of 1024 bytes (used to store primary boot configuration, security and calibration parameters)

The following memory configuration between MCU and Wireless Sub-system are possible:

Table 5.14. Possible Memory Configurations between MCU and Wireless Sub-system

No.	MCU memory size	Wireless Subsystem memory size	Note
1.	320 KB	352 KB	PS4, PS3, and PS2 power states possible
2.	256 KB	416 KB	Only PS4 and PS3 power state possible For MCU RAM retention, MCU needs to retain complete 320 KB
3.	192 KB	480 KB	Only PS4 and PS3 power state possible For MCU RAM retention, MCU needs to retain complete 320 KB

5.16 Pad Configuration

There are multiple processor sub-systems containing SZP (Secure Zone Processor), MCU HP (High Performance) and MCU ULP (Ultra Low Power) which share these common set of GPIO pads. These GPIO pads are controllable by either SZP, MCU HP or MCU ULP. PAD selection register has to be programmed to control the PAD behavior for each GPIO. The SZP and MCU HPGPIOs are available only in PS4/PS3 power states whereas MCU ULP GPIOs are available in all the power states except sleep modes. The UULP Vbat GPIOs are available in all power states.

The SZP, MCU HP and MCU ULP GPIOs PAD are programmable, multi-voltage (1.8 V, 3.3 V) general purpose, bi-directional I/O buffer with a selectable LVCMOS (Low Voltage CMOS) input or LVCMOS Schmitt trigger input and programmable pull-up/pull-down. In the full-drive mode, this buffer can operate in excess of 100 MHz frequency with 15 pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

The following PAD configurations can be controlled by software for SZP, MCU HP and MCU ULP GPIOs.

- Bi-directional IO capability
- Multi-voltage DVDD capability (1.8 V, 3.3 V)
- Power-on-Start (POS) capable
- Optimized for EMC (low di/dt switching supply noise) with SSO (Simultaneous Switching Output) factor of 8
- Four (4) Programmable output drive strengths (rated 2 mA, 4 mA, 8mA, and 12 mA)
- Selectable output slew-rate (slow / fast)
- Open drain output mode (Logic low or high on input and use OEN as data input)
- LVCMOS/LVTTL compatible input with selectable hysteresis
- Programmable input options (pull-up, pull-down, repeater, or plain input)
- No power sequence requirements, I/Os are tri-stated when core power is not valid (POC control). These are tri-stated even if the system is under reset or in the deep sleep power state.

The following PAD configurations can be controlled by software for UULP Vbat GPIOs.

- Bi-directional IO capability
- Multi-voltage DVDD capability (1.8 V, 3.3 V)

5.17 Interrupts

- Nested vectored interrupt controller (NVIC) for interrupts handling
- Supports 99 interrupts
- Flexible exception and interrupt management
- Nested exception/interrupt support
- Vectored exception/interrupt entry
- Interrupt configurations, prioritization, and interrupt masking

6. Pinout and Pin Description

6.1 Pin Diagram

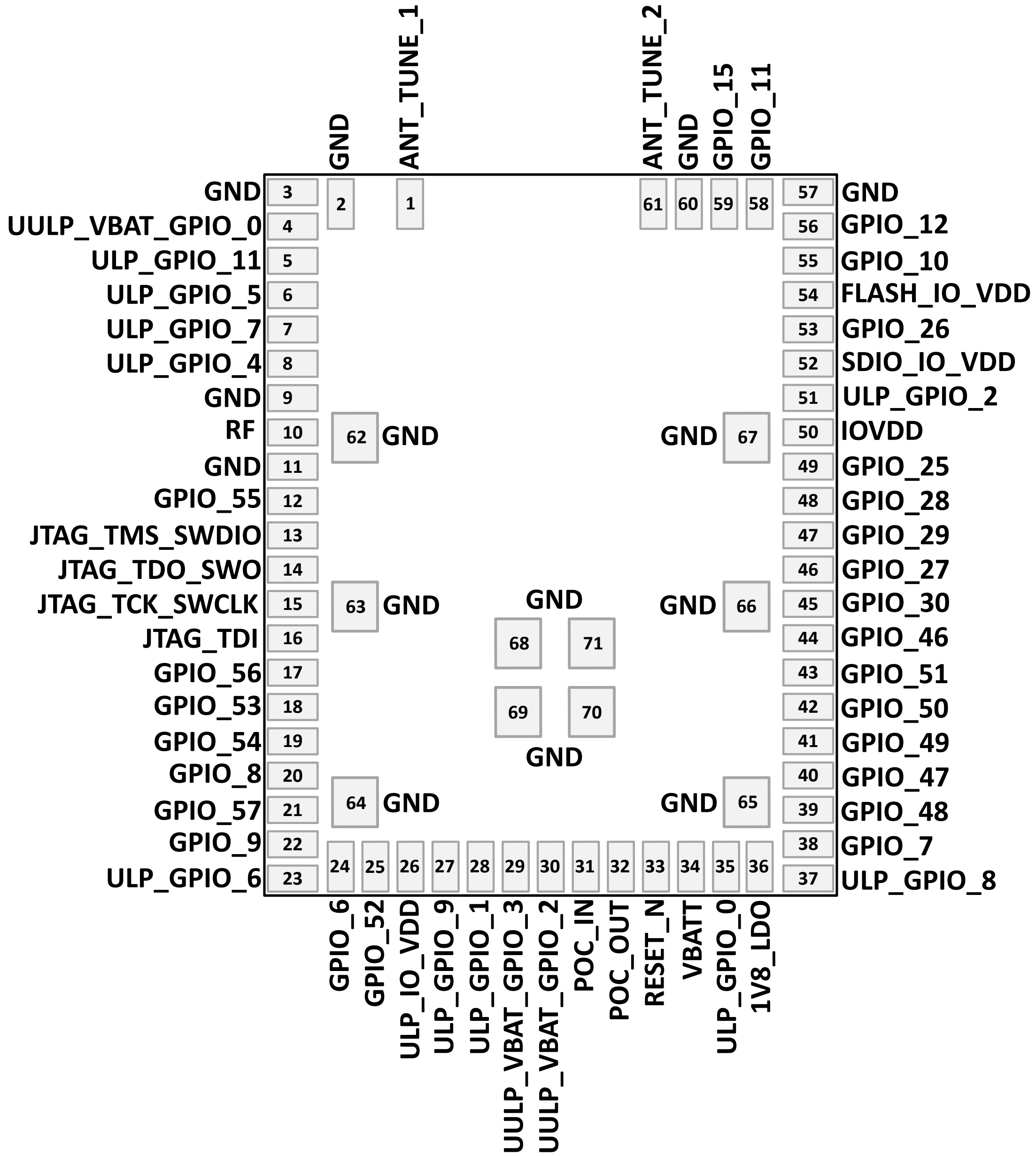


Figure 6.1. SiWG917 Pin Diagram

6.2 Pin Description

Table 6.1. List of IC Pins Not Available in the Modules

Pin Name	QFN I/O Supply Domain	Direction	Initial State (Power up, Active Reset)	Description
RF_BLETX	RF_AVDD	Output	NA	BLE 8 dBm RF Output
ULP_GPIO_10	ULP_IO_VDD	Inout	HighZ	Default: HighZ Sleep: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
XTAL_32KHZ_P	NA	Inout	NA	Analog Pin. 32KHZ XTAL Connection
XTAL_32KHZ_N	NA	Inout	NA	Analog Pin. 32KHZ XTAL Connection
UULP_VBAT_GPIO_1	VBATT	Inout	HighZ	Default: High Sleep: High Refer to Section 6.3 GPIO Pin Multiplexing for configuration
TRST	VBATT	Input	HighZ	Test signal

6.2.1 RF and Control Interfaces

Table 6.2. Chip Packages - RF and Control Interfaces

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
ANT_TUNE_1	1	N/A	Input	N/A	**SiW917Y1GA:** External fine-tuning option for the integral antenna; connect same tuning circuit on both ANT_TUNE1 and ANT_TUNE2 pins; leave floating if no fine-tuning is desired on the integral antenna; **SiW917Y1GN:** leave this pin floating
RF	10	VBATT	Inout	N/A	Connect to antenna with a 50-Ω impedance as per the reference schematics
POC_IN	31	VBATT	Input	NA	This is an input to the chip which resets all analog and digital blocks in the device. It should be made high only after supplies are valid.
POC_OUT	32	VBATT	Output	NA	This is internally generated. Initially, it is low. But it becomes high when the supply (VBATT) is valid.
RESET_N	33	VBATT	Inout	NA	Active-low reset asynchronous reset signal, which resets only digital blocks. RESET_N will be pulled low if POC_IN is low.
ANT_TUNE_2	61	N/A	Input	N/A	**SiW917Y1GA:** External fine-tuning option for the integral antenna; connect same tuning circuit on both ANT_TUNE1 and ANT_TUNE2 pins; leave floating if no fine-tuning is desired on the integral antenna; **SiW917Y1GN:** leave this pin floating

6.2.2 Power and Ground Pins

Table 6.3. Chip Packages - Power and Ground Pins

Pin Name	Pin No.	Type	Direction	Description
ULP_IO_VDD	26	Power	Input	I/O supply for ULP I/Os. Refer to the GPIOs section for details on which GPIOs have this as the I/O supply.
VBATT	34	Power	Input	Power supply for the module.
1V8_LDO	36	Power	Output	Output of 1.8V LDO which is used for Flash supply.
IOVDD	50	Power	Input	I/O Supply for I/Os. Refer to Section 6.3 GPIO Pin Multiplexing for details on which GPIOs have this as the I/O supply.
SDIO_IO_VDD	52	Power	Input	I/O Supply for SDIO I/Os. Refer to Section 6.3 GPIO Pin Multiplexing for details on which GPIOs have this as the I/O supply.
FLASH_IO_VDD	54	Power	Input	I/O Supply for IC stacked Flash. Connect to 1V8_LDO as per Reference Schematics.
GND	2, 3, 9, 11, 57, 60, 62-71	Ground		Common ground pins.

6.2.3 Peripheral Interfaces

Table 6.4. Chip Packages - Peripheral Interfaces

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
UULP_VBAT_GPIO_0	4	VBATT	Output	High	**Default**: High **Sleep**: High Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Supply domain for UULP_VBAT_GPIOs is VBATT and the supported voltage range is defined in Table 7.2 Recommended Operating Conditions on page 92.
ULP_GPIO_11	5	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_5	6	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_7	7	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_4	8	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_55	12	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO.
JTAG_TMS_SWDIO	13	IO_VDD	Input	Pullup	JTAG interface Test Mode Select signal. Bi-directional data pin for SWD interface.

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
JTAG_TDO_SWO	14	IO_VDD	Output	Pullup	JTAG interface output data. Serial wire output for SWD Interface.This pin can also be used as ISP_ENABLE. Pull down to enable ISP mode. In System Programming (ISP) is programming or reprogramming of the flash through boot loader using UART (GPIO_8,GPIO_9), SPI (GPIO_25 to GPIO_28) and SDIO (GPIO_25 to GPIO_30) interfaces. This can be done after the part is integrated on end user board. Boot loader can be requested to boot in ISP mode by pulling down JTAG_TDO_SWO pin. This pin has to be left unconnected during reset for the boot loader to bypass ISP and execute the code that is present in flash. ISP mode can be used to reprogram the flash, if the application codes uses JTAG pins for other multiplexed functionalities. On boot up, if the application code goes into a state where JTAG interface is not functioning, ISP mode can be used to gain the control and to reprogram the flash.
JTAG_TCK_SWCLK	15	IO_VDD	Input	Pullup	JTAG interface clock or serial wire clock
JTAG_TDI	16	IO_VDD	Input	Pullup	JTAG interface input data
GPIO_56	17	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO.
GPIO_53	18	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO.
GPIO_54	19	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO.

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
GPIO_8/ISP_UART_RX	20	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ **ISP**: UART_RX If ISP is not enabled, refer to Scetion 6.3 GPIO Pin Multiplexing for configuration
GPIO_57	21	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO.
GPIO_9/ISP_UART_TX	22	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ **ISP**: UART_TX If ISP is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_6	23	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ PTA_PRIO: "PTA Priority" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. If PTA feature is enabled, use it as PTA_PRIO. If PTA feature is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration.
GPIO_6	24	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_52	25	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO.
ULP_GPIO_9	27	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
ULP_GPIO_1	28	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ PTA_REQ: "PTA Request" input signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. If PTA feature is enabled, use it as PTA_REQ. If PTA feature is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration.
UULP_VBAT_GPIO_3	29	VBATT	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Supply domain for UULP_VBAT_GPIOs is VBATT and the supported voltage range is defined in Table 7.2 Recommended Operating Conditions on page 92.
UULP_VBAT_GPIO_2	30	VBATT	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Supply domain for UULP_VBAT_GPIOs is VBATT and the supported voltage range is defined in Table 7.2 Recommended Operating Conditions on page 92.
ULP_GPIO_0	35	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
ULP_GPIO_8	37	ULP_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_7	38	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ PTA_GRANT: "PTA Grant" output signal is part of 3-wire coexistence (Packet Traffic Arbitration) interface. If PTA feature is enabled, use it as PTA_GRANT. If PTA feature is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration.

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
GPIO_48	39	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO. Reserved for on-module Flash usage with Module OPNs SiWG917Y121MGNBA and SiWG917Y121MGABA.
GPIO_47	40	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO. Reserved for on-module Flash usage with Module OPNs SiWG917Y121MGNBA and SiWG917Y121MGABA.
GPIO_49	41	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO. Reserved for on-module Flash usage with Module OPNs SiWG917Y121MGNBA and SiWG917Y121MGABA.
GPIO_50	42	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO. Reserved for on-module Flash usage with Module OPNs SiWG917Y121MGNBA and SiWG917Y121MGABA.
GPIO_51	43	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO. Reserved for on-module Flash usage with Module OPNs SiWG917Y121MGNBA and SiWG917Y121MGABA.

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
GPIO_46	44	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration. Reserved to Flash or PSRAM memory usage in case of Flash or PSRAM memory is connected to this GPIO. Reserved for on-module Flash usage with Module OPNs SiWG917Y121MGNBA and SiWG917Y121MGABA.
GPIO_30/SDIO_D3	45	SDIO_IO_VDD	Inout	Pullup	**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_D3 If ISP is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration.
GPIO_27/SDIO_D0/HSPI_MOSI	46	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_DO or HSPI_MOSI If ISP is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_29/SDIO_D2/HSPI_INTR	47	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_D2 or HSPI_MISO If ISP is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_28/SDIO_D1/HSPI_MISO	48	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_D1 or HSPI_MISO If ISP is not enable, refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_25/SDIO_CLK/HSPI_CLK	49	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_CLK or HSPI_CLK If ISP is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration

Pin Name	Pin No.	I/O Supply Domain	Direction	Initial State (Power up Active Reset)	Description
ULP_GPIO_2	51	ULP_IO_VDD	Input	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_26/SDIO_CMD/HSPI_CSN	53	SDIO_IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ **ISP**: SDIO_CMD or HSPI_CSN If ISP is not enabled, refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_10	55	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_12	56	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_11	58	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
GPIO_15	59	IO_VDD	Inout	HighZ	**Default**: HighZ **Sleep**: HighZ Refer to Section 6.3 GPIO Pin Multiplexing for configuration
Note: GPIOs 46 to 51 are reserved for the on-module Flash on OPNs SiWG917Y121MGNBA and SiWG917Y121MGABA. No GPIO functionality is available on GPIO pins 46 to 51 for these OPNs.					

6.3 GPIO Pin Multiplexing

Note:

1. SiWG917 has the support for 43 GPIOs. These GPIOs are grouped into SoC GPIOs, ULP GPIOs, and UULP GPIOs.
2. **The possible GPIO combinations for each Peripheral Interface are listed in Section 6.4 Valid GPIO Sets for Peripherals.**
3. The digital GPIOs SOCPERH_ON_ULP_GPIO_0 to SOCPERH_ON_ULP_GPIO_11 are mapped onto physical ULP GPIOs for SoC Peripheral functionality and digital GPIOs ULPPERH_ON_SOC_GPIO_0 to ULPPERH_ON_SOC_GPIO_11 are mapped onto physical SoC GPIOs for ULP Peripheral functionality. Refer to Section 6.3.5 Digital Functions for peripheral mapping on these GPIOs

6.3.1 SoC GPIO Pin Multiplexing

The SoC GPIOs shown in Table 6.5 SoC GPIO Pin Multiplexing on page 67 (GPIO_6 to GPIO_57) are available in the normal mode of operation (Power-states 4 and 3). Default mode is mode0 (Mode = 0) if not explicitly mentioned. For a description of power-states, refer to the Power States section of the Reference Manual. Each of these GPIOs Pin function is controlled by the GPIO Mode register mentioned in SoC GPIOs section of the Reference Manual.

Table 6.5. SoC GPIO Pin Multiplexing

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_6	0: GPIO_6 1: 2: USART0_CTS 3: SSI_MST_DATA2 4: I2C0_SDA 5: I2C1_SCL	6: UART1_RX 7: I2S0_DIN_1 8: PMU_TEST_1 9: ULPPERH_ON_SOC_GPIO_0 10: PWM_0L 11: M4SS_QSPI_D0	12: GSPI_MOSI 13: M4SS_TRACE_CLKIN 14: 15: NWP_GPIO_6
GPIO_7	0: GPIO_7 1: 2: USART0_DTR 3: SSI_MST_DATA3 4: I2C0_SCL 5: I2C1_SDA	6: UART1_TX 7: I2S0_DOUT_1 8: PMU_TEST_2 9: ULPPERH_ON_SOC_GPIO_1 10: PWM_0H 11: M4SS_QSPI_CSN0	12: M4SS_QSPI_CSN1 13: M4SS_TRACE_CLK 14: 15:
GPIO_8 / ISP_UART_RX	0: GPIO_8 1: 2: USART0_CLK 3: SSI_MST_CLK 4: GSPI_CLK 5: QEI_IDX	6: UART1_RS485_RE 7: I2S0_CLK 8: SSI_SLV_CLK 9: ULPPERH_ON_SOC_GPIO_2 10: PWM_1L 11: M4SS_QSPI_CLK	12: 13: M4SS_TRACE_D0 14: 15: NWP_GPIO_8
GPIO_9 / ISP_UART_TX	0: GPIO_9 1: 2: USART0_RTS 3: SSI_MST_CS0 4: GSPI_CS0 5: QEI_PHA	6: UART1_RS485_DE 7: I2S0_WS 8: SSI_SLV_CS 9: ULPPERH_ON_SOC_GPIO_3 10: PWM_1H 11: M4SS_QSPI_D1	12: 13: M4SS_TRACE_D1 14: 15: NWP_GPIO_9
GPIO_10	0: GPIO_10 1: 2: USART0_RX 3: SSI_MST_CS1 4: GSPI_CS1 5: QEI_PHB	6: UART1_RTS 7: I2S0_DIN_0 8: SSI_SLV_MOSI 9: ULPPERH_ON_SOC_GPIO_4 10: PWM_2L 11: M4SS_QSPI_D2	12: SSI_MST_DATA1 13: M4SS_TRACE_D2 14: 15: NWP_GPIO_10

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_11	0: GPIO_11 1: 2: USART0_DSR 3: SSI_MST_DATA0 4: GSPI_MISO 5: QEI_DIR	6: UART1_CTS 7: I2S0_DOUT_0 8: SSI_SLV_MISO 9: ULPPERH_ON_SOC_GPIO_5 10: PWM_2H 11: M4SS_QSPI_D3	12: MCU_CLK_OUT 13: M4SS_TRACE_D3 14: 15: NWP_GPIO_11
GPIO_12	0: GPIO_12 1: 2: USART0_DCD 3: SSI_MST_DATA1 4: GSPI_MOSI 5:	6: UART1_RS485_EN 7: 8: MCU_CLK_OUT 9: ULPPERH_ON_SOC_GPIO_6 10: PWM_3L 11:	12: 13: 14: 15: NWP_GPIO_12
GPIO_15	0: GPIO_15 1: 2: USART0_TX 3: SSI_MST_CS2 4: GSPI_CS2 5:	6: M4SS_TRACE_CLKIN 7: 8: MCU_CLK_OUT 9: ULPPERH_ON_SOC_GPIO_7 10: PWM_3H 11:	12: 13: 14: 15: NWP_GPIO_15
GPIO_25 / SDIO_CLK / HSPI_CLK	0: GPIO_25 1: 2: USART0_CLK 3: SSI_MST_CLK 4: GSPI_CLK 5: QEI_IDX	6: 7: I2S0_CLK 8: SSI_SLV_CS 9: SCT_IN_0 10: PWM_FAULTA 11: ULPPERH_ON_SOC_GPIO_6	12: SOC_PLL_CLOCK 13: USART0_IR_RX 14: TopGPIO_0 15:
GPIO_26 / SDIO_CMD / HSPI_CSN	0: GPIO_26 1: 2: USART0_CTS 3: SSI_MST_DATA0 4: GSPI_MISO 5: QEI_PHA	6: UART1_RS485_EN 7: I2S0_WS 8: SSI_SLV_CLK 9: 10: PWM_FAULTB 11: ULPPERH_ON_SOC_GPIO_7	12: INTERFACE_PLL_CLOCK 13: USART0_IR_TX 14: TopGPIO_1 15:
GPIO_27 / SDIO_D0 / HSPI_MOSI	0: GPIO_27 1: 2: USART0_RI 3: SSI_MST_DATA1 4: GSPI_MOSI 5: QEI_PHB	6: UART1_RTS 7: I2S0_DIN_0 8: SSI_SLV_MOSI 9: 10: PWM_TMR_EXT_TRIG_1 11: ULPPERH_ON_SOC_GPIO_8	12: I2S_PLL_CLOCK 13: USART0_RS485_EN 14: TopGPIO_2 15:

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_28 / SDIO_D1 / HSPI_MISO	0: GPIO_28 1: 2: USART0_RTS 3: SSI_MST_CS0 4: GSPI_CS0 5: QEI_DIR	6: UART1_CTS 7: I2S0_DOUT_0 8: SSI_SLV_MISO 9: 10: PWM_TMR_EXT_TRIG_2 11: ULPPERH_ON_SOC_GPIO_9	12: XTAL_ON_IN 13: USART0_RS485_RE 14: TopGPIO_3 15:
GPIO_29 / SDIO_D2 / HSPI_INTR	0: GPIO_29 1: 2: USART0_RX 3: SSI_MST_DATA2 4: GSPI_CS1 5: I2C1_SCL	6: UART1_RX 7: I2S0_DIN_1 8: PMU_TEST_1 9: SCT_OUT_0 10: PWM_TMR_EXT_TRIG_3 11: ULPPERH_ON_SOC_GPIO_10	12: USART0_DCD 13: USART0_RS485_DE 14: TopGPIO_4 15:
GPIO_30 / SDIO_D3	0: GPIO_30 1: 2: USART0_TX 3: SSI_MST_DATA3 4: GSPI_CS2 5: I2C1_SDA	6: UART1_TX 7: I2S0_DOUT_1 8: PMU_TEST_2 9: SCT_OUT_1 10: PWM_TMR_EXT_TRIG_4 11: ULPPERH_ON_SOC_GPIO_11	12: PMU_TEST_1 13: PMU_TEST_2 14: TopGPIO_5 15:
JTAG_TCK_SWCLK	0: GPIO_31 1: 2: 3: 4: 5:	6: 7: 8: 9: 10: 11: I2C0_SDA	12: UART1_RTS 13: QEI_IDX 14: 15:
JTAG_TDI	0: GPIO_32 1: 2: 3: 4: 5:	6: 7: 8: 9: 10: 11: I2C0_SCL	12: UART1_CTS 13: QEI_PHA 14: 15:
JTAG_TMS_SWDIO	0: GPIO_33 1: 2: 3: 4: 5:	6: 7: 8: 9: 10: 11: I2C1_SCL	12: UART1_RX 13: QEI_PHB 14: 15:

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
JTAG_TDO_SWO	0: GPIO_34 1: 2: 3: 4: 5:	6: 7: 8: 9: 10: 11: I2C1_SDA	12: UART1_TX 13: QEI_DIR 14: 15:
GPIO_46	0: GPIO_46 1: M4SS_QSPI_CLK 2: USART0_RI 3: QEI_IDX 4: GSPI_CLK 5:	6: M4SS_TRACE_CLKIN 7: I2S0_CLK 8: SSI_SLV_CS 9: ULPPERH_ON_SOC_GPIO_8 10: SOC_PLL_CLOCK 11: M4SS_PSRAM_CLK	12: 13: 14: 15: NWP_GPIO_46
GPIO_47	0: GPIO_47 1: M4SS_QSPI_D0 2: USART0_IR_RX 3: QEI_PHA 4: GSPI_MISO 5:	6: M4SS_TRACE_CLK 7: I2S0_WS 8: SSI_SLV_CLK 9: ULPPERH_ON_SOC_GPIO_9 10: INTERFACE_PLL_CLOCK 11: M4SS_PSRAM_D0	12: 13: 14: 15: NWP_GPIO_47
GPIO_48	0: GPIO_48 1: M4SS_QSPI_D1 2: USART0_IR_TX 3: QEI_PHB 4: GSPI_MOSI 5:	6: M4SS_TRACE_D0 7: I2S0_DIN_0 8: SSI_SLV_MOSI 9: ULPPERH_ON_SOC_GPIO_10 10: I2S_PLL_CLOCK 11: M4SS_PSRAM_D1	12: 13: 14: 15: NWP_GPIO_48
GPIO_49	0: GPIO_49 1: M4SS_QSPI_CSN0 2: USART0_RS485_EN 3: QEI_DIR 4: GSPI_CS0 5:	6: M4SS_TRACE_D1 7: I2S0_DOUT_0 8: SSI_SLV_MISO 9: ULPPERH_ON_SOC_GPIO_11 10: 11: M4SS_PSRAM_CSN0	12: 13: 14: 15: NWP_GPIO_49
GPIO_50	0: GPIO_50 1: M4SS_QSPI_D2 2: USART0_RS485_RE 3: SSI_MST_CS2 4: GSPI_CS1 5: I2C1_SCL	6: M4SS_TRACE_D2 7: I2S0_DIN_1 8: PWM_TMR_EXT_TRIG_4 9: UART1_RTS 10: MEMS_REF_CLOCK 11: M4SS_PSRAM_D2	12: 13: 14: 15: NWP_GPIO_50

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_51	0: GPIO_51 1: M4SS_QSPI_D3 2: USART0_RS485_DE 3: SSI_MST_CS3 4: GSPI_CS2 5: I2C1_SDA	6: M4SS_TRACE_D3 7: I2S0_DOUT_1 8: PWM_TMR_EXT_TRIG_1 9: UART1_CTS 10: PLL_TESTMODE_SIG 11: M4SS_PSRAM_D3	12: 13: 14: 15: NWP_GPIO_51
GPIO_52	0: GPIO_52 1: 2: USART0_CLK 3: SSI_MST_CLK 4: GSPI_CLK 5: QEI_IDX	6: M4SS_TRACE_CLKIN 7: I2S0_CLK 8: SSI_SLV_CLK 9: M4SS_QSPI_CLK 10: SOC_PLL_CLOCK 11:	12: M4SS_PSRAM_CLK 13: 14: 15:
GPIO_53	0: GPIO_53 1: M4SS_QSPI_CSN1 2: USART0_RTS 3: SSI_MST_CS0 4: GSPI_CS0 5: QEI_PHA	6: M4SS_TRACE_CLK 7: I2S0_WS 8: SSI_SLV_CS 9: M4SS_QSPI_D0 10: INTERFACE_PLL_CLOCK 11: M4SS_PSRAM_CSN1	12: M4SS_PSRAM_D0 13: 14: 15:
GPIO_54	0: GPIO_54 1: M4SS_QSPI_D4 2: USART0_TX 3: SSI_MST_DATA2 4: GSPI_CS1 5: I2C1_SCL	6: M4SS_TRACE_D0 7: I2S0_DIN_1 8: PWM_TMR_EXT_TRIG_2 9: M4SS_QSPI_D1 10: I2S_PLL_CLOCK 11: M4SS_PSRAM_D4	12: M4SS_PSRAM_D1 13: 14: 15:
GPIO_55	0: GPIO_55 1: M4SS_QSPI_D5 2: USART0_RX 3: SSI_MST_DATA3 4: GSPI_CS2 5: I2C1_SDA	6: M4SS_TRACE_D1 7: I2S0_DOUT_1 8: PWM_TMR_EXT_TRIG_3 9: M4SS_QSPI_CSN0 10: 11: M4SS_PSRAM_D5	12: M4SS_PSRAM_CSN0 13: 14: 15:
GPIO_56	0: GPIO_56 1: M4SS_QSPI_D6 2: USART0_CTS 3: SSI_MST_DATA0 4: GSPI_MISO 5: QEI_PHB	6: M4SS_TRACE_D2 7: I2S0_DIN_0 8: SSI_SLV_MOSI 9: M4SS_QSPI_D2 10: MEMS_REF_CLOCK 11: M4SS_PSRAM_D6	12: M4SS_PSRAM_D2 13: 14: 15:

GPIO	GPIO Modes 0, 1, 2, 3, 4, 5	GPIO Modes 6, 7, 8, 9, 10, 11	GPIO Modes 12, 13, 14, 15
GPIO_57	0: GPIO_57 1: M4SS_QSPI_D7 2: USART0_DSR 3: SSI_MST_DATA1 4: GSPI_MOSI 5: QEI_DIR	6: M4SS_TRACE_D3 7: I2S0_DOUT_0 8: SSI_SLV_MISO 9: M4SS_QSPI_D3 10: XTAL_ON_IN 11: M4SS_PSRAM_D7	12: M4SS_PSRAM_D3 13: 14: 15:

Note:

1. GPIOs 25 to 30 can be used for Analog functions when GPIO Mode = 14. Multiple Analog functions are available on each pin as shown in the below Analog Pin Multiplexing Table. These analog functions are enabled and disabled through programming - refer to the Reference Manual for more details.
2. NWP GPIOs can be used for Network Processor functions when GPIO Mode = 15.
3. GPIOs 46 to 51 are reserved for the on-module Flash on OPNs SiWG917Y121MGNBA and SiWG917Y121MGABA. No GPIO functionality is available on GPIO pins 46 to 51 for these OPNs.

6.3.2 ULP GPIO Pin Multiplexing

The ULP GPIOs shown in Table 6.6 ULP GPIO Pin Multiplexing on page 73 (ULP_GPIO_0 to ULP_GPIO_11) are available in the normal mode of operation (Power-states 4 and 3) and also in Ultra-low power mode of operation of the Microcontroller (Power-states 2 and 1). For a description of power-states, refer to the Power States section of the Reference Manual. Each of these GPIOs Pin function is controlled by the GPIO Mode register mentioned in ULP GPIOs section of the Reference Manual.

Table 6.6. ULP GPIO Pin Multiplexing

ULP_GPIO	ULP GPIO Modes 0, 1, 2, 3	ULP GPIO Modes 4, 5, 6, 7	ULP GPIO Modes 8, 9, 10, 11
ULP_GPIO_0	0: ULP_EGPIO_0 1: ULP_SSI_CLK 2: ULP_I2S_DIN 3: ULP_UART_RTS	4: ULP_I2C_SDA 5: 6: SOCPERH_ON_ULP_GPIO_0 7: AGPIO_0	8: 9: 10: 11:
ULP_GPIO_1	0: ULP_EGPIO_1 1: ULP_SSI_DOUT 2: ULP_I2S_DOUT 3: ULP_UART_CTS	4: ULP_I2C_SCL 5: Timer2 6: SOCPERH_ON_ULP_GPIO_1 7: AGPIO_1	8: 9: 10: 11:
ULP_GPIO_2	0: ULP_EGPIO_2 1: ULP_SSI_DIN 2: ULP_I2S_WS 3: ULP_UART_RX	4: 5: COMP1_OUT 6: SOCPERH_ON_ULP_GPIO_2 7: AGPIO_2	8: 9: 10: 11:
ULP_GPIO_4	0: ULP_EGPIO_4 1: ULP_SSI_CS1 2: ULP_I2S_WS 3: ULP_UART_RTS	4: ULP_I2C_SDA 5: AUX_ULP_TRIG_1 6: SOCPERH_ON_ULP_GPIO_4 7: AGPIO_4	8: ULP_SSI_CLK 9: Timer0 10: IR_INPUT 11:
ULP_GPIO_5	0: ULP_EGPIO_5 1: IR_OUTPUT 2: ULP_I2S_DOUT 3: ULP_UART_CTS	4: ULP_I2C_SCL 5: AUX_ULP_TRIG_0 6: SOCPERH_ON_ULP_GPIO_5 7: AGPIO_5	8: ULP_SSI_DOUT 9: Timer1 10: IR_OUTPUT 11:
ULP_GPIO_6	0: ULP_EGPIO_6 1: ULP_SSI_CS2 2: ULP_I2S_DIN 3: ULP_UART_RX	4: ULP_I2C_SDA 5: 6: SOCPERH_ON_ULP_GPIO_6 7: AGPIO_6	8: ULP_SSI_DIN 9: COMP1_OUT 10: AUX_ULP_TRIG_0 11:
ULP_GPIO_7	0: ULP_EGPIO_7 1: IR_INPUT 2: ULP_I2S_CLK 3: ULP_UART_TX	4: ULP_I2C_SCL 5: Timer1 6: SOCPERH_ON_ULP_GPIO_7 7: AGPIO_7	8: ULP_SSI_CS0 9: COMP2_OUT 10: AUX_ULP_TRIG_1 11:
ULP_GPIO_8	0: ULP_EGPIO_8 1: ULP_SSI_CLK 2: ULP_I2S_CLK 3: ULP_UART_CTS	4: ULP_I2C_SCL 5: Timer0 6: SOCPERH_ON_ULP_GPIO_8 7: AGPIO_8	8: 9: 10: 11:

ULP_GPIO	ULP GPIO Modes 0, 1, 2, 3	ULP GPIO Modes 4, 5, 6, 7	ULP GPIO Modes 8, 9, 10, 11
ULP_GPIO_9	0: ULP_EGPIO_9 1: ULP_SSI_DIN 2: ULP_I2S_DIN 3: ULP_UART_RX	4: ULP_I2C_SDA 5: 6: SOCPERH_ON_ULP_GPIO_9 7: AGPIO_9	8: 9: 10: 11:
ULP_GPIO_11	0: ULP_EGPIO_11 1: ULP_SSI_DOUT 2: ULP_I2S_DOUT 3: ULP_UART_TX	4: ULP_I2C_SDA 5: AUX_ULP_TRIG_0 6: SOCPERH_ON_ULP_GPIO_11 7: AGPIO_11	8: 9: 10: 11:
Note: 1. All the ULP GPIOs can be used for Analog functions when ULP GPIO Mode = 7. Multiple Analog functions are available on each pin as shown in the below Analog Pin Multiplexing Table. These analog functions are enabled and disabled through programming - refer to the Reference Manual for more details. 2. All the ULP GPIOs can be used for Digital functions when ULP GPIO Mode = 6. The digital functions available on these GPIOs is shown in the below Digital Pin Multiplexing Table.			

6.3.3 UULP VBAT GPIO Pin Multiplexing

The UULP VBAT GPIOs shown in Table 6.7 UULP VBAT GPIO Pin Multiplexing on page 74 (UULP_VBAT_GPIO_0 to UULP_VBAT_GPIO_3) are available in the normal mode of operation (Power-states 4 and 3), in Ultra-low power mode of operation (Power-states 2 and 1) and also in the retention and deep sleep mode of operation (Retention and Power-state 0). For a description of power-states, refer to the Power States section of the Reference Manual. Each of this UULP VBAT GPIOs Pin function is controlled by the GPIO Mode register mentioned in UULP VBAT GPIOs section of the Reference Manual.

Table 6.7. UULP VBAT GPIO Pin Multiplexing

UULP VBAT GPIO	UULP VBAT GPIO Mode = 0, 1, 2, 3	UULP VBAT GPIO Mode = 4, 5, 6, 7	Default
UULP_VBAT_GPIO_0	0: UULP_VBAT_GPIO[0] 1: 2: MCU_GPIO0_WAKEUP 3: SYSRTC_PRS_IN_G0	4: SYSRTC_PRS_OUT_G0_1 5: XTAL_32KHZ_IN 6: 7:	1: (no function)
UULP_VBAT_GPIO_2	0: UULP_VBAT_GPIO[2] 1: NWP_GPIO0_WAKEUP 2: MCU_GPIO2_WAKEUP 3: MCU_GPIO_TOGGLE	4: XTAL_32KHZ_IN 5: SYSRTC_PRS_OUT_G1_1 6: 7: VOLT_SENSE	NWP_GPIO0_WAKEUP
UULP_VBAT_GPIO_3	0: UULP_VBAT_GPIO[3] 1: NWP_GPIO1_WAKEUP 2: MCU_GPIO3_WAKEUP 3: SYSRTC_PRS_OUT_G0_0	4: MCU_GPIO_TOGGLE 5: XTAL_32KHZ_IN 6: 7: COMP_P	UULP_VBAT_GPIO[3]

6.3.4 Analog Functions

Analog functions are available on several of the SoC GPIO and ULP_GPIO pins. The analog functions are mapped to ULP_GPIO pins on the AGPIO_x selections, and to SoC GPIO pins on the TopGPIO_x selections shown in the multiplexing tables. A summary of signals and potential GPIO mapping are shown in Table 6.8 Analog Functions for SoC/ULP GPIOs on page 75.

Table 6.8. Analog Functions for SoC/ULP GPIOs

Signal - GPIO	ADC Function	DAC Function	Comparator Function	OpAmp Function
AGPIO_0 - ULP_GPIO_0	ADCP[0]		COMP1_P0	OPAMP1_IN[2]
AGPIO_1 - ULP_GPIO_1	ADCP[10] ADCN[0]		COMP1_N0	
AGPIO_2 - ULP_GPIO_2	ADCP[1]		COMP2_P0	OPAMP1_IN[3]
AGPIO_3 - ULP_GPIO_3	ADCP[11] ADCN[1]		COMP2_N0	
AGPIO_4 - ULP_GPIO_4	ADCP[2]	DAC0	COMP1_N1	OPAMP1OUT0
AGPIO_5 - ULP_GPIO_5	ADCP[12] ADCN[2]		COMP1_P1	OPAMP2_IN[1]
AGPIO_6 - ULP_GPIO_6	ADCP[3]			OPAMP1_IN[4]
AGPIO_7 - ULP_GPIO_7	ADCP[15] ADCN[5]			OPAMP1_IN[1]
AGPIO_8 - ULP_GPIO_8	ADCP[4]			OPAMP1_IN[5]
AGPIO_9 - ULP_GPIO_9	ADCP[14] ADCN[4]			OPAMP2OUT0
AGPIO_11 - ULP_GPIO_11	ADCP[13] ADCN[3]			OPAMP2_IN[0]
TopGPIO_0 - GPIO_25	ADCP[6]			
TopGPIO_1 - GPIO_26	ADCP[16] ADCN[6]			
TopGPIO_2 - GPIO_27	ADCP[7]		COMP2_P1	OPAMP3OUT0 OPAMP1_IN[0]
TopGPIO_3 - GPIO_28	ADCP[17] ADCN[7]		COMP2_N1	
TopGPIO_4 - GPIO_29	ADCP[8]			OPAMP3_IN[1]
TopGPIO_5 - GPIO_30	ADCP[18] ADCN[8]	DAC1		OPAMP1OUT1

Note:

1. Software can program above different functions.
2. ADCP and ADCN can be independently selected from any of the channels shown. Single-ended measurements use only ADCP, and differential measurements use both ADCP and ADCN.
3. Please refer to "Reference Manual" for software programming information.
4. Please refer to "API Documentation" for software programming information.

6.3.5 Digital Functions

The ULP GPIOs shown in Table 6.9 SoC on ULP GPIO Pin Multiplexing on page 76 are configured for SoC peripheral functionality (SOCPERH_ON_ULP_GPIO_0 to SOCPERH_ON_ULP_GPIO_11) and are available only in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Power States section of the Reference Manual. Each of these GPIOs Pin function is controlled by the GPIO Mode register mentioned in SoC GPIOs section of the Reference Manual.

Table 6.9. SoC on ULP GPIO Pin Multiplexing

GPIO	GPIO Modes 0, 1, 2, 3, 4	GPIO Modes 5, 6, 7, 8, 9	GPIO Modes 10, 11, 12, 13
SOCPERH_ON_ULP_GPIO_0	0: GPIO_64 1: 2: USART0_CLK 3: QEI_IDX 4: I2C0_SDA	5: I2C1_SCL 6: UART1_RS485_EN 7: SCT_IN_0 8: PWM_0L 9: UART1_RTS	10: 11: USART0_IR_RX 12: PWM_0L 13: PMU_TEST_1
SOCPERH_ON_ULP_GPIO_1	0: GPIO_65 1: 2: USART0_RX 3: QEI_PHA 4: I2C0_SCL	5: I2C1_SDA 6: UART1_RS485_RE 7: 8: PWM_0H 9: UART1_CTS	10: 11: USART0_IR_TX 12: PWM_0H 13: PMU_TEST_2
SOCPERH_ON_ULP_GPIO_2	0: GPIO_66 1: 2: 3: QEI_PHB 4: I2C0_SCL	5: I2C1_SCL 6: UART1_RS485_DE 7: 8: PWM_1L 9: UART1_RX	10: PMU_TEST_1 11: 12: 13:
SOCPERH_ON_ULP_GPIO_4	0: GPIO_68 1: 2: USART0_TX 3: QEI_IDX 4:	5: 6: UART1_RX 7: SCT_OUT_0 8: PWM_2L 9: SCT_IN_0	10: PWM_FAULTA 11: USART0_RI 12: PWM_1L 13:
SOCPERH_ON_ULP_GPIO_5	0: GPIO_69 1: 2: USART0_RTS 3: QEI_PHA 4:	5: 6: UART1_TX 7: SCT_OUT_1 8: PWM_2H 9:	10: PWM_FAULTB 11: USART0_RS485_EN 12: PWM_1H 13:
SOCPERH_ON_ULP_GPIO_6	0: GPIO_70 1: 2: USART0_CTS 3: QEI_PHB 4: USART0_RX	5: I2C1_SCL 6: UART1_RTS 7: 8: PWM_3L 9:	10: PWM_TMR_EXT_TRIG_1 11: USART0_RS485_RE 12: PMU_TEST_1 13:

GPIO	GPIO Modes 0, 1, 2, 3, 4	GPIO Modes 5, 6, 7, 8, 9	GPIO Modes 10, 11, 12, 13
SOCPERH_ON_ULP_GPIO_7	0: GPIO_71 1: 2: USART0_IR_RX 3: QEI_DIR 4: USART0_TX	5: I2C1_SDA 6: UART1_CTS 7: 8: PWM_3H 9:	10: PWM_TMR_EXT_TRIG_2 11: USART0_RS485_DE 12: PMU_TEST_2 13:
SOCPERH_ON_ULP_GPIO_8	0: GPIO_72 1: 2: USART0_IR_TX 3: QEI_IDX 4:	5: 6: UART1_RX 7: 8: PWM_SLP_EVENT_TRIG 9: UART1_RTS	10: PWM_TMR_EXT_TRIG_3 11: 12: 13:
SOCPERH_ON_ULP_GPIO_9	0: GPIO_73 1: 2: USART0_RS485_EN 3: QEI_PHA 4:	5: 6: UART1_TX 7: 8: PWM_FAULTA 9: UART1_CTS	10: PWM_TMR_EXT_TRIG_4 11: 12: 13:
SOCPERH_ON_ULP_GPIO_11	0: GPIO_75 1: 2: USART0_RS485_DE 3: QEI_DIR 4: I2C0_SCL	5: 6: UART1_RS485_DE 7: 8: PWM_TMR_EXT_TRIG_1 9: UART1_TX	10: PMU_TEST_2 11: 12: 13:

The SoC GPIOs shown in Table 6.10 ULP on SoC GPIO Pin Multiplexing on page 78 are configured for ULP peripheral functionality (ULPPERH_ON_SOC_GPIO_0 to ULPPERH_ON_SOC_GPIO_11) and are available only in the normal mode of operation (Power-states 4 and 3). For a description of power-states, refer to the Power States section of the Reference Manual. Each of these GPIOs Pin function is controlled by the GPIO Mode register mentioned in ULP GPIOs section of the Reference Manual.

Table 6.10. ULP on SoC GPIO Pin Multiplexing

ULP_GPIO	ULP GPIO Mode = 0, 1, 2, 3	ULP GPIO Mode = 4, 5, 6, 7	ULP GPIO Mode = 8, 9, 10, 11
ULPPERH_ON_SOC_GPIO_0	0: ULP_EGPIO[0] 1: ULP_SSI_CLK 2: ULP_I2S_DIN 3: ULP_UART_RTS	4: ULP_I2C_SDA 5: 6: 7:	8: 9: 10: 11:
ULPPERH_ON_SOC_GPIO_1	0: ULP_EGPIO[1] 1: ULP_SSI_DOUT 2: ULP_I2S_DOUT 3: ULP_UART_CTS	4: ULP_I2C_SCL 5: Timer0 6: 7:	8: 9: 10: 11:
ULPPERH_ON_SOC_GPIO_2	0: ULP_EGPIO[2] 1: ULP_SSI_DIN 2: ULP_I2S_WS 3: ULP_UART_RX	4: 5: COMP1_OUT 6: 7:	8: 9: 10: 11:
ULPPERH_ON_SOC_GPIO_3	0: ULP_EGPIO[3] 1: ULP_SSI_CS0 2: ULP_I2S_CLK 3: ULP_UART_TX	4: COMP2_OUT 5: 6: 7:	8: 9: 10: 11:
ULPPERH_ON_SOC_GPIO_4	0: ULP_EGPIO[4] 1: ULP_SSI_CS1 2: ULP_I2S_WS 3: ULP_UART_RTS	4: ULP_I2C_SDA 5: 6: 7:	8: ULP_SSI_CLK 9: Timer0 10: IR_INPUT 11:
ULPPERH_ON_SOC_GPIO_5	0: ULP_EGPIO[5] 1: IR_OUTPUT 2: ULP_I2S_DOUT 3: ULP_UART_CTS	4: ULP_I2C_SCL 5: AUX_ULP_TRIG_0 6: 7:	8: ULP_SSI_DOUT 9: Timer1 10: IR_OUTPUT 11:
ULPPERH_ON_SOC_GPIO_6	0: ULP_EGPIO[6] 1: ULP_SSI_CS2 2: ULP_I2S_DIN 3: ULP_UART_RX	4: ULP_I2C_SDA 5: 6: 7:	8: ULP_SSI_DIN 9: COMP1_OUT 10: AUX_ULP_TRIG_0 11:
ULPPERH_ON_SOC_GPIO_7	0: ULP_EGPIO[7] 1: IR_INPUT 2: ULP_I2S_CLK 3: ULP_UART_TX	4: ULP_I2C_SCL 5: Timer1 6: 7:	8: ULP_SSI_CS0 9: COMP2_OUT 10: AUX_ULP_TRIG_1 11:

ULP_GPIO	ULP GPIO Mode = 0, 1, 2, 3	ULP GPIO Mode = 4, 5, 6, 7	ULP GPIO Mode = 8, 9, 10, 11
ULPPERH_ON_SOC_GPIO_8	0: ULP_EGPIO[8] 1: ULP_SSI_CLK 2: ULP_I2S_CLK 3: ULP_UART_CTS	4: ULP_I2C_SCL 5: Timer0 6: 7:	8: 9: 10: 11:
ULPPERH_ON_SOC_GPIO_9	0: ULP_EGPIO[9] 1: ULP_SSI_DIN 2: ULP_I2S_DIN 3: ULP_UART_RX	4: ULP_I2C_SDA 5: COMP1_OUT 6: 7:	8: 9: 10: 11:
ULPPERH_ON_SOC_GPIO_10	0: ULP_EGPIO[10] 1: ULP_SSI_CS0 2: ULP_I2S_WS 3: ULP_UART_RTS	4: IR_INPUT 5: 6: 7:	8: 9: 10: 11:
ULPPERH_ON_SOC_GPIO_11	0: ULP_EGPIO[11] 1: ULP_SSI_DOUT 2: ULP_I2S_DOUT 3: ULP_UART_TX	4: ULP_I2C_SDA 5: AUX_ULP_TRIG_0 6: 7:	8: 9: 10: 11:

6.4 Valid GPIO Sets for Peripherals

Functions can be split pin wise across all GPIOs except for below restrictions. For synchronous interfaces there are some restrictions on clubbing of GPIOs into synchronous buses to ensure the timings mentioned in section SiWG917 module specifications. For example a single synchronous interface should not be split across ULP & SoC GPIOs. Table 6.11 Peripheral Interface Options on page 80 shows recommended locations for each function. For GPIO mode related information refer to 6.3 GPIO Pin Multiplexing .

Table 6.11. Peripheral Interface Options

ULP SSI (Synchronous Serial Interface) Primary		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_SSI_CLK	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_8	GPIO_6 / GPIO_46
ULP_SSI_CS0	ULP_GPIO_7	GPIO_48
ULP_SSI_CS1	ULP_GPIO_4	GPIO_10
ULP_SSI_CS2	ULP_GPIO_6	GPIO_12
ULP_SSI_DIN	ULP_GPIO_2 / ULP_GPIO_6 / ULP_GPIO_9	GPIO_8 / GPIO_47
ULP_SSI_DOUT	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_11	GPIO_7 / GPIO_49
ULP I2S Primary/Secondary		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_I2S_CLK	ULP_GPIO_7 / ULP_GPIO_8	GPIO_15 / GPIO_46
ULP_I2S_WS	ULP_GPIO_4	GPIO_8 / GPIO_10 / GPIO_48
ULP_I2S_DIN	ULP_GPIO_0 / ULP_GPIO_6 / ULP_GPIO_9	GPIO_6 / GPIO_12 / GPIO_47
ULP_I2S_DOUT	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_11	GPIO_7 / GPIO_11 / GPIO_49
ULP I2C INTERFACE		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_I2C_SCL	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_7 / ULP_GPIO_8	GPIO_7 / GPIO_11 / GPIO_15 / GPIO_46
ULP_I2C_SDA	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_6 / ULP_GPIO_9 / ULP_GPIO_11	GPIO_6 / GPIO_10 / GPIO_12 / GPIO_47 / GPIO_49
ULP UART INTERFACE		

IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
ULP_UART_TX	ULP_GPIO_7 / ULP_GPIO_11	GPIO_9 / GPIO_15 / GPIO_49
ULP_UART_RX	ULP_GPIO_2 / ULP_GPIO_6 / ULP_GPIO_9	GPIO_8 / GPIO_12 / GPIO_47
ULP_UART_CTS	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_8	GPIO_7 / GPIO_11 / GPIO_46
ULP_UART_RTS	ULP_GPIO_0 / ULP_GPIO_4	GPIO_6 / GPIO_10 / GPIO_48
Timer Interrupt Interface		
IO Functionality	Combinations possible on ULP GPIOs	Combinations possible on SoC GPIOs
Timer0	ULP_GPIO_4 / ULP_GPIO_8	GPIO_46
Timer1	ULP_GPIO_5 / ULP_GPIO_7	GPIO_15
Timer2	ULP_GPIO_1	GPIO_7
MCU SSI (Synchronous Serial Interface) Primary[1]		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SSI_MST_CLK	GPIO_8 / GPIO_25 / GPIO_52	
SSI_MST_CS0	GPIO_9 / GPIO_28 / GPIO_53	
SSI_MST_CS1	GPIO_10	
SSI_MST_CS2	GPIO_15 / GPIO_50	
SSI_MST_CS3	GPIO_51	
SSI_MST_DATA0	GPIO_11 / GPIO_26 / GPIO_56	
SSI_MST_DATA1	GPIO_12 / GPIO_27 / GPIO_57	
SSI_MST_DATA2	GPIO_6 / GPIO_29 / GPIO_54	
SSI_MST_DATA3	GPIO_7 / GPIO_30 / GPIO_55	
MCU SSI (Synchronous Serial Interface) Secondary[1]		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SSI_SLV_CLK	GPIO_8 / GPIO_26 / GPIO_47 / GPIO_52	
SSI_SLV_CS	GPIO_9 / GPIO_25 / GPIO_46 / GPIO_53	
SSI_SLV_MISO	GPIO_11 / GPIO_28 / GPIO_49 / GPIO_57	

SSI_SLV_MOSI	GPIO_10 / GPIO_27 / GPIO_48 / GPIO_56	
GSPI (General SPI) Interface[2]		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
GSPI_CLK	GPIO_8 / GPIO_25 / GPIO_46 / GPIO_52	
GSPI_CS0	GPIO_9 / GPIO_28 / GPIO_49 / GPIO_53	
GSPI_CS1	GPIO_10 / GPIO_29 / GPIO_50 / GPIO_54	
GSPI_CS2	GPIO_15 / GPIO_30 / GPIO_51 / GPIO_55	
GSPI_MISO	GPIO_11 / GPIO_26 / GPIO_47 / GPIO_56	
GSPI_MOSI	GPIO_6 / GPIO_12 / GPIO_27 / GPIO_48 / GPIO_57	
QSPI (Quad SPI) Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
M4SS_QSPI_CLK	GPIO_8 / GPIO_46 / GPIO_52	
M4SS_QSPI_CSN0	GPIO_7 / GPIO_49 / GPIO_55	
M4SS_QSPI_CSN1	GPIO_7 / GPIO_53	
M4SS_QSPI_D0	GPIO_6 / GPIO_47 / GPIO_53	
M4SS_QSPI_D1	GPIO_9 / GPIO_48 / GPIO_54	
M4SS_QSPI_D2	GPIO_10 / GPIO_50 / GPIO_56	
M4SS_QSPI_D3	GPIO_11 / GPIO_51 / GPIO_57	
M4SS_QSPI_D4	GPIO_54	
M4SS_QSPI_D5	GPIO_55	
M4SS_QSPI_D6	GPIO_56	
M4SS_QSPI_D7	GPIO_57	
QSPI_PSRAM Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
M4SS_PSRAM_CLK	GPIO_46 / GPIO_52	
M4SS_PSRAM_CSN0	GPIO_49 / GPIO_55	
M4SS_PSRAM_D0	GPIO_47 / GPIO_53	
M4SS_PSRAM_D1	GPIO_48 / GPIO_54	

M4SS_PSRAM_D2	GPIO_50 / GPIO_56	
M4SS_PSRAM_D3	GPIO_51 / GPIO_57	
I2S Primary/Secondary		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
I2S0_CLK	GPIO_8 / GPIO_25 / GPIO_46 / GPIO_52	
I2S0_WS	GPIO_9 / GPIO_26 / GPIO_47 / GPIO_53	
I2S0_DIN_0	GPIO_10 / GPIO_27 / GPIO_48 / GPIO_56	
I2S0_DIN_1	GPIO_6 / GPIO_29 / GPIO_50 / GPIO_54	
I2S0_DOUT_0	GPIO_11 / GPIO_28 / GPIO_49 / GPIO_57	
I2S0_DOUT_1	GPIO_7 / GPIO_30 / GPIO_51 / GPIO_55	
I2C0 INTERFACE		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
I2C0_SCL	GPIO_7 / JTAG_TDI	ULP_GPIO_1 / ULP_GPIO_11
I2C0_SDA	GPIO_6 / JTAG_TCK_SWCLK	ULP_GPIO_0
I2C1 INTERFACE		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
I2C1_SCL	GPIO_6 / JTAG_TMS_SWDIO / GPIO_50 / GPIO_54	ULP_GPIO_0 / ULP_GPIO_6
I2C1_SDA	GPIO_7 / JTAG_TDO_SWO / GPIO_51 / GPIO_55	ULP_GPIO_1 / ULP_GPIO_7
MCPWM Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
PWM_0H	GPIO_7	ULP_GPIO_1
PWM_0L	GPIO_6	ULP_GPIO_0
PWM_1H	GPIO_9	ULP_GPIO_5
PWM_1L	GPIO_8	ULP_GPIO_2 / ULP_GPIO_4
PWM_2H	GPIO_11	ULP_GPIO_5
PWM_2L	GPIO_10	ULP_GPIO_4
PWM_3H	GPIO_15	ULP_GPIO_7
PWM_3L	GPIO_12	ULP_GPIO_6
PWM_FAULTA	GPIO_25	ULP_GPIO_4 / ULP_GPIO_9

PWM_FAULTB	GPIO_26	ULP_GPIO_5
PWM_SLP_EVENT_TRIG		ULP_GPIO_8
PWM_TMR_EXT_TRIG_1	GPIO_27 / GPIO_51	ULP_GPIO_6 / ULP_GPIO_11
PWM_TMR_EXT_TRIG_2	GPIO_28 / GPIO_54	ULP_GPIO_1 / ULP_GPIO_7
PWM_TMR_EXT_TRIG_3	GPIO_29 / GPIO_55	ULP_GPIO_8
PWM_TMR_EXT_TRIG_4	GPIO_30 / GPIO_50	ULP_GPIO_9
QEI Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
QEI_DIR	GPIO_11 / GPIO_28 / JTAG_TDO_SWO / GPIO_49 / GPIO_57	ULP_GPIO_7 / ULP_GPIO_11
QEI_IDX	GPIO_8 / GPIO_25 / JTAG_TCK_SWCLK/ GPIO_46 / GPIO_52	ULP_GPIO_0 / ULP_GPIO_4 / ULP_GPIO_8
QEI_PHA	GPIO_9 / GPIO_26 / JTAG_TDI / GPIO_47 / GPIO_53	ULP_GPIO_1 / ULP_GPIO_5 / ULP_GPIO_9
QEI_PHB	GPIO_10 / GPIO_27 / JTAG_TMS_SWDIO / GPIO_48 / GPIO_56	ULP_GPIO_6
USART0		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
USART0_CLK	GPIO_8 / GPIO_25 / GPIO_52	ULP_GPIO_0
USART0_CTS	GPIO_6 / GPIO_26 / GPIO_56	ULP_GPIO_6
USART0_RTS	GPIO_9 / GPIO_28 / GPIO_53	ULP_GPIO_5
USART0_DCD	GPIO_12 / GPIO_29	
USART0_DSR	GPIO_11 / GPIO_57	
USART0_DTR	GPIO_7	
USART0_IR_RX	GPIO_25 / GPIO_47	ULP_GPIO_0 / ULP_GPIO_7
USART0_IR_TX	GPIO_26 / GPIO_48	ULP_GPIO_1 / ULP_GPIO_8
USART0_RI	GPIO_27 / GPIO_46	ULP_GPIO_4
USART0_RS485_DE	GPIO_29 / GPIO_51	ULP_GPIO_7 / ULP_GPIO_11
USART0_RS485_EN	GPIO_27 / GPIO_49	ULP_GPIO_5 / ULP_GPIO_9
USART0_RS485_RE	GPIO_28 / GPIO_50	ULP_GPIO_6
USART0_RX	GPIO_10 / GPIO_29 / GPIO_55	ULP_GPIO_1 / ULP_GPIO_6
USART0_TX	GPIO_15 / GPIO_30 / GPIO_54	ULP_GPIO_4 / ULP_GPIO_7
SCT		

IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
SCT_IN_0	GPIO_25	ULP_GPIO_0 / ULP_GPIO_4
SCT_OUT_0	GPIO_29	ULP_GPIO_4
SCT_OUT_1	GPIO_30	ULP_GPIO_5
UART1 INTERFACE		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
UART1_TX	GPIO_7 / GPIO_30	ULP_GPIO_5 / ULP_GPIO_9 / ULP_GPIO_11
UART1_RX	GPIO_6 / GPIO_29	ULP_GPIO_4 / ULP_GPIO_8
UART1_CTS	GPIO_11 / GPIO_28 / GPIO_51	ULP_GPIO_7 / ULP_GPIO_1 / ULP_GPIO_9
UART1_RTS	GPIO_10 / GPIO_27 / GPIO_50	ULP_GPIO_6 / ULP_GPIO_0 / ULP_GPIO_8
UART1_RS485_EN	GPIO_12 / GPIO_26	ULP_GPIO_0
UART1_RS485_RE	GPIO_8	ULP_GPIO_1
UART1_RS485_DE	GPIO_9	ULP_GPIO_11
M4SS TRACE		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
M4SS_TRACE_CLKIN	GPIO_6 / GPIO_15 / GPIO_46 / GPIO_52	
M4SS_TRACE_CLK	GPIO_7 / GPIO_47 / GPIO_53	
M4SS_TRACE_D0	GPIO_8 / GPIO_48 / GPIO_54	
M4SS_TRACE_D1	GPIO_9 / GPIO_49 / GPIO_55	
M4SS_TRACE_D2	GPIO_10 / GPIO_50 / GPIO_56	
M4SS_TRACE_D3	GPIO_11 / GPIO_51 / GPIO_57	
Miscellaneous Interface		
IO Functionality	Combinations possible on SoC GPIOs	Combinations possible on ULP GPIOs
MCU_CLK_OUT	GPIO_11 / GPIO_12 / GPIO_15	

Note:

1. For SSI (Synchronous Serial Interface) use the combinations on SoC GPIOs from these set of GPIOs only – GPIO_8 to GPIO_15, GPIO_25 to GPIO_30, GPIO_46 to GPIO_51 and GPIO_52 to GPIO_57.
2. For GSPI (General SPI) use the combinations on SoC GPIOs from these set of GPIOs only – GPIO_6 to GPIO_15, GPIO_25 to GPIO_30, GPIO_46 to GPIO_51 and GPIO_52 to GPIO_57.

6.5 Functional Description

6.5.1 Digital Functions

Table 6.12. Digital Functions

Pin Name	Direction	Description
GSPI (General SPI) Interface		
GSPI_CLK	Output	Output Clock from the GSPI primary to external secondary
GSPI_CS0 to GSPI_CS2	Output	Active low chip select. GSPI primary can select a maximum of 3 secondaries.
GSPI_MISO	Input	Input data to primary from external secondaries
GSPI_MOSI	Output	Output data from primary to external secondary
I2C (Inter-integrated Circuit) Interface		
I2C0_SCL I2C1_SCL ULP_I2C_SCL	Inout	I2C Serial Clock
I2C0_SDA I2C1_SDA ULP_I2C_SDA	Inout	I2C Serial Data
2 Channel I2S (Inter-IC Sound) Interface		
I2S0_CLK ULP_I2S_CLK	Output/ Input	I2S Clock Output in Primary Mode and Input in Secondary Mode
I2S0_WS ULP_I2S_WS	Output/ Input	Active high I2S Word Select Output in Primary Mode and Input in Secondary Mode
I2S0_DIN_0 to I2S0_DIN_1 ULP_I2S_DIN	Input	I2S Input Data
I2S0_DOUT_0 to I2S0_DOUT_1 ULP_I2S_DOUT	Output	I2S Output Data
QSPI (Quad SPI) Interface		
MCU_QSPI_CLK	Output	Output clock to the external SPI secondary.
MCU_QSPI_CSN0 to MCU_QSPI_CSN1	Output	Active Low Chip Select to select a maximum of two secondaries.
MCU_QSPI_D0 to MCU_QSPI_D7	Inout	QSPI Data. Supports both QUAD and OCTA Data. In Quad Mode, only Bits M4SS_QSPI_D0 to M4SS_QSPI_D3 are valid. In Octa Mode, all the bits are valid
QSPI_PSRAM		
M4SS_PSRAM_CLK	Output	Output clock to the external PSRAM.
M4SS_PSRAM_CSN0	Output	Active Low Chip Select to select a maximum of two secondaries.
M4SS_PSRAM_D0 to M4SS_PSRAM_D3	Inout	QSPI Data. Supports QUAD Data only. In Quad Mode, only Bits M4SS_QSPI_D0 to M4SS_QSPI_D3 are valid.
MCPWM (Pulse Width Modulation) Interface		

Pin Name	Direction	Description
PWM_xH	Output	PWM output signals. The output pins are grouped in pairs, to facilitate driving the low side and high side of a power half-bridge. x = 0,1,2,3
PWM_xL	Output	
PWM_FAULTA	Input	External fault signal A
PWM_FAULTB	Input	External fault signal B
PWM_SLP_EVENT_TRIG	Output	Special event trigger for synchronizing analog to digital conversions.
PWM_TMR_EXT_TRIG_1 to PWM_TMR_EXT_TRIG_4	Input	External trigger for base timers to increment. Each Channel has separate trigger input.
QEI (Quadrature Encode Interface)		
QEI_DIR	Output	Position counter direction. '1' means counter direction is positive. '0' means counter direction is negative.
QEI_IDX	Input	QE Index. Index pulse occurs once per mechanical revolution and is used as a reference to indicate an absolute position.
QEI_PHA	Input	QE Phase A input
QEI_PHB	Input	QE Phase B input
SCT (State Configurable Timer) Interface		
SCT_IN_0	Input	Timer input event
SCT_OUT_0 to SCT_OUT_1	Output	Timer output event
SSI (Synchronous Serial Interface) Primary		
SSI_MST_CLK ULP_SSI_CLK	Output	Output clock from SSI Primary
SSI_MST_CS0 to SSI_MST_CS3 ULP_SSI_CS0 to ULP_SSI_CS2	Output	Active Low Chip select
SSI_MST_DATA0 to SSI_MST_DATA3	Inout	Single Bit Mode: DATA0 = Input Data, DATA1 = Output Data Quad Bit Mode: Bidirectional Data
ULP_SSI_DOUT	Output	Primary Output Data
ULP_SSI_DIN	Input	Primary Input Data
SSI (Synchronous Serial Interface) Secondary		
SSI_SLV_CLK	Input	Input clock to SSI Secondary
SSI_SLV_CS	Input	Active Low Chip select
SSI_SLV_MISO	Output	Secondary Output Data
SSI_SLV_MOSI	Input	Secondary Input Data
SYSRTC (System Real Time Clock) Interface		
SYSRTC_PRS_IN_G0	Input	Group 0 input to trigger capture operation
SYSRTC_PRS_IN_G1	Input	Group 1 input to trigger capture operation
SYSRTC_PRS_OUT_G0_0	Output	Group 0 compare 0 match interrupt
SYSRTC_PRS_OUT_G0_1	Output	Group 0 compare 1 match interrupt
SYSRTC_PRS_OUT_G1_0	Output	Group 1 compare 0 match interrupt

Pin Name	Direction	Description
SYSRTC_PRS_OUT_G1_1	Output	Group 1 compare 1 match interrupt
UART (Universal Asynchronous Receiver Transmitter) Interface		
UART1_CTS, ULP_UART_CTS	Input	Active low Clear to Send
UART1_RTS, ULP_UART_RTS	Output	Active low Request to Send
UART1_RS485_DE	Output	Driver Enable. Polarity is programmable.
UART1_RS485_EN	Output	Active High RS485 Enable
UART1_RS485_RE	Output	Receiver Enable. Polarity is programmable.
UART1_RX, ULP_UART_RX	Input	Serial Input
UART1_TX, ULP_UART_TX	Output	Serial Output
USART (Universal Synchronous Asynchronous Receiver Transmitter) Interface		
USART0_CLK	Inout	Serial interface clock
USART0_CTS	Input	Active low Clear to Send
USART0_RTS	Output	Active low Request to Send
USART0_DCD	Input	Active low Data Carrier Detect
USART0_DSR	Input	Active low Data Set Ready
USART0_DTR	Output	Active low Data Terminal Ready
USART0_IR_RX	Input	IrDA SIR Input
USART0_IR_TX	Output	IrDA SIR Output
USART0_RI	Input	Active low Ring Indicator
UART0_RS485_DE	Output	Driver Enable. Polarity is programmable.
UART0_RS485_EN	Output	Active High RS485 Enable
UART0_RS485_RE	Output	Receiver Enable. Polarity is programmable.
USART0_RX	Input	Serial Input
USART0_TX	Output	Serial Output
Timers Interrupt Interface		
Timer0, Timer1,Timer2	Output	Active-high interrupts from Timers
Miscellaneous Interface		
MCU_CLK_OUT	Output	All the Clocks that are used by Cortex-M4 SoC are multiplexed and connected on this pin
ULP_EGPIO_*	Inout	ULP GPIOs controlled by Cortex M4 Processor. * represents 0,1,2,4,5,6,7,8,9,10,11
AUX_ULP_TRIG_0, AUX_ULP_TRIG_1	Input	External trigger to ADC.
NWP_GPIO_*	Inout	NWP GPIOs controlled by Network Wireless Processor. * represents 6,8,9,10,11,12,15,46,47,48,49,50,51

Pin Name	Direction	Description
UULP VBAT Pin Interface		
XTAL_32KHZ_IN	Input	Low Frequency clock input from an External 32 kHz Crystal oscillator
MCU_GPIO0/1/2/3_WAKEUP	Input	GPIOs that can be used as Wakeup interrupt to MCU while in Retention or Deep sleep mode
NWP_GPIO0/1_WAKEUP	Input	GPIOs that can be used to wake the Network Processor
MCU_GPIO_TOGGLE	Input	Input pulse counting function
TRACE Pins		
M4SS_TRACE_CLKIN	Input	
M4SS_TRACE_CLK	Output	
M4SS_TRACE_D0	Output	Trace Packet, bit 0.
M4SS_TRACE_D1	Output	Trace Packet, bit 1
M4SS_TRACE_D2	Output	Trace Packet, bit 2
M4SS_TRACE_D3	Output	Trace Packet, bit 3

6.5.2 Analog Functions

Table 6.13. Analog Functions

Pin Name	Direction	Description
ADC Interface		
ADCP[0] - ADCP[18]	Input	The 18 single ended input channels that are multiplexed onto the ADCP positive input These can be used alone for single-ended measurements, or selected with ADCN inputs for differential measurements
ADCN[0] - ADCN[8]	Input	The 9 channels that are multiplexed onto the ADCN negative input. These are used together with ADCP inputs for differential measurements
DAC Interface		
DAC0, DAC1	Output	Possible output pins from the internal DAC
OpAmp Interface		
OPAMPxyz	Input	Multiplexed inputs of the three OpAmps. xyz denote the OpAmp number, the terminal and the multiplexing on that pin of the OpAmp x = OpAmp number (1, 2 or 3) y = P or N terminal of OpAmp z = 0, 1, 2, 3, 4, 5 (Multiplexing at OpAmp input pin). Note that OPAMP1P is available at 6 locations, OPAMP2P, 3P and 1N are available at 2 locations each and OPAMP2N and 3N pins are available at only one location
OPAMP1OUT0/1, OPAMP2/3OUT0	Output	Outputs of the three OpAmps. Note that OPAMP1 output is available at two possible pin locations whereas OPAMP2 and 3 outputs are available at a fixed pin
Comparator Interface		

Pin Name	Direction	Description
COMPx_yz		Multiplexed inputs of the two Comparators. xyz denote the Comparator number, the terminal and the multiplexing on that pin of the Comparator x = Comparator number (1 or 2) y = P or N terminal of OpAmp z = 0, 1 (Multiplexing at Comparator Input pin). Note that each input pin of both comparators is available on two possible GPIO pins.

7. Electrical Specifications

7.1 Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions beyond those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at https://www.silabs.com/about-us/quality.

Table 7.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature	T_{store}		-40	—	125	ºC
Maximum junction temperature	$T_{j(max)}$			—	125	ºC
3.3V power supply for the on-chip Buck, RF circuit, and UULP IOs	VBATT		-0.5	—	3.63	V
I/O supply for GPIOs	IO_VDD		-0.5	—	3.63	V
I/O supply for SDIO I/Os	SDIO_IO_VDD		-0.5	—	3.63	V
I/O supply for QSPI flash signals	FLASH_IO_VDD		-0.5	—	3.63	V
I/O supply for ULP I/Os	ULP_IO_VDD		-0.5	—	3.63	V
DC voltage on any I/O pin [1]	V_{IO_PIN}		-0.5	—	VDD + 0.5	V
Total average max current into chip	I_{pmax}		—	—	500	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	100	mA
		Source	—	—	100	mA

Note:

1. VDD = I/O supply domain pin. Refer to pin description tables for supply domain associated with each I/O.

7.2 Recommended Operating Conditions

Note: The device may operate continuously at the maximum allowable ambient $T_{ambient}$ rating as long as the maximum junction $T_{junction(max)}$ is not exceeded. For an application with significant power dissipation, the allowable $T_{ambient}$ may be lower than the maximum $T_{ambient}$ rating. $T_{ambient} = T_{junction(max)} - (\Theta_{JA}$ x Power Dissipation). Refer to the Thermal Characteristics table for Θ_{JA}.

Table 7.2. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Ambient temperature	$T_{ambient}$		-40	25	85	ºC
Junction temperature	$T_{junction}$				105	ºC
3.3V power supply for the on-chip Buck, RF Power Amplifier, UULP I/Os	VBATT		3.0	3.3	3.63	V
I/O supply for Flash	FLASH_IO_VDD		1.71	1.8	1.98	V
I/O supply for GPIOs	IO_VDD[1]	1.8 V nominal operation	1.71	1.8	1.98	V
		3.3 V nominal operation	2.97	3.3	3.63	
I/O supply for SDIO I/Os	SDIO_IO_VDD[1]	1.8 V nominal operation	1.71	1.8	1.98	V
		3.3 V nominal operation	2.97	3.3	3.63	
I/O supply for ULP I/Os	ULP_IO_VDD[1]	1.8 V nominal operation	1.71	1.8	1.98	V
		3.3 V nominal operation	2.97	3.3	3.63	

Note:

1. Supplies can operate at a nominal 3.3 V or 1.8 V level independent of the other supplies in the system.

7.3 DC Characteristics

7.3.1 RESET_N Pin and POC_IN Pins

Table 7.3. RESET_N Pin and POC_IN Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level input voltage	V_{IH}	RESET_N pin, VBATT = 3.3 V	0.8 * VBATT	—	—	V
		POC_IN pin, VBATT = 3.3 V	2.76	—	—	V
Low level input voltage	V_{IL}	RESET_N pin, VBATT = 3.3 V	—	—	0.3 * VBATT	V
		POC_IN pin, VBATT = 3.3 V	—	—	1.10	V

7.3.2 Power On Control (POC) and Reset

There are three signals involved in power-on control and reset of the device:

- POC_IN: When pulled low, POC_IN will reset all of the internal blocks in the device. The POC_IN signal can be controlled either by external circuitry, by POC_OUT, or both.
- RESET_N: RESET_N is an open-drain signal which will be pulled low during a chip reset. It is released after POC_IN is high. RESET_N should be connected to an RC circuit to fulfill the timing requirements shown in Figure 7.1 Power Up Sequence on page 93.
- POC_OUT: The POC_OUT signal is the output of the internal blackout supply monitor. POC_OUT is distributed to all I/O cells to prevent the I/O cells from powering up in an undesired configuration and is also used inside the IC to place the IC in a safe state until a valid supply is available for proper operation. During power up, POC_OUT stays low until the VBATT reaches 1.6 V. After the VBATT supply exceeds 1.6 V, POC_OUT becomes high and normal operation begins. If VBATT becomes lower than the blackout threshold voltage, POC_OUT will return low. POC_OUT can be used to provide chip reset by connecting to POC_IN in a loopback configuration.

The recommended schematic for the reset signals is shown in Reset Configuration..

Figure 7.1 Power Up Sequence on page 93 shows the signal timing when POC_OUT, POC_IN, and RESET_N are connected per the recommended schematic. The POC_IN-to-RESET_N delay will occur when POC_IN transitions from low to high.

In this configuration the system only has to control the supply (VBATT) during power-up and power down and need not control POC_IN externally. On power-up the chip will be reset internally. The power-down sequence will follow VBATT and external control of POC_IN is not required.

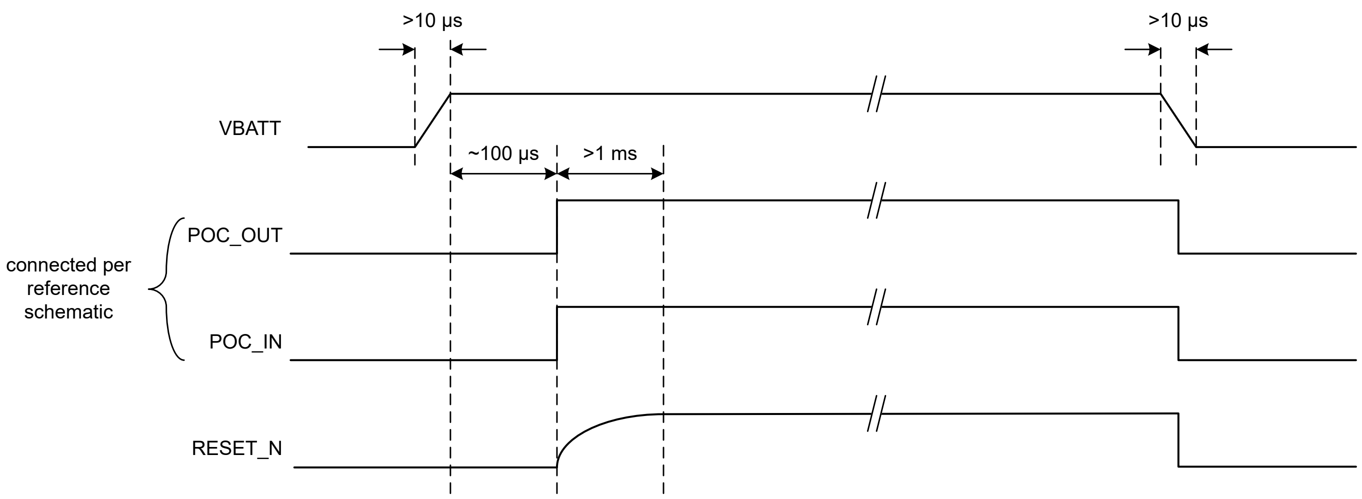


Figure 7.1. Power Up Sequence

If the chip is to be reset from an external host device while powered up, the POC_IN signal should be pulled low for at least 10 ms as shown in Figure 7.2 External Reset via POC_IN on page 93. Upon release of POC_IN, the POC_IN-to-RESET_N delay will occur.

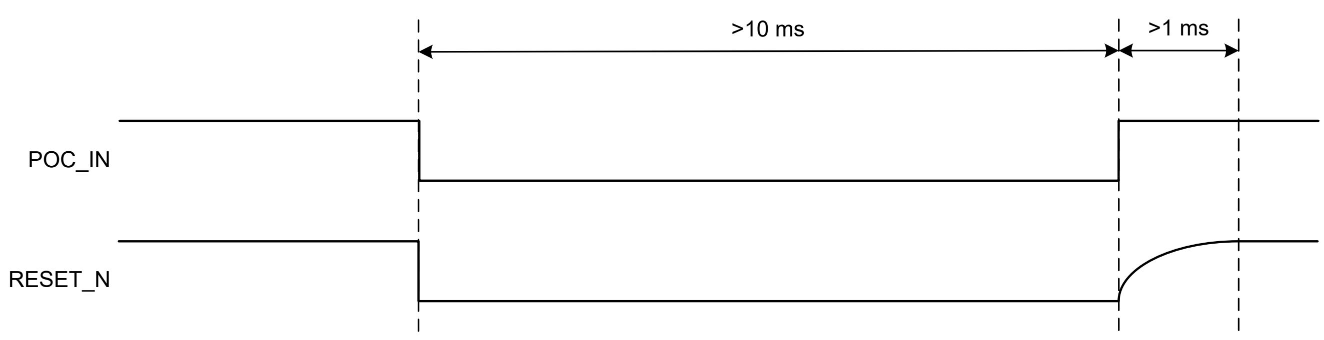


Figure 7.2. External Reset via POC_IN

In the above timing diagrams, it is assumed that all supplies including VBATT are connected together. If they are not connected together and independently controlled, then the guidance below must be followed.

- **Case1**: POC_OUT is looped back and there is no external control for POC_IN
  - All supplies can be enabled at the same time, if possible
  - If supplies cannot be enabled at the same time, the VBATT supplies should be powered up first and all other supplies should be powered on at least 1 ms before RESET_N is high. The RC circuit controlling RESET_N must be adjusted to provide the appropriate delay.
  - While powering down, supplies can be powered off simultaneously, or with VBATT the last to be disabled.
- **Case2**: POC_OUT is looped back and there is external control for POC_IN during power-up / power-down.
  - All supplies can be enabled at the same time, or VBATT may be enabled before other supplies.
  - POC_IN should be kept low for at least 600 us after all the supplies have settled.
  - On power-down, POC_IN can be driven low before disabling the supplies. Supplies can be powered off simultaneously, or with VBATT the last to be disabled.

7.3.3 Blackout Monitor

The blackout comparator is enabled by default upon power up. Blackout is typically asserted when the VBATT supply goes lower than 1.6 V (see Table 7.4 Blackout Monitor Electrical Specifications on page 95), and it is de-asserted when VBATT supply goes higher than 1.625 V. The blackout monitor circuit will reset the device when POC_OUT is connected to POC_IN as recommended.

The blackout monitor will be disabled after power up. The functionality should be enabled by the SoC firmware if required in the system. The blackout monitor block should be enabled to monitor the VBATT voltage only in high power modes. In low power modes battery level detection can be implemented using the Nano-Power Brownout detection comparator.

When the system is in low power mode, the blackout comparator is automatically enabled upon a brownout event.

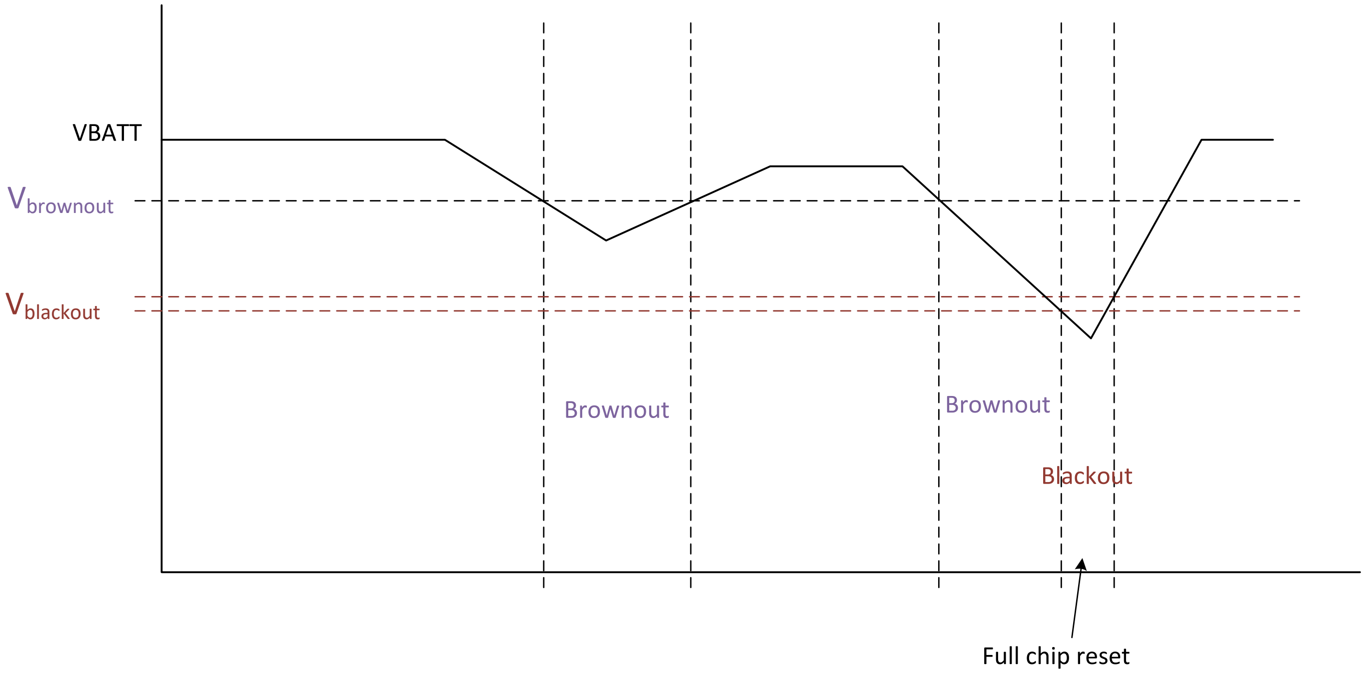


Figure 7.3. Blackout Monitor

Table 7.4. Blackout Monitor Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VBATT voltage at which the Blackout monitor resets the IC	$VTL_{blackout}$		—	1.56	1.65	V
VBATT voltage at which the Blackout monitor releases the IC from reset	$VTH_{blackout}$		—	1.59	1.675	V

7.3.4 Nano Power Comparator and Brown Out Detection (BOD)

The Nano Power comparator subsystem consists of a sampled comparator, reference buffer and resistor bank.

Features

- Battery voltage measurement
- Brownout detection
- Three button wakeup is supported using single VOLT_SENSE signal

Table 7.5. Nano Power BOD Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Battery status accuracy	V_{batt_status}		—	+/-100	—	mV
Brownout detection accuracy	V_{BOD}		—	+/-100	—	mV

7.3.5 Thermal Characteristics

Table 7.6. Thermal Characteristics

Package	Board	Parameter	Symbol	Test Condition (1)	Value	Units
Module	JEDEC- High Thermal Cond. (2s2p)	Thermal Resistance, Junction to Ambient	Θ_{JA}	Still Air (JESD51-2A)	66	°C/W

Note:

1. PCB: 76.2 mm x 114.3 mm x 1.6 mm (JEDEC High Effective); 2s2p = 2 signals, 2 planes.
2. The absolute maximum device currrent when transmitting at highest transmit power will not exceed 400 mA.

7.3.6 Digital I/O Signals

Table 7.7. Digital I/O Signals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level input voltage	V_{IH}	IO_VDDx = 3.3 V	2	—	—	V
		IO_VDDx = 1.8 V	1.17	—	—	V
Low level input voltage	V_{IL}	IO_VDDx = 3.3 V	—	—	0.8	V
		IO_VDDx = 1.8 V	—	—	0.63	V
Low level output voltage	V_{OL}		—	—	0.4	V
High level output voltage	V_{OH}		IO_VDDx - 0.4	—	—	V
Low level output current	I_{OL}	GPIO_* and ULP_GPIO_* pins	2	4	12	mA
		UULP_GPIO_*	1	—	2	mA
High level output current	I_{OH}	GPIO_* and ULP_GPIO_* pins	2	4	12	mA
		UULP_GPIO_*	1	—	2	mA

7.3.6.1 Open-Drain I2C Pins

Table 7.8. Open-Drain I2C Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High level input voltage	V_{IH}		0.7 * IO_VDDx	—	—	V
Low level input voltage	V_{IL}		—	—	0.3 * IO_VDDx	V

7.3.7 Flash LDO Electrical Specifications - Regulation Mode

Table 7.9. Flash LDO Electrical Specifications - Regulation Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage (VBATT)	V_{in}	Flash LDO in Regulation Mode	2.97	3.3	3.63	V
Output Voltage Range (1V8_LDO)	V_{out}		1.75	1.88	1.95	V
Load current	I_{load}		—	—	48	mA
Line Regulation	REG_{line}	V_{in} Changed from 2.97 V to 3.63 V	—	—	0.6	%
Load Regulation	REG_{load}	I_{load} changed from 0 mA to 48 mA	—	—	3	%

7.4 AC Characteristics

7.4.1 Clock Specifications

The SiWG917 modules require two primary clocks:

- Low frequency clock options for sleep manager and RTC
  - Internal 32 kHz RC clock may be used for applications with low timing accuracy requirements
  - 32.768 kHz LVCMOS rail-to-rail external oscillator input pin UULP_VBAT_GPIO_3 for external oscillator or host clock. **Required for MCU timing accuracy and all power-sensitive Wi-Fi, BLE, and Coex use cases.**
- High frequency 40 MHz clock for NWP, Cortex-M4, baseband subsystem and the radio
  - 40 MHz clock is integrated inside the module, and no external clock needs to be provided

7.4.1.1 Low Frequency Clock

Low-frequency clock selection can be done through software. The RC oscillator clock is not suited for high timing accuracy applications and may increase overall system current consumption in duty-cycled power modes.

32 kHz Internal RC Oscillator

Table 7.10. 32 kHz RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	F_{osc}			32.0		kHz
Frequency Variation across Temperature	F_{osc_Acc}			1.2		%

32.768 kHz External Oscillator

An external 32.768 kHz low-frequency clock can be fed through UULP_VBAT_GPIO_3.

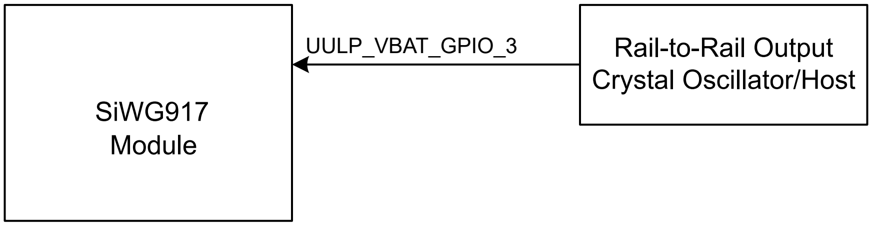


Figure 7.4. External 32.768 kHz Oscillator - Rail to Rail

Table 7.11. 32.768 kHz External Oscillator Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillator Frequency	f_{osc}		—	32.768	—	kHz
Frequency Variation with Temp and Voltage	f_{osc_Acc}		-100	—	100	ppm
Input duty cycle	DC_{in}		30	50	70	%
Input AC peak-peak voltage swing at input pin.	V_{AC}		-0.3	—	VBATT +/- 10%	Vpp

7.4.1.2 High-Frequency Crystal (HFXO)

Table 7.12. High-Frequency Crystal (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Oscillator Frequency	F_{osc}		—	40	—	MHz
Initial Calibrated Accuracy	F_{osc_Acc}		-5	—	+5	ppm
Frequency Variation across Temperature	F_{osc_Drift}		-14	—	+14	ppm

7.4.2 SDIO 2.0 Secondary

7.4.2.1 Full Speed Mode

Table 7.13. SDIO 2.0 Secondary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SDIO_CLK	f_{sdio_clk}		—	—	25	MHz
SDIO_DATA, SDIO_CMD input setup time	t_s		4	—	—	ns
SDIO_DATA, SDIO_CMD input hold time	t_h		1.2	—	—	ns
SDIO_DATA, clock to output delay	t_{od}		—	—	13	ns
Output Load	C_L		5	—	10	pF

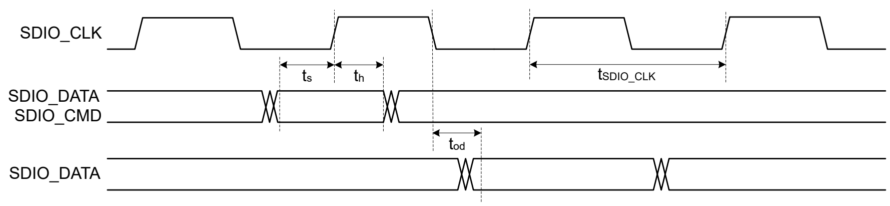


Figure 7.5. Interface Timing Diagram for SDIO 2.0 Secondary Full Speed Mode

7.4.2.2 High Speed Mode

Table 7.14. SDIO 2.0 Secondary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SDIO_CLK	f_{sdio_clk}		25	—	50	MHz
SDIO_DATA, input setup time	t_s		4	—	—	ns
SDIO_DATA, input hold time	t_h		1.2	—	—	ns
SDIO_DATA, clock to output delay	t_{od}		2.5	—	13	ns
Output Load	C_L		5	—	10	pF

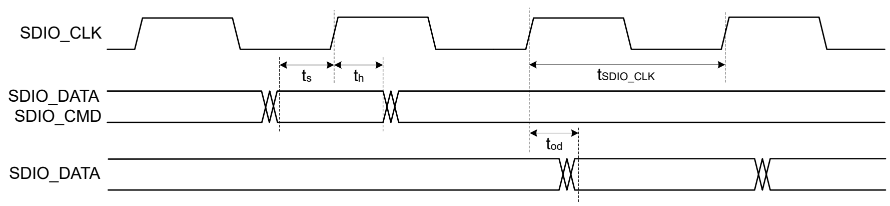


Figure 7.6. Interface Timing Diagram for SDIO 2.0 Secondary High Speed Mode

7.4.3 HSPI Secondary

7.4.3.1 Low Speed Mode

Table 7.15. HSPI Secondary Low Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HSPI_CLK	f_{hspi}		0	—	25	MHz
HSPI_CSN to output delay	t_{cs}		—	—	7.5	ns
HSPI_CSN to input setup time	t_{cst}		4.5	—	—	ns
HSPI_MOSI, input setup time	t_s		1.4	—	—	ns
HSPI_MOSI, input hold time	t_h		1.5	—	—	ns
HSPI_MISO, clock to output delay	t_{od}		—	—	8.75	ns
Output Load	C_L		5	—	10	pF

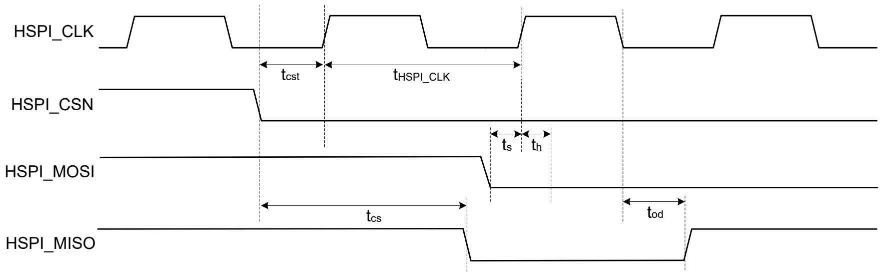


Figure 7.7. Interface Timing Diagram for HSPI Secondary Low Speed Mode

In low speed mode, HSPI_MISO data is driven on the falling edge of HSPI_CLK, and HSPI_MOSI is read on the rising edge of HSPI_CLK.

7.4.3.2 High Speed Mode

Table 7.16. HSPI Secondary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HSPI_CLK	f_{hspi}		25	—	80	MHz
HSPI_CSN to output delay	t_{cs}		—	—	7.5	ns
HSPI_CSN to input setup time	t_{cst}		4.5	—	—	ns
HSPI_MOSI, input setup time	t_s		1.4	—	—	ns
HSPI_MOSI, input hold time	t_h		1.4	—	—	ns
HSPI_MISO, clock to output delay	t_{od}		1.5	—	8.75	ns
Output Load	C_L		5	—	10	pF

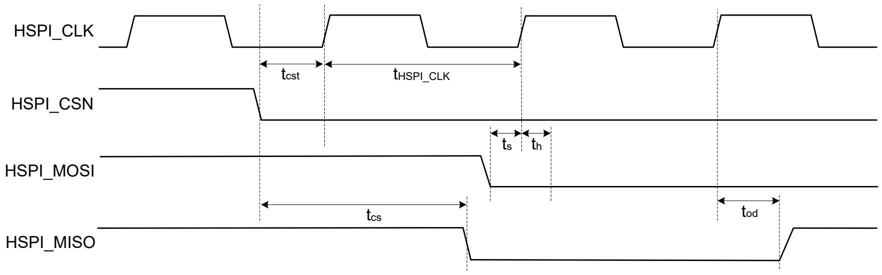


Figure 7.8. Interface Timing Diagram for HSPI Secondary High Speed Mode

In high speed mode, HSPI_MISO data is driven on the rising edge of HSPI_CLK, and HSPI_MOSI is read on the rising edge of HSPI_CLK.

7.4.3.3 Ultra High Speed Mode

Table 7.17. HSPI Secondary Ultra High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
HSPI_CLK	f_{hspi}		80	—	100	MHz
HSPI_MOSI, input setup time	t_s		1.4	—	—	ns
HSPI_MOSI, input hold time	t_h		1.4	—	—	ns
HSPI_MISO, clock to output delay	t_{od}		1.5	—	8.75	ns
Output Load	C_L		5	—	10	pF

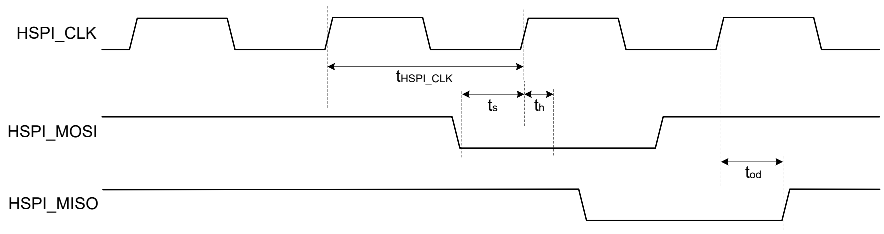


Figure 7.9. Interface Timing Diagram for HSPI Secondary Ultra High Speed Mode

In ultra high speed mode, HSPI_MISO data is driven on the rising edge of HSPI_CLK, and HSPI_MOSI is read on the rising edge of HSPI_CLK.

7.4.4 GPIO Pins

Table 7.18. GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise time	t_{rf}	Pin configured as output; SLEW = 1 (fast mode)	1	—	4	ns
Fall time	t_{ff}	Pin configured as output; SLEW = 1 (fast mode)	0.9	—	4	ns
Rise time	t_{rs}	Pin configured as output; SLEW = 0 (standard mode)	1.9	—	5	ns
Fall time	t_{fs}	Pin configured as output; SLEW = 0 (standard mode)	1.9	—	5	ns
Rise time	t_r	Pin configured as input	0.3	—	1.3	ns
Fall time	t_f	Pin configured as input	0.2	—	1.2	ns

7.4.5 In-Package Flash Memory

Table 7.19. In-Package Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Endurance	N_{endu}	Sector erase/program	10000	—	—	cycles
		Page erase/program, page in large sector	10000	—	—	cycles
		Page erase/program, page in small sector	10000	—	—	cycles
Retention time	t_{ret}	Powered	10	—	—	years
		Unpowered	10	—	—	years
Block Erase time (32 KB)	t_{er}	Page, sector or multiple consecutive sectors	—	150	1400	ms
Page programming time	t_{prog}		—	0.5	3	ms
Chip Erase time	t_{ce}		—	20	65	s

7.4.6 QSPI

7.4.6.1 Full Speed Mode (Rising Edge Sampling)

Table 7.20. QSPI Full Speed Mode (Rising Edge Sampling)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
qspi_clk	f_{qspi}		0	—	40	MHz
qspi_cs, to clock edge(this is achieved functionally)	t_{cs}		8.6	—	—	ns
qspi_miso, setup time	t_s		4	—	—	ns
qspi_miso, hold time	t_h		2.5	—	—	ns
qspi_mosi, clock to output valid	t_{od}		-2	—	2	ns
Output Load	C_L		5	—	10	pF

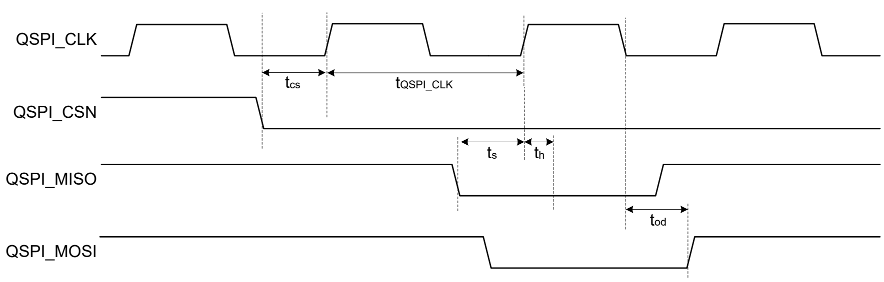


Figure 7.10. Interface Timing Diagram for QSPI Full Speed Mode (Rising Edge Sampling)

7.4.6.2 High Speed Mode (Falling Edge Sampling)

Table 7.21. QSPI High Speed Mode (Falling Edge Sampling)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
qspi_clk	f_{qspi}		40	—	80	MHz
qspi_cs, to clock edge(this is achieved functionally)	t_{cs}		4.3	—	—	ns
qspi_miso, setup time	t_s		4	—	—	ns
qspi_miso, hold time	t_h		2.5	—	—	ns
qspi_mosi, clock to output valid	t_{od}		-2	—	2	ns
Output Load	C_L		5	—	10	pF

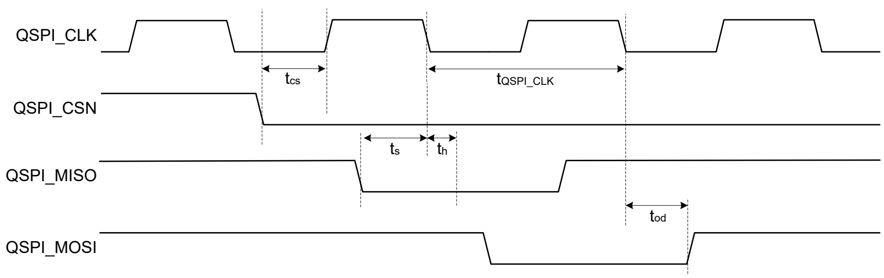


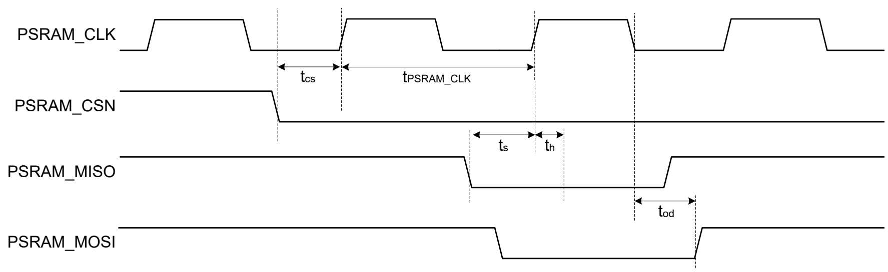
Figure 7.11. Interface Timing Diagram for QSPI High Speed Mode (Falling Edge Sampling)

7.4.7 PSRAM

7.4.7.1 Full Speed Mode (Rising Edge Sampling)

Table 7.22. PSRAM Full Speed Mode (Rising Edge Sampling)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
psram_clk	f_{psram}		0	—	40	MHz
psram_cs, to clock edge(this is achieved functionally)	t_{cs}		8.6	—	—	ns
psram_miso, setup time	t_s		4	—	—	ns
psram_miso, hold time	t_h		2.5	—	—	ns
psram_mosi, clock to output valid	t_{od}		-2	—	2	ns
Output Load	C_L		5	—	10	pF



Interface Timing Diagram for PSRAM Full Speed Mode (Rise Edge Sampling)

7.4.7.2 High Speed Mode (Falling Edge Sampling)

Table 7.23. PSRAM High Speed Mode (Falling Edge Sampling)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
psram_clk	f_{psram}		40	—	80	MHz
psram_cs, to clock edge(this is achieved functionally)	t_{cs}		4.3	—	—	ns
psram_miso, setup time	t_s		4	—	—	ns
psram_miso, hold time	t_h		2.5	—	—	ns
psram_mosi, clock to output valid	t_{od}		-2	—	2	ns
Output Load	C_L		5	—	10	pF

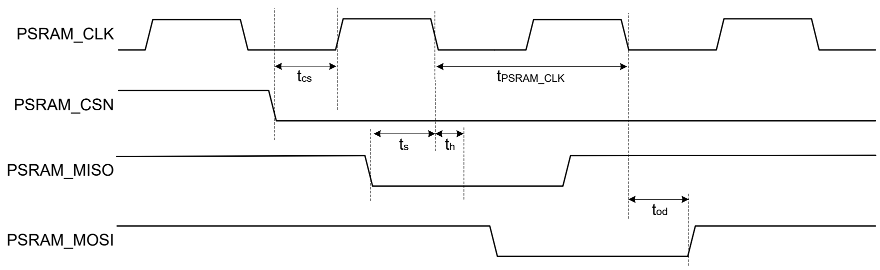


Figure 7.12. Interface Timing Diagram for PSRAM High Speed Mode (Falling Edge Sampling)

7.4.8 I2C

7.4.8.1 Standard Mode

Table 7.24. I2C Standard Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL	f_{i2c}		0	—	100	kHz
clock low period	t_{low}		4.7	—	—	µs
clock high period	t_{high}		4.0	—	—	µs
start condition, setup time	t_{sstart}		4.7	—	—	µs
start condition, hold time	t_{hstart}		4.0	—	—	µs
data, setup time	t_s		250	—	—	ns
stop condition, setup time	t_{sstop}		4.0	—	—	µs
Output Load	C_L		5	—	10	pF

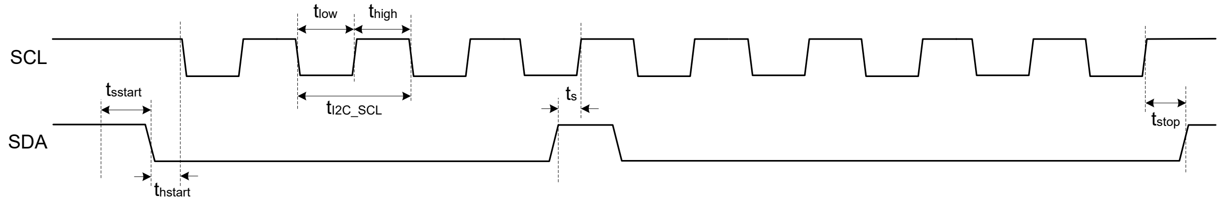


Figure 7.13. Interface Timing Diagram for I2C Standard Mode

7.4.8.2 Fast Speed Mode

Table 7.25. I2C Fast Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL	f_{i2c}		100	—	400	kHz
clock low period	t_{low}		1.3	—	—	µs
clock high period	t_{high}		0.6	—	—	µs
start condition, setup time	t_{sstart}		0.6	—	—	µs
start condition, hold time	t_{hstart}		0.6	—	—	µs
data, setup time	t_s		100	—	—	ns
stop condition, setup time	t_{sstop}		0.6	—	—	µs
Output Load	C_L		5	—	10	pF

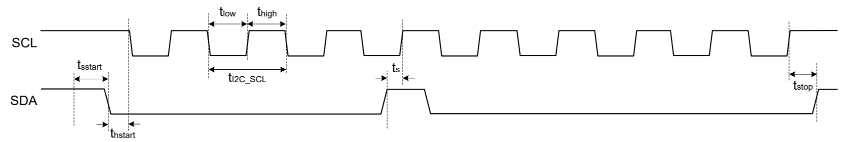


Figure 7.14. Interface Timing Diagram for I2C Fast Speed Mode

7.4.8.3 Fast Mode Plus

Table 7.26. I2C Fast Mode Plus

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL	f_{i2c}		400	—	1000	kHz
clock low period	t_{low}		0.5	—	—	µs
clock high period	t_{high}		0.26	—	—	µs
start condition, setup time	t_{sstart}		0.26	—	—	µs
start condition, hold time	t_{hstart}		0.26	—	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
data, setup time	t_s		50	—	—	ns
stop condition, setup time	t_{sstop}		0.26	—	—	µs
Output Load	C_L		5	—	10	pF

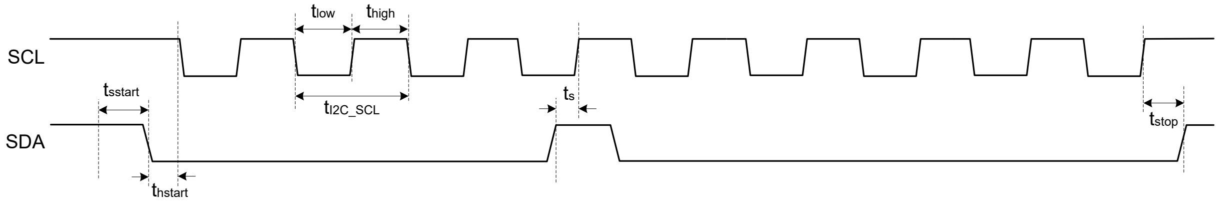


Figure 7.15. Interface Timing Diagram for I2C Fast Speed Mode

7.4.8.4 High Speed Mode

Table 7.27. I2C High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL	f_{i2c}		1	—	3.4	MHz
clock low period	t_{low}		160	—	—	ns
clock high period	t_{high}		60	—	—	ns
start condition, setup time	t_{sstart}		160	—	—	ns
start condition, hold time	t_{hstart}		160	—	—	ns
data, setup time	t_s		10	—	—	ns
data, hold time	t_h		0	—	70	ns
stop condition, setup time	t_{sstop}		160	—	—	ns
Output Load	C_L		5	—	10	pF

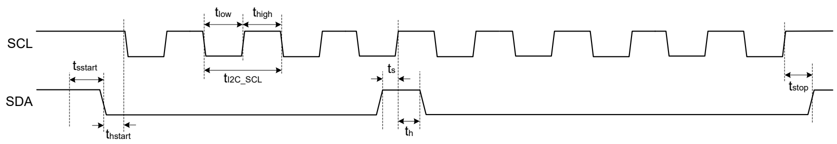


Figure 7.16. Interface Timing Diagram for I2C High Speed Mode

7.4.9 I2S/PCM Primary and Secondary

7.4.9.1 Primary Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Table 7.28. I2S/PCM Primary Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
i2s_clk	f_{i2s}		0	—	25	MHz
i2s_din,i2s_ws setup time	t_s		10	—	—	ns
i2s_din,i2s_ws hold time	t_h		3	—	—	ns
i2s_dout output delay	t_{od}		0	—	15	ns
i2s_dout output load	C_L		5	—	10	pF

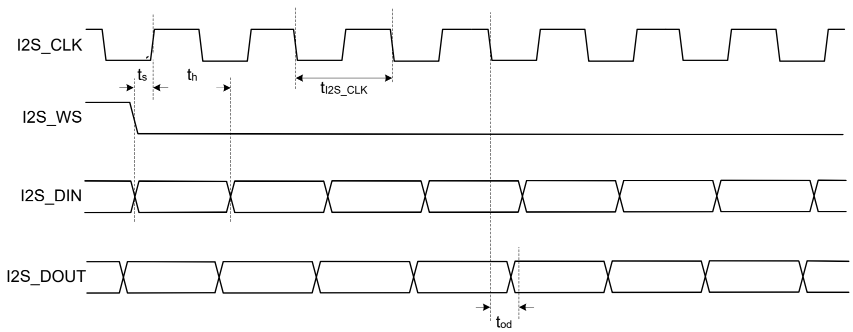


Figure 7.17. Interface Timing Diagram for I2S Primary Mode

7.4.9.2 Secondary Mode

Negedge driving and posedge sampling for I2S

Posedge driving and negedge sampling for PCM

Table 7.29. I2S/PCM Secondary Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
i2s_clk	f_{i2s}		0	—	25	MHz
i2s_din,i2s_ws setup time	t_s		7.5	—	—	ns
i2s_din,i2s_ws hold time	t_h		2	—	—	ns
i2s_dout output delay	t_{od}		0	—	17	ns
i2s_dout output load	C_L		5	—	10	pF

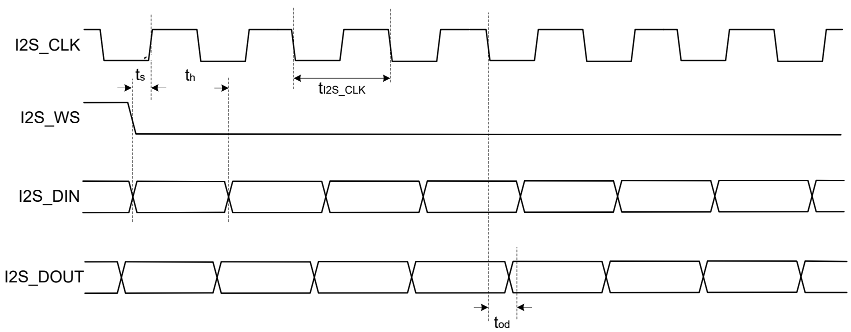


Figure 7.18. Interface Timing Diagram for I2S Secondary Mode

7.4.10 ULP I2S/PCM Primary and Secondary

7.4.10.1 Primary Mode

Negedge driving and posedge sampling for I2S
posedge driving and negedge sampling for PCM

Table 7.30. ULP I2S/PCM Primary Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
i2s_clk	f_{i2s}		0	—	10	MHz
i2s_din,i2s_ws setup time w.r.t negedge	t_s		15	—	—	ns
i2s_din,i2s_ws hold time w.r.t negedge	t_h		0	—	—	ns
i2s_dout output delay	t_{od}		0	—	20	ns
i2s_dout output load	C_L		5	—	10	pF

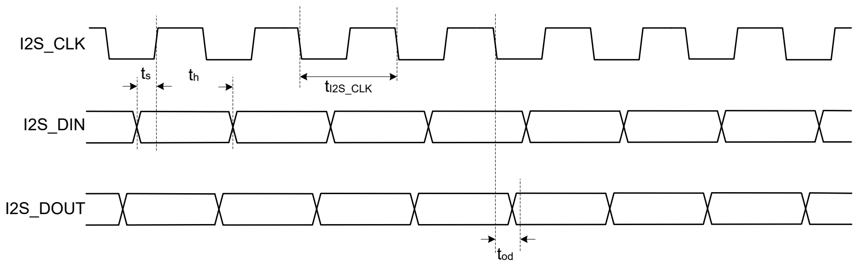


Figure 7.19. Interface timing Diagram for ULP I2S/PCM Primary

7.4.10.2 Secondary Mode

Negedge driving and posedge sampling for I2S
Posedge driving and negedge sampling for PCM

Table 7.31. ULP I2S/PCM Secondary Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
i2s_clk	f_{i2s}		0	—	10	MHz
i2s_din,i2s_ws setup time w.r.t negedge	t_s		10	—	—	ns
i2s_din,i2s_ws hold time w.r.t negedge	t_h		3	—	—	ns
i2s_dout output delay	t_{od}		0	—	20	ns
i2s_dout output load	C_L		5	—	10	pF

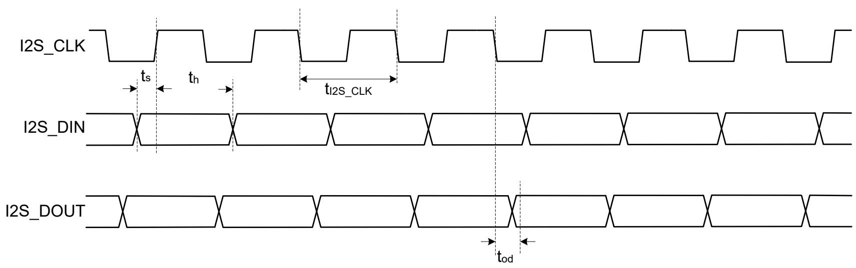


Figure 7.20. Interface Timing Diagram for ULPI2S Secondary

7.4.11 SSI Primary/Secondary

7.4.11.1 Primary Full Speed Mode

Negedge driving and posedge sampling

Table 7.32. SSI Primary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SSI_CLK	f_{ssi}		0	—	20	MHz
SSI_MISO, input setup time	t_s		17	—	—	ns
SSI_MISO, input hold time	t_h		2	—	—	ns
SSI_MOSI, clock to output valid	t_{od}		0	—	16	ns
Output Load	C_L		5	—	10	pF

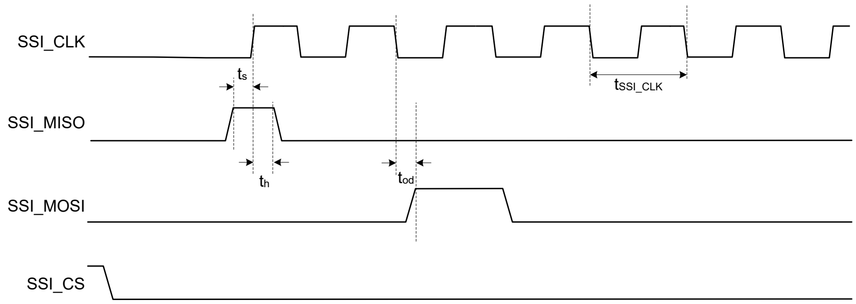


Figure 7.21. Interface Timing Diagram for SSI Primary Full Speed Mode

7.4.11.2 Primary High Speed Mode

Posedge driving and posedge sampling.

Table 7.33. SSI Primary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SSI_CLK	f_{ssi}		20	—	40	MHz
SSI_MISO, input setup time	t_s		17	—	—	ns
SSI_MISO, input hold time	t_h		2	—	—	ns
SSI_MOSI, clock to output valid	t_{od}		1	—	16	ns
Output Load	C_L		5	—	10	pF

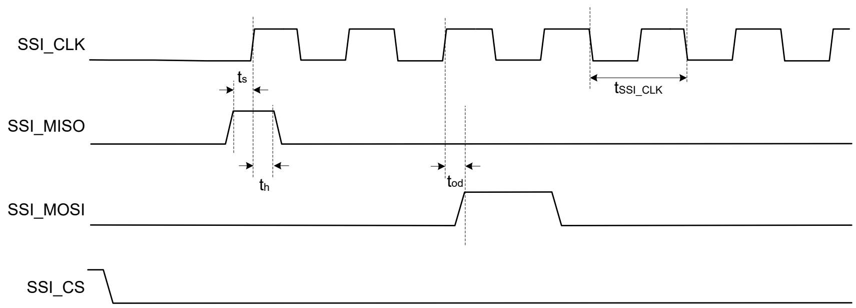


Figure 7.22. Interface Timing Diagram for SSI Primary High Speed Mode

7.4.11.3 Secondary Full Speed Mode

Negedge driving and posedge sampling

Table 7.34. SSI Secondary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SSI_CLK	f_{ssi}		0	—	20	MHz
SSI_MOSI, SSI_CS, input setup time	t_s		5	—	—	ns
SSI_MOSI, input hold time	t_h		0	—	—	ns
SSI_MISO, clock to output delay	t_{od}		—	—	24	ns
Output Load	C_L		5	—	10	pF

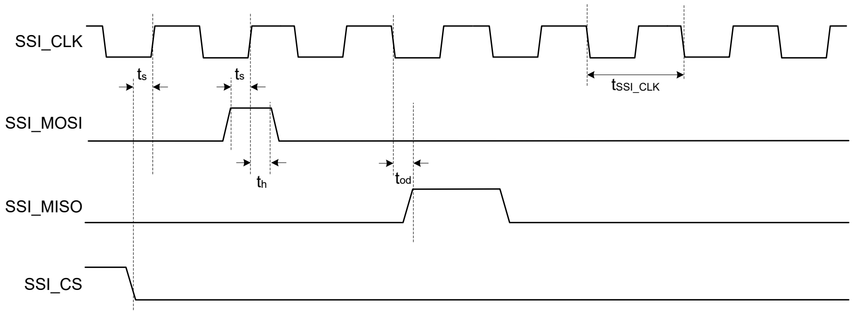


Figure 7.23. Interface Timing Diagram for SSI Secondary Full Speed Mode

7.4.12 ULP SSI Primary

7.4.12.1 Primary Full Speed Mode

Negedge driving and posedge sampling

Table 7.35. ULP SSI Primary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SSI_CLK	f_{ssi}		0	—	10	MHz
SSI_MISO, input setup time	t_s		20	—	—	ns
SSI_MISO, input hold time	t_h		0	—	—	ns
SSI_CS, SSI_MOSI, clock to output valid	t_{od}		0	—	25	ns
Output Load	C_L		5	—	10	pF

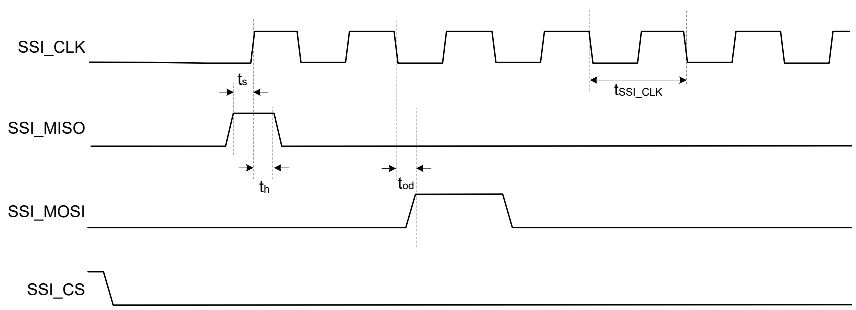


Figure 7.24. Interface Timing Diagram for ULP SSI -- Full Speed Mode

7.4.13 GSPI Primary

7.4.13.1 Full Speed Mode

Negedge driving and posedge sampling.

Table 7.36. GSPI Primary Full Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
gspi_clk	f_{gspi}		0	—	58	MHz
gspi_csn, to clock edge(this is achieved functionally)	t_{cs}		4.16	—	—	ns
gspi_miso, setup time	t_s		2	—	—	ns
gspi_miso, hold time	t_h		2	—	—	ns
gspi_csn, gspi_mosi, clock to output valid	t_{od}		0	—	8	ns
Output Load	C_L		5	—	10	pF

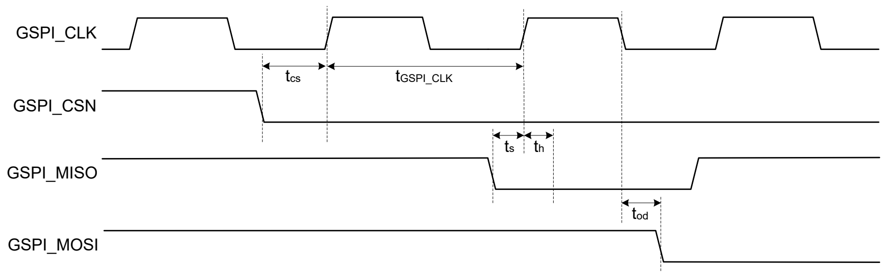


Figure 7.25. Interface Timing Diagram for GSPI Primary Full Speed Mode

7.4.13.2 High Speed Mode

Negedge driving and negedge sampling.

Table 7.37. GSPI Primary High Speed Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
gspi_clk	f_{gspi}		58	—	116	MHz
gspi_csn, to clock edge(this is achieved functionally)	t_{cs}		4.16	—	—	ns
gspi_miso, setup time	t_s		2	—	—	ns
gspi_miso, hold time	t_h		2	—	—	ns
gspi_csn, gspi_mosi, clock to output valid	t_{od}		0	—	8	ns
Output Load	C_L		5	—	10	pF

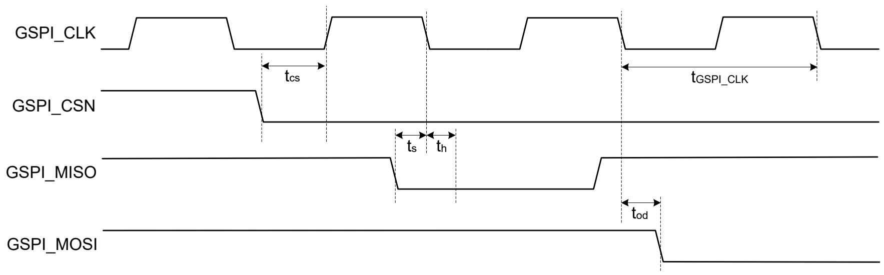


Figure 7.26. Interface Timing Diagram for GSPI Primary High Speed Mode

7.4.14 Cortex-M4 JTAG

Table 7.38. Cortex-M4F JTAG

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TCK period	f_{tck}		—	—	20	MHz
Setup	t_s		5	—	—	ns
Hold	t_h		4	—	—	ns
Output Delay	t_{od}		0	—	38.5	ns
Output Load	C_L		5	—	10	pF

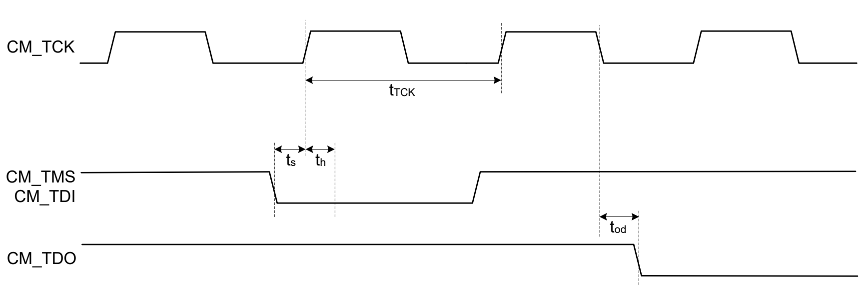


Figure 7.27. Interface Timing Diagram for Cortex-M4 JTAG

7.4.15 Cortex-M4 Trace

Table 7.39. Cortex-M4F Trace

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TRACECLK Period	f_{trace}		0	—	100	MHz
Output Delay	t_{od}		1.2	—	8	ns
Output Load	C_L		5	—	10	pF

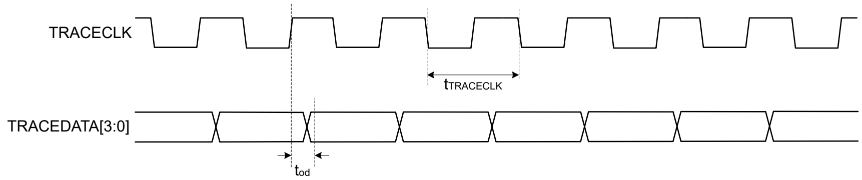


Figure 7.28. Interface Timing Diagram for Cortex-M4 Trace

7.4.16 Power State Wake Timing

Table 7.40. Power State Wake Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transition time from PS4 standby to PS4 active	t_{PS4SB_TR}		—	0.8	—	µs
Transition time from PS3 standby to PS3 active	t_{PS3SB_TR}		—	1.0	—	µs
Transition time from PS2 standby to PS2 active	t_{PS2SB_TR}		—	2.7	—	µs
Wake up time from PS4 sleep to PS4 active	t_{PS4SLP_WU}	320 KB RAM retained in sleep	—	1.1	—	ms
Wake up time from PS3 sleep to PS3 active	t_{PS3SLP_WU}	320 KB RAM retained in sleep	—	1.05	—	ms
Wake up time from PS2 sleep to PS3 active	t_{PS2SLP_WU}	320 KB RAM retained in sleep	—	15.8	—	µs
Transition time from PS1 to PS2 active	t_{PS1_tr}		—	5.1	—	ms
Wake up time from PS0 to PS4 active	t_{PS0_WU}	RC oscillator configured to 20 MHz	—	12.3	—	ms

7.5 Analog Peripherals

The following analog peripherals are available:

- 2x Analog Comparators
- 3x General purpose Op-Amp
- 16 channel, 12 bit, 5 Msps Analog to Digital Converter with both single ended and differential modes
- 10 bit, 5 MSPS Digital to Analog Converter

7.5.1 Analog Comparators

Analog comparator is a peripheral circuit that compares two analog voltage inputs and gives a logical output based on comparison.

There are 9 different inputs for each pin of comparator, and 2 of the 9 are external pin inputs.
The following cases of comparison are possible

1. Compare external pin inputs
2. Compare external pin input to internal voltages
3. Compare internal voltages

The comparator compares inputs p and n to produce an output, cmp_out.

p > n, cmp_out = 1

p < n, cmp_out = 0

Analog Peripherals consists of 2 comparators whose inputs can be programmed independently. The reference buffer and resistor bank are shared between the two comparators and can be enabled only when at least one of the comparators is enabled.

Table 7.41. Analog Comparator Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply	V_{supply}	Supply is AUX_AVDD	1.72	—	3.63	
Programmable voltage reference minimum	V_{ref_min}		—	0.1	—	V
Programmable voltage reference maximum	V_{ref_max}		—	1.1	—	V
Programmable voltage reference step size	V_{ref_step}		—	0.1	—	V
The minimum voltage difference required between inputs to make output high	V_{os_comp}		—	5	—	mV
Hysteresis	V_{hyst_comp}	Hysteresis = 2'd1	—	60	—	mV
		Hysteresis = 2'd3	—	95	—	mV
Input common-mode range	$ICMR_{comp}$		0.15	—	ULP_IO_VDD - 0.15	V
Current consumption on VBATT with all blocks enabled	I_{q_comp}		—	305	—	µA

7.5.2 Auxiliary LDO Electrical Specifications - Regulation Mode

Table 7.42. AUX LDO Electrical Specifications - Regulation Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Supply Voltage	V_{in}	AUX LDO in Regulation Mode	2.97	3.3	3.63	V
Max programmable output voltage at AUX_AVDD	V_{outmax}		—	2.8	—	V
Min programmable output voltage at AUX_AVDD	V_{outmin}		—	1.6	—	V
Output voltage programmable step size[1]	V_{step}		—	80	—	mV
Load current capability	I_{load}		—	—	10	mA
Quiescent current	I_q		—	80	—	µA

Note:

1. Programmable output voltage step, Vstep, can vary up to ± 5%.

7.5.3 AUX LDO Electrical Specifications - Bypass Mode

Table 7.43. AUX LDO Electrical Specifications - Bypass Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Supply Voltage	V_{in}	AUX LDO in Bypass Mode	1.71	1.8	1.98	V
ON Resistance between V_{in} to V_{out} pins of AUX LDO	R_{on}		—	6.3	—	Ω
Voltage drop from V_{in} to V_{out}	V_{drop}	Load = 10 mA (Max)	—	100	—	mV
Output voltage at AUX_AVDD [1]	V_{out}	Load = 10 mA at Vin = 1.71 V [2]	—	1.63	—	V

Note:

1. $V_{out} = V_{in} - R_{on} * I_{load}$
2. Maximum load current is possible when the three op-amps, two analog comparators, ADC, and DAC are all enabled.

7.5.4 Analog to Digital Converter

- 12 bit precision ADC
- Single ended mode and differential mode configuration
- Two clock latency
- ADC performance not guaranteed below -20 °C.

Table 7.44. ADC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution of ADC	N		—	12	—	bits
Number of channels	$N_{channel}$	Single ended Mode	—	18	—	channel
		Differential Mode	—	9	—	channel
ADC sampling and input clock frequency	f_{ADC}		—	—	2.5	MHz
Input voltage range	V_{AIN}	Single ended Mode, Positive terminal	0	—	AUX_AVDD	V
		Differential Mode, Positive and negative terminals	0	—	AUX_AVDD / 2	V
Input resistance	R_{in}	Single Channel input conversion	—	100	—	kΩ
ADC internal sample and hold capacitor	$C_{sampled}$		—	3	—	pF
Fixed capacitance from multiplexers and ESD protection	C_{fixed}		—	2	—	pF
Sampling time	t_s		0.1	—	—	uS
Gain Error	G_{err}		—	2	—	%
Offset Error	$Offset_{err}$		—	10	—	mV
Effective number of bits	ENOB	Input frequency 100 kHz at 2.5 Msps	—	9.45	—	bits
Signal to noise and distortion ratio	SNDR	Input frequency 100 kHz at 2.5 Msps	—	59	—	dB
Active current consumption	I_{active}	Input frequency 100 kHz at 2.5 Msps	—	1.55	—	mA

7.5.5 Digital to Analog Converter

- 10 bit precision DAC
- Single-ended voltage outputs
- 1.71 to 3.63 V supply operation
- DAC performance not guaranteed below -20 °C

Table 7.45. DAC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Lowest output voltage	VOL		—	0.15 * AUX_AVDD	—	V
Highest output voltage	VOH		—	0.85 * AUX_AVDD	—	V
Resistive load	R_{load}	Connect to ground	5	—	—	kΩ
Load capacitance	C_{load}		—	—	50	pF
Signal to noise and distortion ratio	SNDR	40 kHz sine wave output and sampling frequency of 2 MHz	—	50	—	dB
Effective number of bits	ENOB	40 kHz sine wave output and sampling frequency of 2 MHz	—	8	—	bits

7.5.6 Op-Amp

There are 3 general purpose Operational Amplifiers (Op-Amps) offering rail-to-rail inputs and outputs.
The Op-Amps can be configured as:

1. Unity gain amplifier
2. Trans-Impedance Amplifier (TIA)
3. Non-inverting Programmable Gain Amplifier (PGA)
4. Inverting Programmable Gain Amplifier (PGA)
5. Non-inverting Programmable hysteresis comparator
6. Inverting Programmable hysteresis comparator
7. Cascaded Non-Inverting PGA
8. Cascaded Inverting PGA
9. Two Op-Amps Differential Amplifier
10. Instrumentation Amplifier

Note:

- In the above list, #7, #8, #9 are configured by cascading 2 Op-Amps
- In the above list, #10 is configured by cascading 3 Op-Amps

Table 7.46. Opamp Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage range	V_{in}		0	—	AUX_AVDD	V
output voltage range	V_{out}	source or sink 1 mA	0.1	—	AUX_AVDD - 0.1	V
output current capability, source or sink	I_{out}	0.5 < V_{out} < AUX_AVDD-0.5	—	—	3	mA
Input offset voltage (1 sigma)	V_{os}	Power mode = high, C_L = 50 pF	—	2.2	—	mV
		Power mode = low, C_L = 50 pF	—	2.2	—	mV
Gain error, unity gain buffer mode, R_L = 1 kΩ	Ge1	Power mode = high, C_L = 50 pF	—	1	—	%
		Power mode = low, C_L = 50 pF	—	1	—	%
Phase margin, in UGB mode	PM	Power mode = high, C_L = 50 pF	—	59	—	°C
		Power mode = low, C_L = 50 pF	—	63	—	°C
Gain-bandwidth product	GBW	Power mode = high, C_L = 50 pF	—	17	—	MHz
		Power mode = low, C_L = 50 pF	—	7.5	—	MHz
Total Harmonic Distortion, at 100 kHz (UGB mode)	THD_{UGB}	Power mode = high, C_L = 50 pF	—	-64	—	dB
		Power mode = low, C_L = 50 pF	—	-62	—	dB
Total Harmonic Distortion, at 10 kHz (Non inv amp mode, gain = 51)	THD	Power mode = high, C_L = 50 pF	—	-58	—	dB
		Power mode = low, C_L = 50 pF	—	-56	—	dB
DC Power supply rejection ratio	PSRR	Power mode = high, C_L = 50 pF	—	90	—	dB
		Power mode = low, C_L = 50 pF	—	90	—	dB
DC Common mode rejection ratio	CMRR	Power mode = high, C_L = 50 pF	—	70	—	dB
		Power mode = low, C_L = 50 pF	—	71	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Quiescent current - 1 Op-Amp	I_{dd}	Power mode = high, C_L = 50 pF	—	0.95	—	mA
		Power mode = low, C_L = 50 pF	—	315	—	µA

7.5.7 Temperature Sensor

- Generates PTAT Voltage from BJT based band gap.
- Buffered PTAT voltage is given at ADC Input.
- Output of the ADC is linear function of temperature.

The BJT based sensor works over the full operating temperature and supply range of the device. It outputs a digital word having a resolution of nearly 1 ºC. The conversion time is 2 clock cycles of ADC after turning ON the temperature sensor. Typically, the block consumes 110 uA of current and leakage current is 800 pA.

Table 7.47. BJT Based Temperature Sensor Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Accuracy	T_{acc}		—	6	—	°C

7.6 RF Characteristics

In the sub-sections below,

- All numbers are measured at T_A = 25 °C, VBATT = 3.3 V
- Please refer to 8. Reference Schematics, BOM, and Layout Guidelines. The integrated RF front end includes the matching network, internal RF switch, and a band-pass filter.
- Supported WLAN channels for different regions include:
  - US: Channels 1 (2412 MHz) through 11 (2462 MHz)
  - Europe: Channels 1 (2412 MHz) through 13 (2472 MHz)
  - Japan: Channels 1 (2412 MHz) through 14 (2484 MHz), Channel 14 supports 1 and 2 Mbps data rates only

7.6.1 WLAN 2.4 GHz Transmitter Characteristics

7.6.1.1 Transmitter Characteristics with 3.3 V Supply

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VBATT = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at RF pin.

Table 7.48. WLAN 2.4 GHz Transmitter Characteristics with 3.3 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power for 20 MHz Bandwidth, with EVM limits [1, 2, 5]	POUT	802.11b 1 Mbps DSSS, EVM< -9 dB	—	17	—	dBm
		802.11b 11 Mbps CCK, EVM< -9 dB	—	17	—	dBm
		802.11g 6 Mbps OFDM, EVM< -5 dB [3]	—	17	—	dBm
		802.11g 54 Mbps OFDM, EVM< -25 dB [3]	—	13.5	—	dBm
		802.11n HT20 MCS0 Mixed Mode, EVM< -5 dB[3]	—	17.5	—	dBm
		802.11n HT20 MCS7 Mixed Mode, EVM< -27 dB[3]	—	12.5	—	dBm
		802.11ax HE20 MCS0 SU, EVM< -5 dB[3, 4]	—	15.5	—	dBm
		802.11ax HE20 MCS7 SU, EVM< -27 dB[3, 4]	—	11	—	dBm
Power variation across channels	$POUT_{VAR\_CH}$		—	2	—	dB
Power variation across temperature	$POUT_{VAR\_T}$	-40 to +85 °C	—	3	—	dB

Note:
1. Transmit power listed in this table is average power across all channels.
2. TX power in edge channels will be limited by Restricted band edge in the FCC region.
3. 11g/n/ax TX power in edge channels will be limited by Unwanted Emissions in MIC region.
4. 11ax TX power will be limited by PSD in the ETSI region.
5. Channels 1 (2412 MHz) through 11 (2462 MHz) are supported for North America (FCC, ISED). Channels 1 (2412 MHz) through 13 (2472 MHz) are supported for Europe and Japan (CE, MIC). Channel 14 (2484 MHz) is additionally supported for Japan.

7.6.2 WLAN 2.4 GHz Receiver Characteristics on High-Performance (HP) Mode

Unless otherwise indicated, typical conditions are: T_A = 25 °C. VBATT = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at RF pin.

Table 7.49. WLAN 2.4 GHz Receiver Characteristics on HP Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity for 20 MHz Bandwidth [1, 2]	SENS	802.11b 1 Mbps DSSS [4]	—	-95.5	—	dBm
		802.11b 11 Mbps CCK [4]	—	-87	—	dBm
		802.11g 6 Mbps OFDM [5]	—	-91.5	—	dBm
		802.11g 54 Mbps OFDM [5]	—	-75	—	dBm
		802.11n HT20 MCS0 Mixed Mode [6]	—	-90.5	—	dBm
		802.11n HT20 MCS7 Mixed Mode [6]	—	-70.5	—	dBm
		802.11ax HE20 MCS0 SU [7]	—	-90	—	dBm
		802.11ax HE20 MCS7 SU [7]	—	-70	—	dBm
		802.11ax HE20 MCS0 ER [7]	—	-91.5	—	dBm
Maximum Input Level for PER below 10 %	RX_{SAT}	802.11b	—	3	—	dBm
		802.11g	—	-2.5	—	dBm
		802.11n	—	-4.5	—	dBm
		802.11ax	—	-2.5	—	dBm
RSSI Accuracy Range	$RSSI_{RNG}$		—	+/-4	—	dB
Adjacent Channel Interference [8]	ACI	802.11b 1 Mbps DSSS [4] [9]	—	48	—	dB
		802.11b 11 Mbps CCK [4] [9]	—	36	—	dB
		802.11g 6 Mbps OFDM [5] [10]	—	41	—	dB
		802.11g 54 Mbps OFDM [5] [10]	—	23	—	dB
		802.11n HT20 MCS0 Mixed Mode [6] [10]	—	33	—	dB
		802.11n HT20 MCS7 Mixed Mode [6] [10]	—	11	—	dB
		802.11ax HE20 MCS0 SU [7] [10]	—	20	—	dB
		802.11ax HE20 MCS7 SU [7] [10]	—	6	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Alternate Adjacent Channel Interference [8]	AACI	802.11b 1 Mbps DSSS [4] [9]	—	50	—	dB
		802.11b 11 Mbps CCK [4] [9]	—	39	—	dB
		802.11g 6 Mbps OFDM [5] [10]	—	51	—	dB
		802.11g 54 Mbps OFDM [5] [10]	—	31	—	dB
		802.11n HT20 MCS0 Mixed Mode [6] [10]	—	51	—	dB
		802.11n HT20 MCS7 Mixed Mode [6] [10]	—	29	—	dB
		802.11ax HE20 MCS0 SU [7] [10]	—	50	—	dB
		802.11ax HE20 MCS7 SU [7] [10]	—	30	—	dB

Note:

1. RX Sensitivity Variation is up to 2 dB for channels (1, 2, 3, 4, 5, 9, and 10) at typical / room temperature.
2. RX Sensitivity may be degraded up to 3 dB for channels (6, 7, 8, 11, 12, 13 and 14) at typical / room temperature.
3. Sensitivity variation across temperature -40 °C to +85 °C is up to 3 dB
4. 802.11b, Packet size is 1024 bytes, < 8 % PER limit, Carrier modulation is non-DCM
5. 802.11g, Packet size is 1024 bytes, < 10 % PER limit, Carrier modulation is non-DCM
6. 802.11n, Packet size is 4096 bytes, < 10 % PER limit, Carrier modulation is non-DCM
7. 802.11ax, Packet size is 4096 bytes, < 10 % PER limit, Carrier modulation is non-DCM
8. ACI / AACI is calculated as Interferer Power (dBm) - Inband power (dBm)
9. Desired signal power is 6 dB above standard defined sensitivity level
10. Desired signal power is 3 dB above standard defined sensitivity level

7.6.3 WLAN 2.4 GHz Receiver Characteristics on Low-Power (LP) Mode

Unless otherwise indicated, typical conditions are: T_A = 25 °C. VBATT = 3.3 V. Remaining supplies are at typical operating conditions. Parameters are referred at RF pin.

Table 7.50. WLAN 2.4 GHz Receiver Characteristics on LP Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sensitivity for 20 MHz Bandwidth [1, 2]	SENS	802.11b 1 Mbps DSSS [4]	—	-95.5	—	dBm
		802.11b 11 Mbps CCK [4]	—	-87	—	dBm
		802.11g 6 Mbps OFDM [5]	—	-91	—	dBm
		802.11g 36 Mbps OFDM [5]	—	-80.5	—	dBm
		802.11n HT20 MCS0 Mixed Mode [6]	—	-90	—	dBm
		802.11n HT20 MCS4 Mixed Mode [6]	—	-78	—	dBm
Maximum Input Level for PER below 10%	RX_{SAT}	802.11b	—	-8	—	dBm
		802.11g	—	-0.5	—	dBm
		802.11n	—	-1	—	dBm
RSSI Accuracy Range	$RSSI_{RNG}$		—	+/-4	—	dB
Adjacent Channel Interference [7]	ACI	802.11b 1 Mbps DSSS [4, 8]	—	46	—	dB
		802.11b 11 Mbps CCK [4, 8]	—	33	—	dB
		802.11g 6 Mbps OFDM [5, 9]	—	42	—	dB
		802.11g 36 Mbps OFDM [5, 9]	—	26	—	dB
		802.11n HT20 MCS0 Mixed Mode [6, 9]	—	33	—	dB
		802.11n HT20 MCS4 Mixed Mode [6, 9]	—	20	—	dB
Alternate Adjacent Channel Interference [7]	AACI	802.11b 1 Mbps DSSS [4, 8]	—	49	—	dB
		802.11b 11 Mbps CCK [4, 8]	—	37	—	dB
		802.11g 6 Mbps OFDM [5, 9]	—	50	—	dB
		802.11g 36 Mbps OFDM [5, 9]	—	35	—	dB
		802.11n HT20 MCS0 Mixed Mode [6, 9]	—	50	—	dB
		802.11n HT20 MCS4 Mixed Mode [6, 9]	—	33	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. RX Sensitivity Variation is up to 2 dB for channels (1, 2, 3, 4, 5, 9, and 10) at typical / room temperature 2. RX Sensitivity may be degraded up to 3 dB for channels (6, 7, 8, 11, 12, 13, 14) at typical / room temperature 3. Sensitivity variation across temperature -40 °C to +85 °C is up to 3 dB 4. 802.11b, Packet size is 1024 bytes, < 8 % PER limit, Carrier modulation is non-DCM 5. 802.11g, Packet size is 1024 bytes, < 10 % PER limit, Carrier modulation is non-DCM 6. 802.11n, Packet size is 4096 bytes, < 10 % PER limit, Carrier modulation is non-DCM 7. ACI / AACI is calculated as Interferer Power (dBm) - Inband power (dBm) 8. Desired signal power is 6 dB above standard defined sensitivity level 9. Desired signal power is 3 dB above standard defined sensitivity level						

7.6.4 Bluetooth Transmitter Characteristics on High-Performance (HP) Mode

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VBATT = 3.3 V, and remaining supplies are at typical operating conditions. Parameters are referred at RF pin.

Table 7.51. Bluetooth Transmitter Characteristics on HP Mode 3.3 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power [1]	POUT	LE 1 Mbps	—	17	—	dBm
		LE 2 Mbps	—	17	—	dBm
		LR 500 kbps[2]	—	17	—	dBm
		LR 125 kbps [2]	—	17	—	dBm
Power variation across channels	$POUT_{VAR\_CH}$		—	2	—	dB
Power variation across temperature	$POUT_{VAR\_T}$	-40 to +85 °C	—	3	—	dB
Adjacent Channel Power |M-N| = 2	ACP_{eq2}	LE	—	-34	—	dBm
Adjacent Channel Power |M-N| > 2	ACP_{gt2}	LE	—	-38	—	dBm
BLE Modulation Characteristics at 1 Mbps	MOD_{CHAR}	Δf1 Avg	—	248	—	kHz
		Δf2 Max	—	250	—	kHz
		Δf2 Avg/Δf1 Avg	—	1.5	—	
Note: 1. ETSI Max Power is limited to 10 dBm/MHz EIRP to meet PSD requirements, because device falls under DTS. 2. In FCC, LR 125 kbps, 500 kbps Max Power is limited to 11 dBm to meet PSD requirement, because device falls under DTS. 3. In MIC Max power is limited to 7 dBm to meet 10 dBm/MHz limit.						

7.6.5 Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Mode

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VBATT = 3.3 V, and remaining supplies are at typical operating conditions. Parameters are referred at RF pin.

Table 7.52. Bluetooth Transmitter Characteristics on Low-Power (LP) 0 dBm RF Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Transmit Power	POUT	LE 1 Mbps	—	-1	—	dBm
		LE 2 Mbps	—	-1	—	dBm
		LR 500 kbps	—	-1	—	dBm
		LR 125 kbps	—	-1	—	dBm
Power variation across channels	$POUT_{VAR\_CH}$		—	2	—	dB
Power variation across temperature	$POUT_{VAR\_T}$	-40 °C to +85 °C	—	2	—	dB
Adjacent Channel Power |M-N| = 2	ACP_{eq2}	LE	—	-44	—	dBm
Adjacent Channel Power |M-N| > 2	ACP_{gt2}	LE	—	-48	—	dBm
BLE Modulation Characteristics at 1 Mbps	MOD_{CHAR}	Δf1 Avg	—	248	—	kHz
		Δf2 Max	—	250	—	kHz
		Δf2 Avg/Δf1 Avg	—	1.4	—	kHz

7.6.6 Bluetooth Receiver Characteristics for 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VBATT = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, and parameters are referred at RF pin. Unless otherwise indicated, specifications apply to both HP and LP modes.

Table 7.53. Bluetooth Receiver Characteristics for 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017 %, HP Mode	—	2	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017 %, LP Mode	—	-2	—	dBm
Sensitivity [1 2]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1 %	—	-94	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017 %	—	-91.5	—	dBm
Signal to co-channel interferer [3]	C/I_{CC}	(see notes)[4 5]	—	-10	—	dB
N ± 1 Adjacent channel selectivity [3]	C/I_1	Interferer is reference signal at +1 MHz offset[4 5 6 7]	—	-1	—	dB
		Interferer is reference signal at -1 MHz offset[4 5 6 7]	—	-4	—	dB
N ± 2 Alternate channel selectivity [3]	C/I_2	Interferer is reference signal at +2 MHz offset[4 5 6 7]	—	22	—	dB
		Interferer is reference signal at -2 MHz offset[4 5 6 7]	—	26	—	dB
N ± 3 Alternate channel selectivity [3]	C/I_3	Interferer is reference signal at +3 MHz offset[4 5 6 7]	—	28	—	dB
		Interferer is reference signal at -3 MHz offset[4 5 6 7]	—	40	—	dB
N ≥ | ± 4| Alternate channel selectivity[4]	C/I_4	Interferer is reference signal at ≥ | ± 4| MHz offset [4 5 6 7]	—	33	—	dB
Selectivity to image frequency [3]	C/I_{IM}	Interferer is reference signal at image frequency[4 5 7 8]	—	25	—	dB
Selectivity to image frequency ± 1 MHz [3]	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz[4 5 7 8]	—	33	—	dB
		Interferer is reference signal at image frequency -1 MHz[4 5 7 8]	—	28	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. Sensitivities for channels 19, 39 are up to 2 dB lower performance 2. Sensitivity variation across temperature -40 to +85 °C is up to 4 dB 3. C/I is calculated as Interferer Power (dBm) - Inband power (dBm) 4. 0.1 % BER, 37 byte packet size 5. Desired signal = -67 dBm 6. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz 7. With allowed exceptions 8. Image frequency is at +4 MHz offset						

7.6.7 Bluetooth Receiver Characteristics for 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VBATT = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, and parameters are referred at RF pin. Unless otherwise indicated, specifications apply to both HP and LP modes.

Table 7.54. Bluetooth Receiver Characteristics for 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017 %, HP mode	—	2	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017 %, LP mode	—	-6	—	dBm
Sensitivity [1,2]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1 %	—	-91.5	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017 %	—	-89.5	—	dBm
Signal to co-channel interferer [3]	C/I_{CC}	(see notes)[4,5]	—	-7	—	dB
N ± 1 Adjacent channel selectivity [3]	C/I_1	Interferer is reference signal at +2 MHz offset[4,6,5,7]	—	6	—	dB
		Interferer is reference signal at -2 MHz offset[4,6,5,7]	—	3	—	dB
N ± 2 Alternate channel selectivity [3]	C/I_2	Interferer is reference signal at +4 MHz offset[4,6,5,7]	—	16	—	dB
		Interferer is reference signal at -4 MHz offset[4,6,5,7]	—	21	—	dB
Selectivity to image frequency [3]	C/I_{IM}	Interferer is reference signal at image frequency[4,5,7,8]	—	16	—	dB
Selectivity to image frequency ± 2 MHz [3]	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz[4,5,7,8]	—	27	—	dB
		Interferer is reference signal at image frequency -2 MHz[4,5,7,8]	—	6	—	dB

Note:
1. Sensitivities for channels 19, 39 are up to 2 dB lower performance
2. Sensitivity variation across temperature -40 to +85 °C is up to 4 dB
3. C/I is calculated as Interferer Power (dBm) - Inband power (dBm)
4. 0.1% BER, 37 byte packet size
5. Desired signal = -67 dBm
6. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz
7. With allowed exceptions
8. Image frequency is at +4 MHz offset

7.6.8 Bluetooth Receiver Characteristics for 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VBATT = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, and parameters are referred at RF pin. Unless otherwise indicated, specifications apply to both HP and LP modes.

Table 7.55. Bluetooth Receiver Characteristics for 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017 %, HP mode	—	3	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017 %, LP mode	—	0	—	dBm
Sensitivity [1] [2]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1 %	—	-105.5	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017 %	—	-105.5	—	dBm

Note:
1. Sensitivities for channels 19, 39 are up to 5 dB lower performance
2. Sensitivity variation across temperature -40 to +85 °C is up to 4 dB

7.6.9 Bluetooth Receiver Characteristics for 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: T_A = 25 °C, VBATT = 3.3 V, remaining supplies are at typical operating conditions, packet length is 37 bytes, and parameters are referred at RF pin. Unless otherwise indicated, specifications apply to both HP and LP modes.

Table 7.56. Bluetooth Receiver Characteristics for 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max usable receiver input level	RX_{SAT}	Signal is reference signal, 255 byte payload, BER = 0.017 %, HP Mode	—	3	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017 %, LP Mode	—	0	—	dBm
Sensitivity [1] [2]	SENS	Signal is reference signal, 37 byte payload, BER = 0.1 %	—	-101.5	—	dBm
		Signal is reference signal, 255 byte payload, BER = 0.017 %	—	-99.5	—	dBm

Note:
1. Sensitivities for channels 19, 39 are up to 2 dB lower performance
2. Sensitivity variation across temperature -40 to +85 °C is up to 4 dB

7.7 Typical Current Consumption

Figure 7.29 Supply Connection for Current Measurements on page 137 shows the supply connection and measurement point for supply current numbers in this section. Note that for WLAN and BLE supply current measurements, the MCU is in deep sleep mode with no RAM retained and external 32.726 kHz oscillator connected to UULP_VBAT_GPIO_3. All measurements are taken on devices with in-package flash. The impact of external SRAM on current consumption is detailed in Table 5.13 Estimated Deepsleep/DTIMs Current with PSRAM for Different Input Supply Options on page 41.

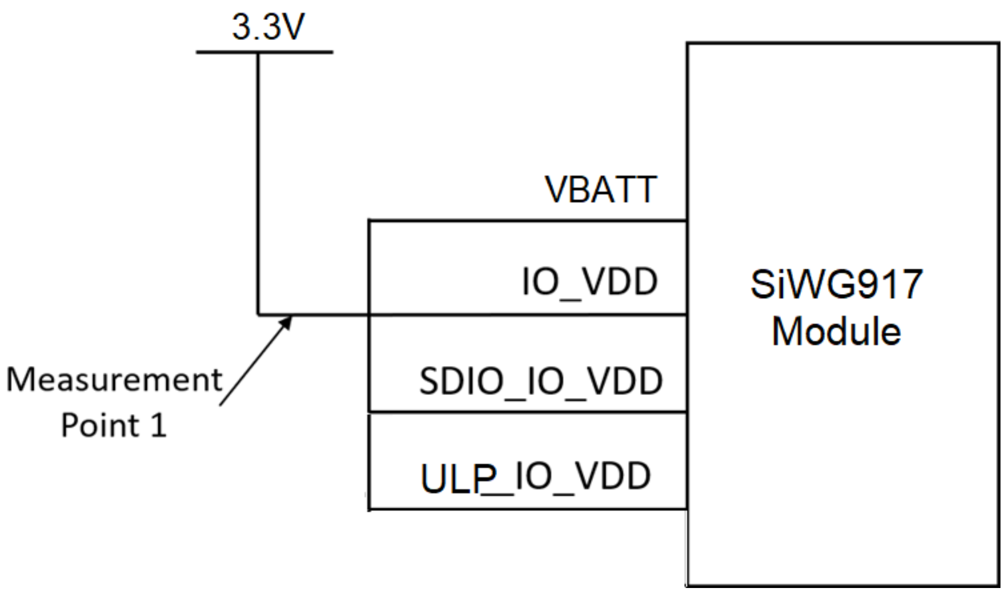


Figure 7.29. Supply Connection for Current Measurements

7.7.1 WLAN 2.4 GHz

T_A = 25 °C. VBATT = 3.3 V. Remaining supplies are at typical operating conditions. NWP clock is running at 80 MHz and Cortex-M4 is in PS0 mode.

Table 7.57. WLAN 2.4 GHz 3.3 V Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Listen current	I_{RX_LISTEN}	LP mode, 1 Mbps Listen	—	16.5	—	mA
Active Receive Current	I_{RX_ACTIVE}	1 Mbps RX Active, LP mode	—	22	—	mA
		HT20 MCS0, HP mode	—	51	—	mA
		HT20 MCS7, HP mode	—	51	—	mA
		HE20 MCS0, HP mode	—	51	—	mA
		HE20 MCS7, HP mode	—	51	—	mA
Transmit Current	I_{TX}	1 Mbps, HP mode	—	203	—	mA
		HT20 MCS0, HP mode	—	216	—	mA
		HT20 MCS7, HP mode	—	159	—	mA
		HE20 MCS0, HP mode	—	191	—	mA
		HE20 MCS7, HP mode	—	159	—	mA
Deep Sleep	I_{SLEEP}	No RAM retained	—	4.5	—	µA
		352 KB RAM retained	—	11	—	µA
Standby Associated, DTIM = 10	I_{STBY_ASSOC}	WLAN Keep Alive Every 30 s with 352 KB RAM Retained, Without TCP Keep Alive	—	71	—	µA
		WLAN Keep Alive Every 30 s with 352 KB RAM Retained, TCP Keep Alive Every 240s	—	84	—	µA
11ax TWT, Auto Config Enabled, Without TCP Keep Alive	I_{STBY_AX}	RX latency 2 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	103	—	µA
		RX latency 30 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	37	—	µA
		RX latency 60 s with 8 ms wakeup duration, WLAN Keep Alive Every 60 s with 352 KB RAM Retained	—	25	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
11ax TWT, Auto Config Enabled, With TCP Keep Alive Every 240 s	$I_{STBY\_AX\_TCP}$	RX latency 2 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	105	—	µA
		RX latency 30 s with 8 ms wakeup duration, WLAN Keep Alive Every 30 s with 352 KB RAM Retained	—	39	—	µA
		RX latency 60 s with 8 ms wakeup duration, WLAN Keep Alive Every 60 s with 352 KB RAM Retained	—	28	—	µA

Note:

1. The absolute maximum device current when transmitting at highest transmit power will not exceed 400 mA.

7.7.2 Bluetooth LE

T_A = 25 °C. VBATT = 3.3 V. Remaining supplies are at typical operating conditions. NWP clock running at 80 MHz.

Table 7.58. Bluetooth LE Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Active Current	I_{TX}	LP mode, Tx Power Index 31 (0 dBm)	—	10	—	mA
		HP mode, Tx Power Index 16 (16 dBm)	—	172	—	mA
		HP mode, Tx Power Index 4 (4 dBm)	—	79	—	mA
RX Active Current	I_{RX}	LP mode	—	11	—	mA
Advertising, Unconnectable	I_{ADV_UC}	Advertising on all 3 channels, 37 Byte payload, Interval = 1.28 s, Tx Power = 0 dBm, LP mode	—	37	—	µA
Advertising, Connectable	I_{ADV_CN}	Advertising on all 3 channels, 37 Byte payload, Interval = 1.28 s, Tx Power = 0 dBm, LP mode	—	43	—	µA
Connected	I_{CONN}	Connection Interval = 200 ms, No data, Tx Power = 0 dBm, LP mode	—	141	—	µA
		Connection Interval = 1.28 s, No data, Tx Power = 0 dBm, LP mode	—	41	—	µA

7.7.3 MCU Power State Current Consumption

T_A = 25 °C. VBATT = 3.3 V. Remaining supplies are at typical operating conditions. All numbers taken with NWP in shutdown mode.

Table 7.59. MCU Power State Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PS4 Supply Current	I_{PS4}	Sleep, 320 KB RAM retained, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	13.7	—	µA
		Active - Default configuration	—	12.7	—	mA
PS3 Supply Current	I_{PS3}	Sleep, 320 KB RAM retained, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	13.7	—	µA
		Active - Default configuration	—	7.6	—	mA
PS2 Supply Current	I_{PS2}	Sleep, 320 KB RAM retained, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	13.7	—	µA
		Active - Default configuration	—	808	—	µA
PS1 Supply Current	I_{PS1}	320 KB RAM retained, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	309	—	µA
PS0 Supply Current	I_{PS0}	Without RAM retention, SRAM PERI ON, SCDC = 1.05 V, ULP LDO = 0.75 V	—	1.44	—	µA

8. Reference Schematics, BOM, and Layout Guidelines

Note:

1. Customers should include provision for programming or updating the firmware at manufacturing.
   a. If using UART, we recommend bringing out the HSPI or SDIO lines to test points, so designers could use the faster interface for programming the firmware as needed.
   b. If using HSPI or SDIO as host interface, then firmware programming or update can be done through the host MCU, or if designer prefers to program standalone at manufacturing, then it is recommended to have test points on the SPI or SDIO signals.
2. 3.3 V/1.8 V/VBATT must be supplied by external source.
3. VBATT, SDIO_IO_VDD, IO_VDD, ULP_IO_VDD must be powered using External/On-board Power.
4. FLASH_IO_VDD is powered by 1V8_LDO output.
5. Place all the Caps closer to the corresponding Module pins.

8.1 SiW917Y1GN Schematics for Parts with RF Pin

8.1.1 System Supplies

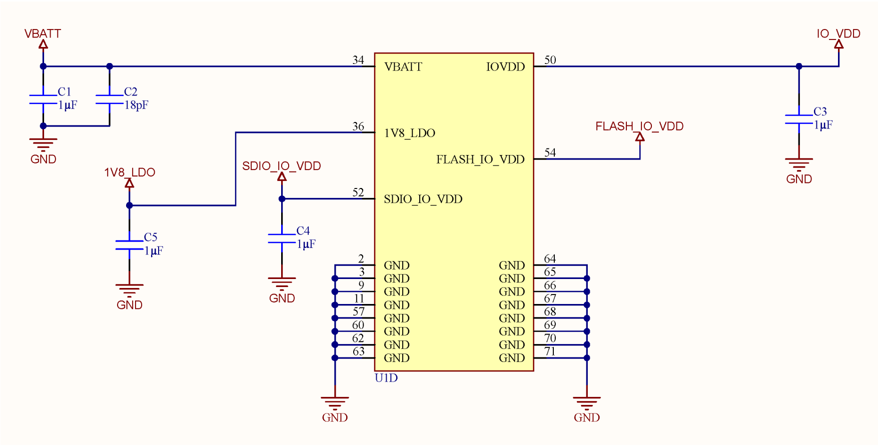


Figure 8.1. System Power Supplies

Note:

1. Place all the decoupling capacitors close to the module pins.
2. IO_VDD, SDIO_IO_VDD, ULP_IO_VDD can be powered independently by different voltage sources based on their corresponding signals voltage levels requirements. Voltages must be as per Table 7.2 Recommended Operating Conditions on page 92.
3. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.

8.1.2 RF, JTAG, and Reset Connection

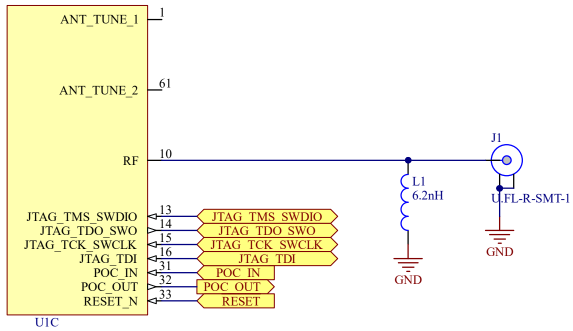


Figure 8.2. RF, JTAG, and Reset Connection

Note:

1. Place L1 close to the RF pin.
2. It is mandatory to follow the reference schematics for optimal RF performance.
3. Maintain 50 ohm characteristic impedance for RF traces.
4. J1: In-built antenna or an external antenna (with U.FL connector) can be used.
5. It is recommended to add microwave coaxial switch connector (Example : Murata's MM8430-2610RA1) or U.FL connector for conducted measurements.
6. Additional matching circuit to be provided near the antenna, based on antenna used and location on the board.

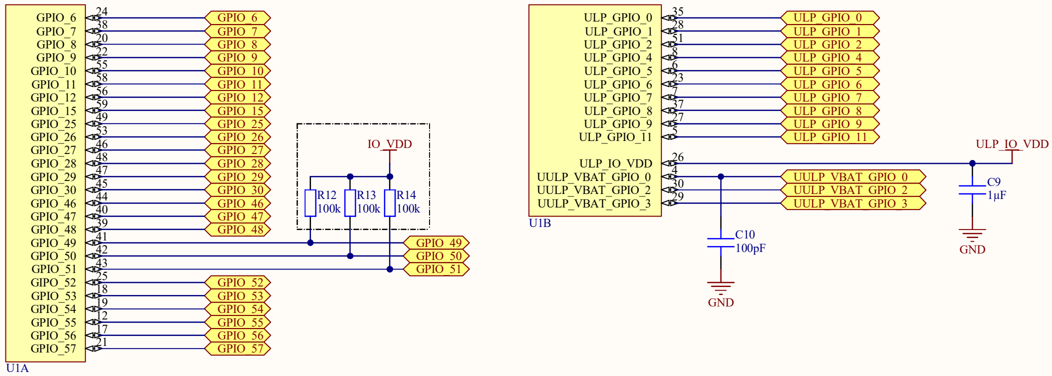


Figure 8.3. GPIO Connection

Note:

1. Place all the decoupling capacitors close to the module pins.
2. IO_VDD, SDIO_IO_VDD, ULP_IO_VDD can be powered independently by different voltage sources based on their corresponding signals voltage levels requirements. Voltages must be as per Table 7.2 Recommended Operating Conditions on page 92.
3. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.
4. IO_VDD domain must be same as PSRAM supply in case of External PSRAM.
5. Use recommended External PSRAM IC's as per the PSRAM section of the data sheet.
6. PSRAM and Flash configurations:
   a. If the module does not require external PSRAM and requires external Flash, then external flash can be connected to 46:51 or 52:57.
   b. If module requires external PSRAM and does not require external Flash, then external PSRAM can be connected to 46:51 or 52:57.
   c. If module requires both external flash and PSRAM, then external flash must be connected to 46:51, and external PSRAM must be connected to 52:57.
   d. The default pinset for external Flash is GPIO 46:51, while the default pinset for external PSRAM is GPIO 52:57.
   e. If either external Flash or external PSRAM is to be connected other than the default pinset, a change of MBR is required as described in UG574: SiWx917 SoC Manufacturing Utility User Guide, section 9.2.
   f. R12, R13, and R14 resistors must be mounted for OPNs having on-module Flash (for example, SiWG917Y121MGNBA or SiWG917Y121MGABA). For other OPNs, these resistors are recommended if external Flash is connected on GPIO_49 to GPIO_51. Check additional notes in section 8.1.6 Flash Memory Configurations for more details about external Flash connections and these resistors.
7. IO_VDD and its corresponding GPIOs in IO_VDD domain must be 1.8 V when 1.8 V external flash is used.
8. IO_VDD and its corresponding GPIOs in IO_VDD domain must be 3.3 V when 3.3 V external flash is used.
9. Use recommended External Flash ICs as per the Flash section of the data sheet.
10. Place filtering capacitor C10 close to Module Pin.

8.1.4 Reset

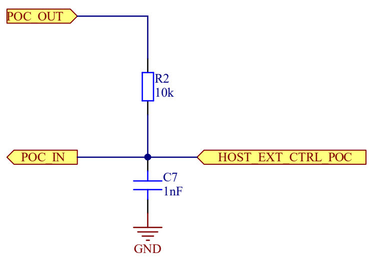


Figure 8.4. Reset Configuration

Note:

1. The configuration shown allows for blackout monitor functionality along with external reset of the SiWG917 module.
2. The POC_IN signal connects to the POC_IN pin on the SiWG917 module. POC_IN resets all the internal blocks of the IC.
3. The Si917_RESET signal connects to the RESET_N pin on the SiWG917 module. It is recommended to use the RC filter as shown. RESET_N is an open-drain output pin that will be pulled low when POC_IN goes low.
4. The POC_OUT signal connects to the POC_OUT pin on the SiWG917 module. POC_OUT is an active-low, push-pull output from the internal blackout monitor. In this configuration, it is isolated from the external HOST_EXT_CTRL_POC signal with a series resistor. In applications without external host control (HOST_EXT_CTRL_POC), POC_OUT may be directly connected to POC_IN. Without external host control to the POC_IN pin, the module cannot be reset multiple times after power-on.
5. The HOST_EXT_CTRL_POC signal connects to a GPIO of an external host processor. In this configuration, HOST_EXT_CTRL_POC must be an open-drain output to allow POC_OUT to control POC_IN.
6. HOST_EXT_CTRL_POC must be at the same voltage level as the VBATT supply pin.

8.1.5 LF Clock Option

Note: For Wi-Fi, BLE, and Co-Ex power saving use cases & high accuracy MCU applications, Silicon Labs mandates an external clock to be used on UULP_VBAT_GPIO_3 pin for the low-frequency clock source to maintain timing accuracy requirements and optimize power consumption.

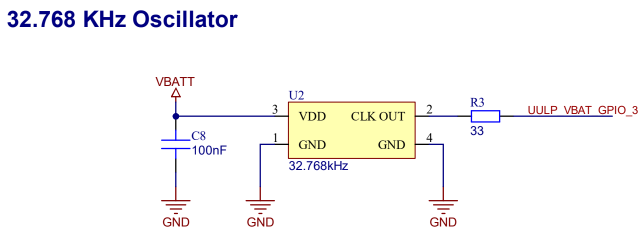


Figure 8.5. 32.768 kHz Clock Oscillator

8.1.6 Flash Memory Configurations

Figure 8.6. Option 1: In-Package Common Flash (NWP + MCU) Powered From On-Chip LDO Supply

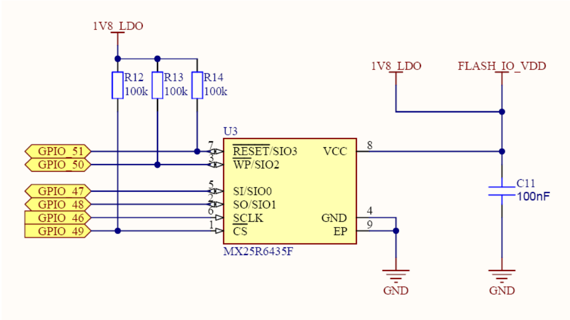


Figure 8.7. Option 2: In-Package NWP Flash + External 1.8 V MCU Flash Powered From On-Chip LDO Supply

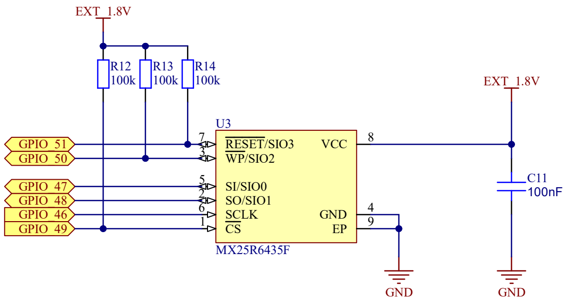


Figure 8.8. Option 3: External 1.8 V Common Flash (NWP + MCU) Powered From External 1.8 V Supply

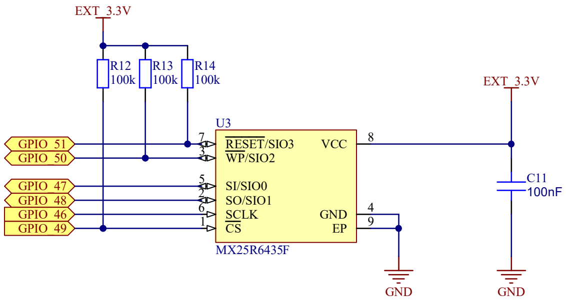


Figure 8.9. Option 4: External 3.3 V Common Flash (NWP + MCU) Powered From External 3.3 V Supply

Note:

1. Option 3 and Option 4 show single common flash to be used with both the NWP and MCU. A dual external flash configuration is also possible. The flash used for NWP must be connected to GPIO 46:51. A second external flash for MCU can be attached to GPIO 52:57.
2. IO_VDD and its corresponding GPIOs in IO_VDD domain must be 1.8 V when 1.8 V external flash is used.
3. IO_VDD and its corresponding GPIOs in IO_VDD domain must be 3.3 V when 3.3 V external flash is used.
4. See 5.6.1.18 SPI Flash Controllers for more information on external flash interface capabilities, and refer to AN1494: SiWx917 External Flash and PSRAM Application Note for recommended external flash ICs.
5. If Flash is used at GPIO 46:51 or GPIO 52:57 they are reserved for Flash usage only.

8.1.7 PSRAM Memory Configurations

Figure 8.10. Option 1: In-Package PSRAM Powered From On-Chip LDO Supply

Figure 8.11. Option 2: In-Package PSRAM Powered From External 1.8 V Supply

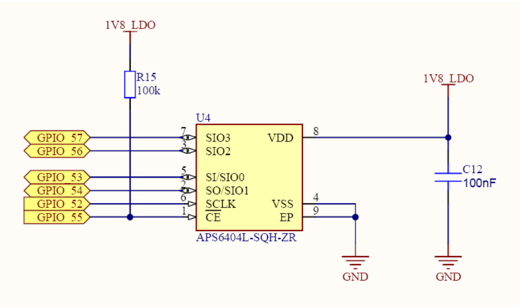


Figure 8.12. Option 3: External PSRAM Powered From On-Chip LDO Supply

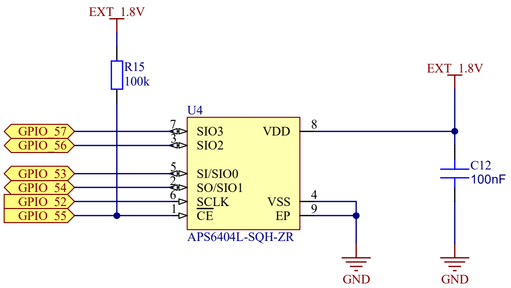


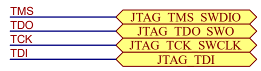
Figure 8.13. Option 4: External PSRAM Powered From External 1.8 V Supply

Note:

1. IO_VDD and its corresponding GPIOs in the IO_VDD domain must be same as PSRAM supply in case of external PSRAM.
2. Either GPIO 46:51 or GPIO 52:57 can be used as the external PSRAM interface. For external common flash mode, the flash device must be connected to GPIO 46:51, and PSRAM must be connected to GPIO 52:57.
3. Standby associated current numbers vary based on the above option used.
4. The reference schematics represent a sample of configurations. See 5.6.1.20 FLASH and PSRAM Supply Connections for more details on possible configurations.
5. If PSRAM is used at GPIO 46:51 or GPIO 52:57 they are reserved for PSRAM usage only.
6. Refer to AN1494: SiWx917 External Flash and PSRAM Application Note for recommended external PSRAM ICs.

8.1.8 Debug and In-System Programming

Option 1: JTAG



Option 2: Serial Wire Debug

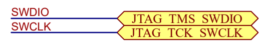


Figure 8.14. JTAG or Serial Wire Debug Interface

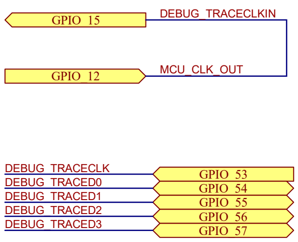
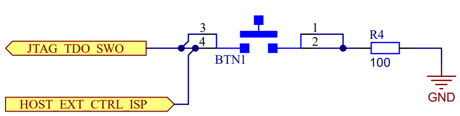


Figure 8.15. ETM Trace Interface

Note:

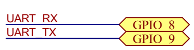
1. It is recommended to use GPIO 53:57 for ETM trace. GPIO 47:51 can also be used.
2. If external flash or external PSRAM are connected on GPIO 46:51 and GPIO 52:57 then ETM trace is not available.

SiWG917 In-System Programming (ISP)

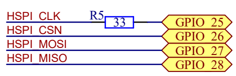


ISP Interfaces

Option 1: UART



Option 2: HSPI



Option 3: SDIO

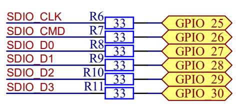


Figure 8.16. In-System Programming (ISP) Options

Note:

1. In UART mode, ensure that the input signal, UART_RX is not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset.

2. In HSPI mode, ensure that the input signals, HSPI_CSN and HSPI_CLK are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the external Host processor configures its signals (outputs) before deasserting the reset. HSPI_INTR is the interrupt signal driven by the secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required.

   The following actions can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.

   a. To use the signal in the Active-high or Active-low mode, ensure that during the power up of the device, the Interrupt is disabled in the Host processor before deasserting the reset. After deasserting the reset, the Interrupt needs to be enabled only after the HSPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
   b. The Host processor needs to disable the interrupt before the ULP Sleep mode is entered and enable it after SPI interface is reinitialized upon wakeup from ULP Sleep.
3. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification version 2.0.
4. R5 to R11 are optional resistors for signal integrity.
5. 33 ohm on SDIO_CLK/HSPI_CLK has to be near the source of the clock, and not near the module.
6. BTN1 button is optional and need not be used for every use-case.
7. Module enters ISP mode by driving JTAG_TDO_SWO low.

8.1.9 Bill of Materials

Table 8.1. Bill of Materials

Line No	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description	Tolerance	Rating
1	5	C1, C3, C4, C5, C9	1 uF	—	—	CAP CER 0402 X5R 1 uF 10 V 10 %	10 %	10 V
2	1	C2	18 pF	—	—	CAP CER 0201 C0G 18 pF 25 V 2 %	2 %	25 V
3	1	C6	10 nF	—	—	CAP CER 0402 X7R 10 nF 16 V 10 %	10 %	16 V
4	1	C7	1 nF	—	—	CAP CER 0402 X7R 1 nF 16 V 10 %	10 %	16 V
5	1	C8	100 nF	—	—	CAP CER 0402 X7R 100 nF 50 V 10 %	10 %	50 V
6	1	C10	100 pF	—	—	CAP CER 0201 C0G 100 pF 50 V 2 %	2 %	50 V
7	1	J1	U.FL-R-SMT-1	—	—	CONN RF 50 OHM UFL_2.6x2.6 SMD	—	—
8	1	L1	6.2 nH	—	—	IND Fixed 0201 6.2 nH 300 mA 600 mOhm 3 %	3 %	300 mA
9	1	R1	100 k	—	—	RES 0402 100 K 1/16 W 1 %	1 %	63 mW
10	1	R2	10 k	—	—	RES 0402 10 K 1/16 W 1 %	1 %	63 mW
11	8	R3, R5, R6, R7, R8, R9, R10, R11	33	—	—	RES 0402 33R 1/16W 1%	1 %	63 mW
12	1	R4	100	—	—	RES 0402 100R 1/16 W 1 %	1 %	63 mW
13	1	BTN1	PTS810 SJM 250 SMTR LFS	C&K	PTS810 SJM 250 SMTR LFS	C&K Tactile Switch SPST-NO 0.05 A 16 V	—	—
14	1	U1	SiW917Y1GN	Silicon Labs	—	PCB Module SiW917Y1GN	—	—
15	1	U2	32.768 kHz	SiTIME	SiT1532AI-J4-DCC-32.768	SiTIME Oscillator CSPBGA 32.768 kHz 10 pF 100 ppm	—	—

Table 8.2. SiWG917: External Flash & PSRAM BOM Options (these are optional and need not be used for every use-case)

Line no	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description	Tolerance	Rating
1	1	U3	MX25R6435F	Macronix	MX25R6435FM2IL0	IC FLASH 64 MBIT SPI/QUAD 8SOP	—	—
2	1	U4	APS6404L-SQH-ZR	AP Memory	APS6404L-SQH-ZR	IC PSRAM 64 Mbit QSPI USON	—	—
3	4	R12, R13, R14, R15	100 k	—	RES 0402 100 K 1/16W 1 %	—	1 %	63 mW
4	2	C11, C12	100 nF	—	CAP CER 0402 X7R 100 nF 50 V 10 %	—	10 %	50 V

8.2 SiW917Y1GA Schematics for Parts with Integral Antenna

8.2.1 System Supplies

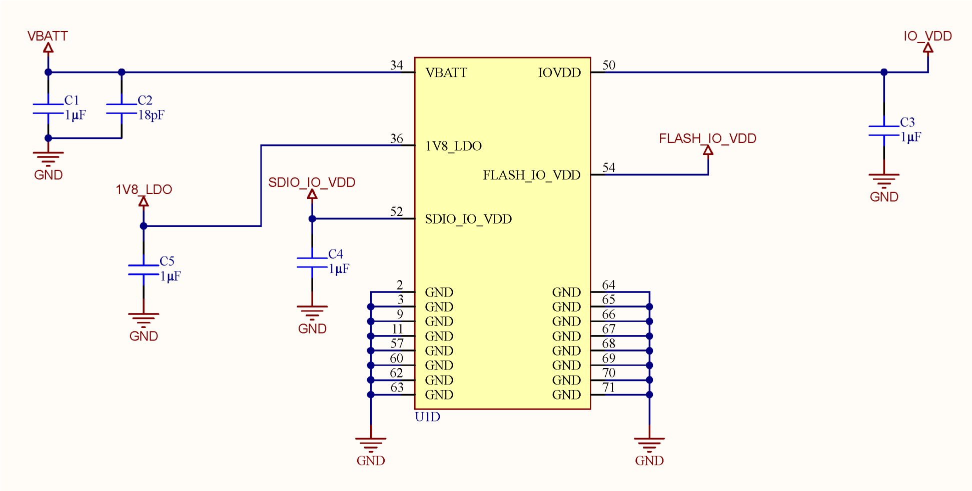


Figure 8.17. System Power Supplies

Note:

1. Place all the decoupling capacitors close to the module pins.
2. IO_VDD, SDIO_IO_VDD, ULP_IO_VDD can be powered independently by different voltage sources based on their corresponding signals voltage levels requirements. Voltages must be as per Table 7.2 Recommended Operating Conditions on page 92.
3. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.

8.2.2 RF, JTAG, and Reset Connection

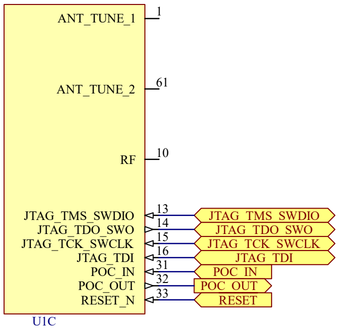


Figure 8.18. RF, JTAG, and Reset Connection

Note:

1. It is mandatory to follow the reference schematics for optimal RF performance.

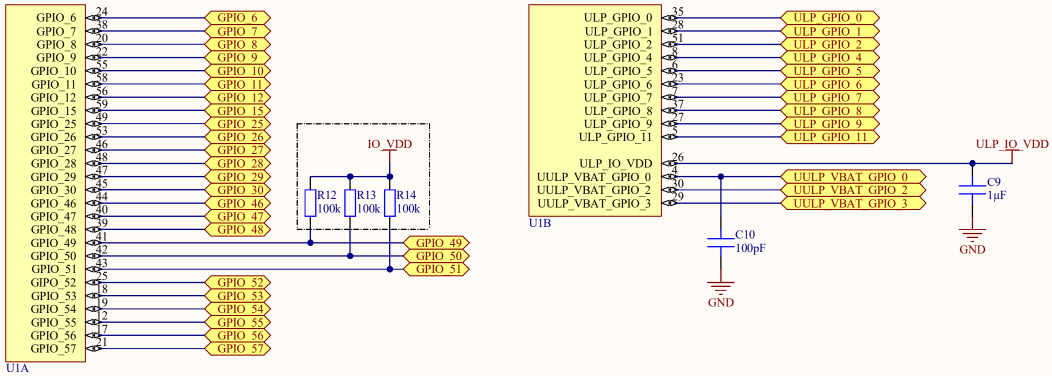


Figure 8.19. GPIO Connection

Note:

1. Place all the decoupling capacitors close to the module pins.
2. IO_VDD, SDIO_IO_VDD, ULP_IO_VDD can be powered independently by different voltage sources based on their corresponding signals voltage levels requirements. Voltages must be as per Table 7.2 Recommended Operating Conditions on page 92.
3. Even if GPIOs are not used, their respective IO domains must still be connected to the power supply.
4. IO_VDD domain must be same as PSRAM supply in case of External PSRAM.
5. Use recommended External PSRAM IC's as per the PSRAM section of the data sheet.
6. PSRAM and Flash configurations:
   a. If the module does not require external PSRAM and requires external Flash, then external flash can be connected to 46:51 or 52:57.
   b. If module requires external PSRAM and does not require external Flash, then external PSRAM can be connected to 46:51 or 52:57.
   c. If module requires both external flash and PSRAM, then external flash must be connected to 46:51, and external PSRAM must be connected to 52:57.
   d. The default pinset for external Flash is GPIO 46:51, while the default pinset for external PSRAM is GPIO 52:57.
   e. If either external Flash or external PSRAM is to be connected other than the default pinset, a change of MBR is required as described in UG574: SiWx917 SoC Manufacturing Utility User Guide, section 9.2.
   f. R12, R13, and R14 resistors must be mounted for OPNs having on-module Flash (for example, SiWG917Y121MGNBA or SiWG917Y121MGABA). For other OPNs, these resistors are recommended if external Flash is connected on GPIO_49 to GPIO_51. Check additional notes in section 8.2.6 Flash Memory Configurations for more details about external Flash connections and these resistors.
7. IO_VDD and its corresponding GPIOs in IO_VDD domain must be 1.8 V when 1.8 V external flash is used.
8. IO_VDD and its corresponding GPIOs in IO_VDD domain must be 3.3 V when 3.3 V external flash is used.
9. Use recommended External Flash IC's as per the Flash section of the data sheet.
10. Place filtering capacitor C10 close to Module Pin.

Board name SiWG917Y [No Variations]
Designer Approved Page title *
Size A3 Sheet Modified Date 24.6.2025 Board number
COPYRIGHT SILICON LABORATORIES INC. 2022 CONFIDE

8.2.4 Reset

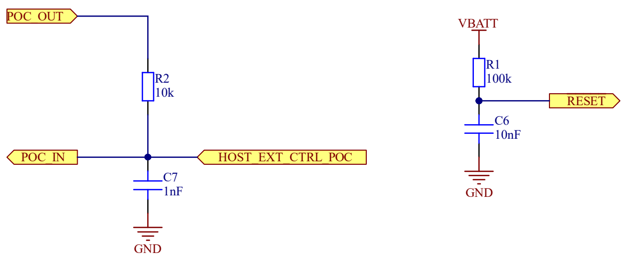


Figure 8.20. Reset Configuration

Note:

1. The configuration shown allows for blackout monitor functionality along with external reset of the SiWG917 module.
2. The POC_IN signal connects to the POC_IN pin on the SiWG917 module. POC_IN resets all the internal blocks of the IC.
3. The Si917_RESET signal connects to the RESET_N pin on the SiWG917 module. It is recommended to use the RC filter as shown. RESET_N is an open-drain output pin that will be pulled low when POC_IN goes low.
4. The POC_OUT signal connects to the POC_OUT pin on the SiWG917 module. POC_OUT is an active-low, push-pull output from the internal blackout monitor. In this configuration, it is isolated from the external HOST_EXT_CTRL_POC signal with a series resistor. In applications without external host control (HOST_EXT_CTRL_POC), POC_OUT may be directly connected to POC_IN. Without external host control to the POC_IN pin, the module cannot be reset multiple times after power-on.
5. The HOST_EXT_CTRL_POC signal connects to a GPIO of an external host processor. In this configuration, HOST_EXT_CTRL_POC must be an open-drain output to allow POC_OUT to control POC_IN.
6. HOST_EXT_CTRL_POC must be at the same voltage level as the VBATT supply pin.

8.2.5 LF Clock Option

Note: For Wi-Fi, BLE, and Co-Ex power saving use cases & high accuracy MCU applications, Silicon Labs mandates an external clock to be used on UULP_VBAT_GPIO_3 pin for the low-frequency clock source to maintain timing accuracy requirements and optimize power consumption.

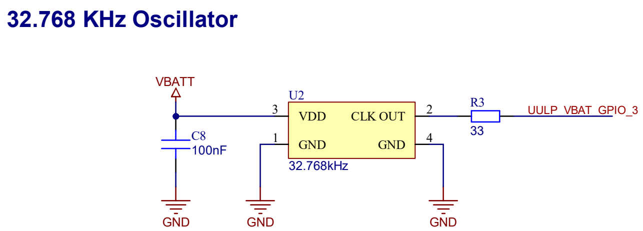


Figure 8.21. 32.768 kHz Clock Oscillator

8.2.6 Flash Memory Configurations

Figure 8.22. Option 1: In-Package Common Flash (NWP + MCU) Powered From On-Chip LDO Supply

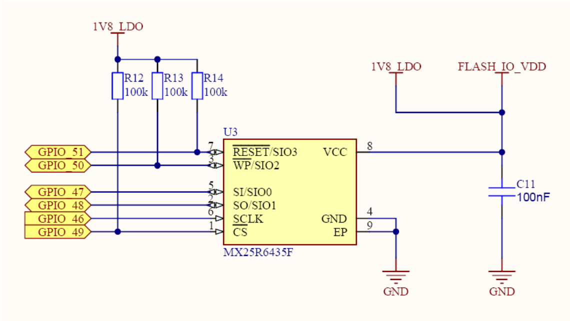


Figure 8.23. Option 2: In-Package NWP Flash + External 1.8 V MCU Flash Powered From On-Chip LDO Supply

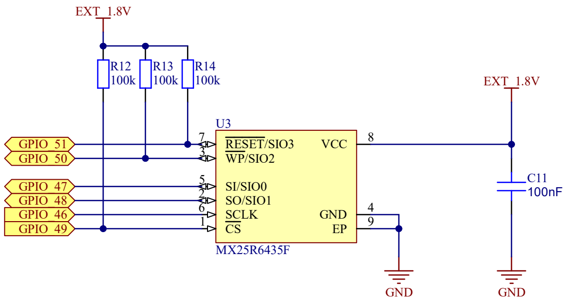


Figure 8.24. Option 3: External 1.8 V Common Flash (NWP + MCU) Powered From External 1.8 V Supply

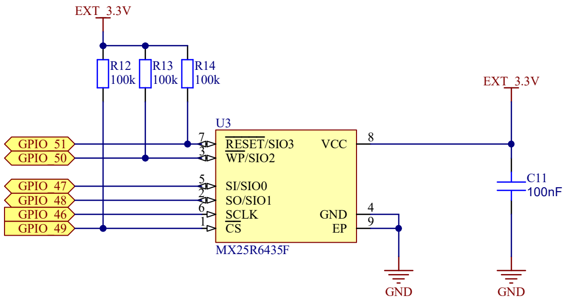


Figure 8.25. Option 4: External 3.3 V Common Flash (NWP + MCU) Powered From External 3.3 V Supply

Note:

1. Option 3 and Option 4 show single common flash to be used with both the NWP and MCU. A dual external flash configuration is also possible. The flash used for NWP must be connected to GPIO 46:51. A second external flash for MCU can be attached to GPIO 52:57.
2. IO_VDD and its corresponding GPIOs in IO_VDD domain must be 1.8 V when 1.8 V external flash is used.
3. IO_VDD and its corresponding GPIOs in IO_VDD domain must be 3.3 V when 3.3 V external flash is used.
4. See 5.6.1.18 SPI Flash Controllers for more information on external flash interface capabilities, and refer to AN1494: SiWx917 External Flash and PSRAM Application Note for recommended external flash ICs.
5. If Flash is used at GPIO 46:51 or GPIO 52:57 they are reserved for Flash usage only.

8.2.7 PSRAM Memory Configurations

Figure 8.26. Option 1: In-Package PSRAM Powered From On-Chip LDO Supply

Figure 8.27. Option 2: In-Package PSRAM Powered From External 1.8 V Supply

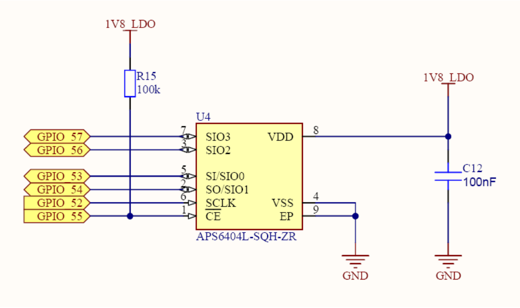


Figure 8.28. Option 3: External PSRAM Powered From On-Chip LDO Supply

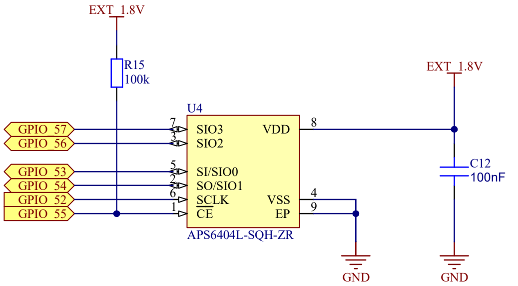


Figure 8.29. Option 4: External PSRAM Powered From External 1.8 V Supply

Note:

1. IO_VDD and its corresponding GPIOs in the IO_VDD domain must be same as PSRAM supply in case of external PSRAM.
2. Either GPIO 46:51 or GPIO 52:57 can be used as the external PSRAM interface. For external common flash mode, the flash device must be connected to GPIO 46:51, and PSRAM must be connected to GPIO 52:57.
3. Standby associated current numbers vary based on the above option used.
4. The reference schematics represent a sample of configurations. See 5.6.1.20 FLASH and PSRAM Supply Connections for more details on possible configurations.
5. If PSRAM is used at GPIO 46:51 or GPIO 52:57 they are reserved for PSRAM usage only.
6. Refer to AN1494: SiWx917 External Flash and PSRAM Application Note for recommended external PSRAM ICs.

8.2.8 Debug and In-System Programming

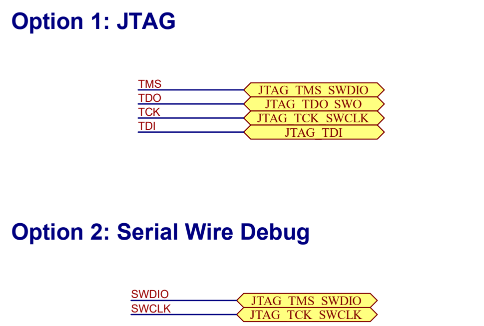


Figure 8.30. JTAG or Serial Wire Debug Interface

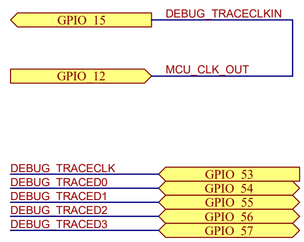


Figure 8.31. ETM Trace Interface

Note:

1. It is recommended to use GPIO 53:57 for ETM trace. GPIO 47:51 can also be used.
2. If external flash or external PSRAM are connected on GPIO 46:51 and GPIO 52:57 then ETM trace is not available.

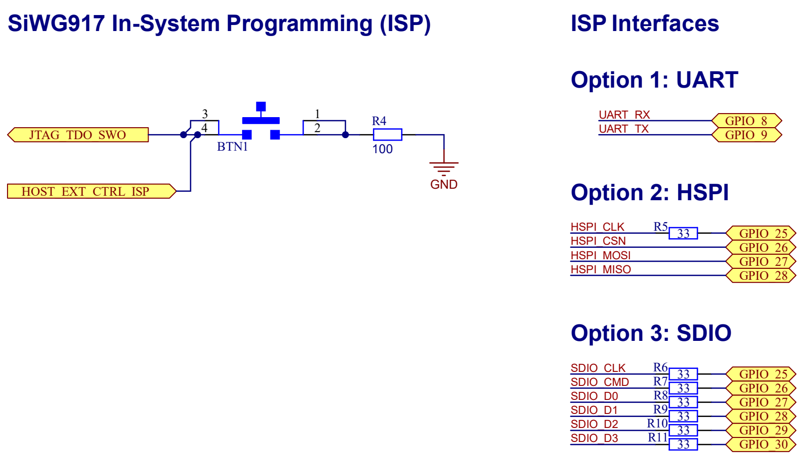


Figure 8.32. In-System Programming Options

Note:

1. In UART mode, ensure that the input signal, UART_RX is not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the host processor configures its signals (outputs) before deasserting the reset.

2. In HSPI mode, ensure that the input signals, HSPI_CSN and HSPI_CLK are not floating when the device is powered up and reset is deasserted. This can be done by ensuring that the external Host processor configures its signals (outputs) before deasserting the reset. HSPI_INTR is the interrupt signal driven by the secondary device. This signal may be configured as Active-high or Active-low. If it is active-high, an external pull-down resistor is required. If it is active-low, an external pull-up resistor is required.

   The following actions can be carried out by the host processor during power-up of the device, and before/after ULP Sleep mode.
   a. To use the signal in the Active-high or Active-low mode, ensure that during the power up of the device, the Interrupt is disabled in the Host processor before deasserting the reset. After deasserting the reset, the Interrupt needs to be enabled only after the HSPI initialization is done and the Interrupt mode is programmed to either Active-high or Active-low mode as required.
   b. The Host processor needs to disable the interrupt before the ULP Sleep mode is entered and enable it after SPI interface is reinitialized upon wakeup from ULP Sleep.
3. In SDIO mode, pull-up resistors should be present on SDIO_CMD & SDIO Data lines as per the SDIO physical layer specification version 2.0.
4. R5 to R11 are optional resistors for signal integrity.
5. 33 ohm on SDIO_CLK/HSPI_CLK has to be near the source of the clock, and not near the module.
6. BTN1 button is optional and need not be used for every use-case.
7. Module enters ISP mode by driving JTAG_TDO_SWO low.

8.2.9 Bill of Materials

Table 8.3. Bill of Materials

Line No	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description	Tolerance	Rating
1	5	C1, C3, C4, C5, C9	1 uF	—	—	CAP CER 0402 X5R 1 uF 10 V 10 %	10 %	10 V
2	1	C2	18 pF	—	—	CAP CER 0201 C0G 18 pF 25 V 2 %	2 %	25 V
3	1	C6	1 nF	—	—	CAP CER 0402 X7R 10 nF 16 V 10 %	10 %	16 V
4	1	C7	10 nF	—	—	CAP CER 0402 X7R 1 nF 16 V 10 %	10 %	16 V
5	1	C8	100 nF	—	—	CAP CER 0402 X7R 100 nF 50 V 10 %	10 %	50 V
6	1	C10	100 pF	—	—	CAP CER 0201 C0G 100 pF 50 V 2 %	2 %	50 V
9	1	R1	100 k	—	—	RES 0402 100K 1/16 W 1 %	1 %	63 mW
10	1	R2	10 k	—	—	RES 0402 10 K 1/16 W 1 %	1 %	63 mW
11	8	R3, R5, R6, R7, R8, R9, R10, R11	33	—	—	RES 0402 33R 1/16W 1%	1 %	63 mW
12	1	R4	100	—	—	RES 0402 100R 1/16 W 1 %	1 %	63 mW
13	1	BTN1	PTS810 SJM 250 SMTR LFS	C&K	PTS810 SJM 250 SMTR LFS	C&K Tactile Switch SPST-NO 0.05A 16V	—	—
14	1	U1	SiW917Y1GA	Silicon Labs	—	PCB Module SiW917Y1GA	—	—
15	1	U2	32.768 kHz	SiTIME	SiT1532AI-J4-DCC-32.768	SiTIME Oscillator CSPBGA 32.768 kHz 10 pF 100 ppm	—	—

Table 8.4. SiWG917: External Flash & PSRAM BOM Options (these are optional and need not be used for every use-case)

Line no	Quantity	Designator	Value	Manufacturer	Manufacturer PN	Description	Tolerance	Rating
1	1	U3	MX25R6435F	Macronix	MX25R6435F M2IL0	IC FLASH 64 MBIT SPI/ QUAD 8SOP	—	—
2	1	U4	APS6404L-SQH-ZR	AP Memory	APS6404L-SQH-ZR	IC PSRAM 64 Mbit QSPI USON	—	—
3	4	R12, R13, R14, R15	100 k	—	RES 0402 100 K 1/16W 1 %	—	1 %	63 mW
4	2	C11, C12	100 nF	—	CAP CER 0402 X7R 100 nF 50 V 10 %	—	10 %	50 V

8.3 Layout Guidelines

1. The RF (Module Pin No. 10) signal may be directly connected to an on-board chip antenna or terminated in an RF pin connector of any form factor for enabling the use of external antennas. RF pin can be left floating if not used.
2. Antenna clearance area is not necessary if you are using an external antenna attached to the RF pin.
3. The RF pin trace on RF pin should have a characteristic impedance of 50 Ohms. Any standard 50 Ohms RF pin trace (Microstrip or Coplanar wave guide) may be used. The width of the 50 Ohms line depends on the PCB stack, e.g., the dielectric of the PCB, thickness of the copper, thickness of the dielectric and other factors. Consult the PCB fabrication unit to get these factors right.
4. To evaluate transmit and receive performance like Tx Power, and EVM and Rx sensitivity, an RF pin connector would be required. A suggestion is to place a 'microwave coaxial connector with switch' between RF pin and the antenna.
5. Each GND pin must have a separate GND via. Place the ground vias as close to the ground pads as possible.
6. All decoupling capacitors placement must be as much close as possible to the corresponding power pins, and the trace lengths as short as possible.
7. Ensure all power supply traces widths are sufficient enough to carry corresponding currents.
8. Add GND copper pour underneath Module in all layers, for better thermal dissipation.
9. Add solid GND copper pour underneath Module for better emission performance.

8.3.1 Installation Guide for SiW917Y1GN Module

Figure 8.33 on page 159 below shows the recommended layout for SiW917Y1GN when using an u.fl connector for an external antenna. The short RF trace from the RF pad of the module to the pad of the u.fl connector must be 50 ohm and exactly the same width as the RF pad of the module, i.e., 700 µm. Figure 8.33 SiW917Y1GN Top Layer Application Layer with u.fl Connector on page 159 shows two examples on practical implementations of such a trace. The widths S is fixed to 700 um. The height h depends on the PCB stack-up, and the gap width W is adjusted until the impedance of the trace is exactly 50 ohm. Online calculators for coplanar waveguide with ground can be used to calculate the width W for any specific PCB stack-up. The integrator must consider using a unique connector, such as a "reverse polarity SMA" or "reverse thread SMA", if detachable antenna is offered with the host chassis.

Ground vias underneath the module must be used extensively especially around the rectangular GND pins to enable heat transfer from the bottom of the module to the GND plane of the host board. Routing signal lines elsewhere underneath the module is acceptable.

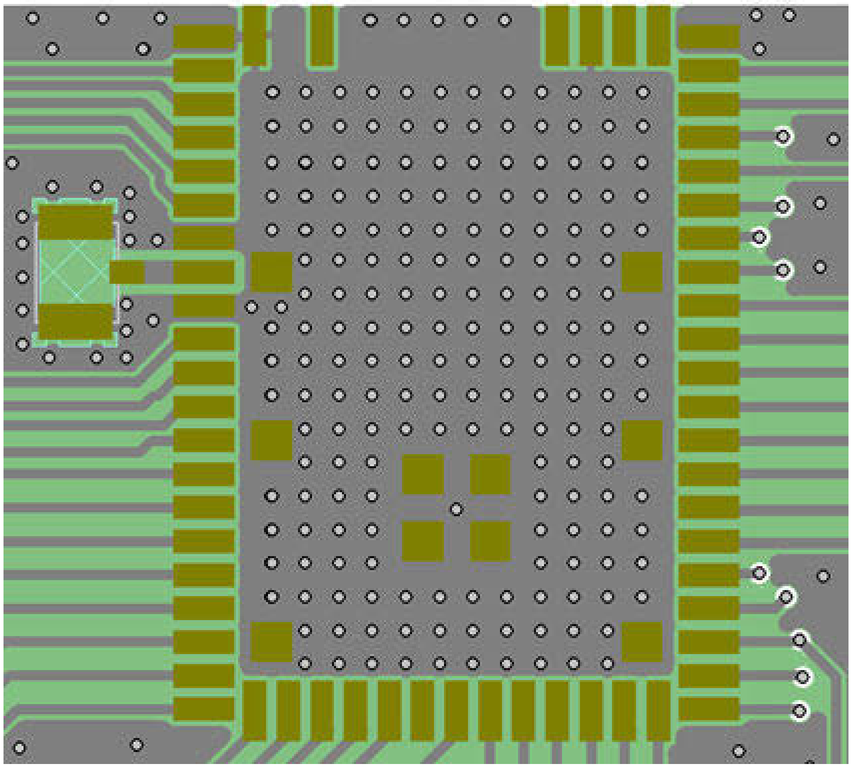


Figure 8.33. SiW917Y1GN Top Layer Application Layer with u.fl Connector

The typical permittivity of PCB laminate is 4.6. If assuming permittivity of 4.6, in the example shown in Figure 8.34 on page 160 the dimensions would be:

S = 700 um

h = 420 um

W = 332 um

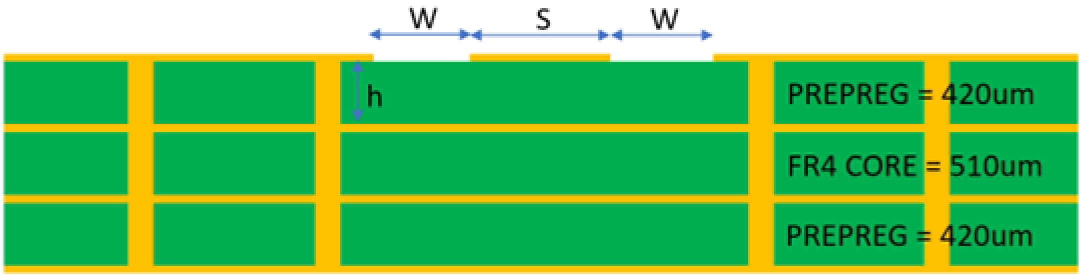


Figure 8.34. Example Implementation of a Co-planar Wave Guide with Ground and Thick Prepeg

Similarly, if assuming permittivity of 4.6, in the example shown in Figure 8.34 on page 160 the dimensions would be:

S = 700 um

h = 730 um

W = 132 um

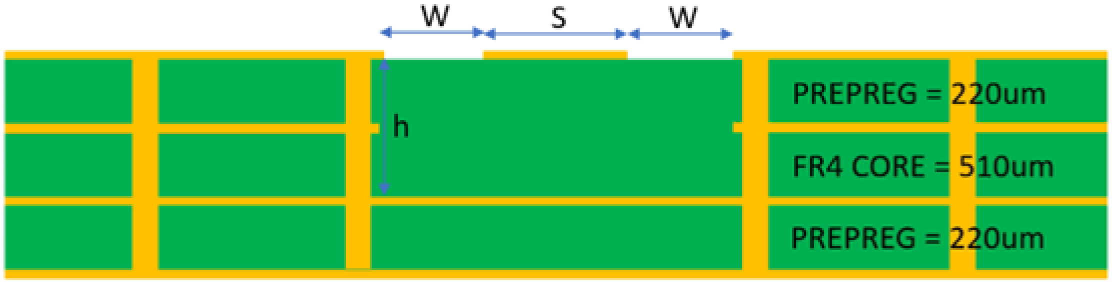
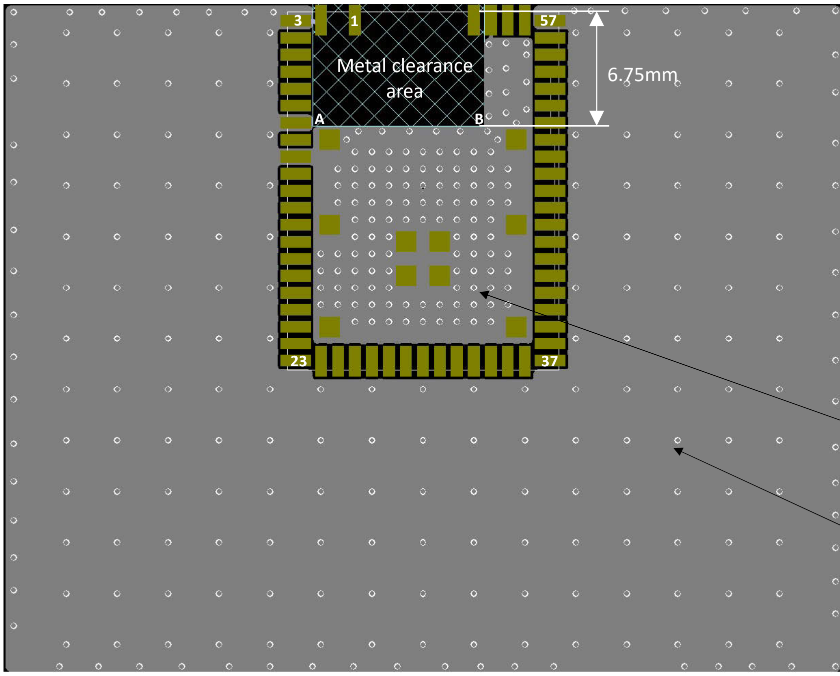


Figure 8.35. Example Implementation of a Co-planar Wave Guide with Ground and Thin Prepeg

8.3.2 Installation Guide for SiW917Y1GA Module



	X-cordinate (mm)	Y-cordinate (mm)
A (Corner of the metal clearance)	-6.5	3.8
B (Corner of the metal clearance)	3.6	3.8
1 (Center point of PAD1)	-4	10.05
3 (Center point of PAD3)	-7.5	10
23 (Center point of PAD23)	-7.5	-10
37 (Center point of PAD37)	7.5	-10
57 (Center point of PAD 57)	7.5	10

Figure 8.36. Application Layout of SiW917Y1GA

For optimal performance of the SiW917Y1GA:

- Place the module aligned to the edge of the application PCB, as illustrated in Figure 8.36 on page 161.
- Leave the antenna clearance area void of any traces, components, or copper on all layers of the application PCB.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Avoid plastic or any other dielectric material in direct contact with the antenna.

Figure 8.37 Figure on page 162 shows example layout scenarios which will lead to degraded performance and possible EMC issues with the module.

Ground vias underneath the module must be used extensively especially around the rectangular GND pins to enable heat transfer from the bottom of the module to the GND plane of the host board. Routing signal lines elsewhere underneath the module is acceptable.

Antennas are by nature affected by the surrounding PCB design and in particular the size and shape of the ground surrounding the antenna. The wide band antenna of SiW917Y1GA is designed to operate in various size/shape application boards and the antenna is not sensitive to dielectric material near the antenna. However, in certain extreme circumstances, such as extremely small board or narrow board, the antenna can be detuned enough to have an impact to the range, EVM characteristics and in-band emissions. In such cases it is possible to fine tune the antenna by using one or two external capacitors or inductors connected between the ANT_TUNE1 and GND and/or ANT_TUNE2 and GND. An example is shown in the Figure 8.38 Figure on page 162. Finding the correct value for these components requires empirical testing and measuring the antenna return loss. Typically capacitor with value between 0.5 pF to 2 pF or inductor with value between 2 nH to 4 nH can be used for tuning. (See the 8.4.2 Proximity to Human Body below.)

The best antenna performance is achieved when the board width is 50 mm and the antenna is placed at the center of the board edge. Having wider or narrower PCB will have up to 25 % impact to the range. If the board is narrower than 35mm or wider than 100 mm, it is possible that external fine tuning becomes necessary to maintain the EVM performance.

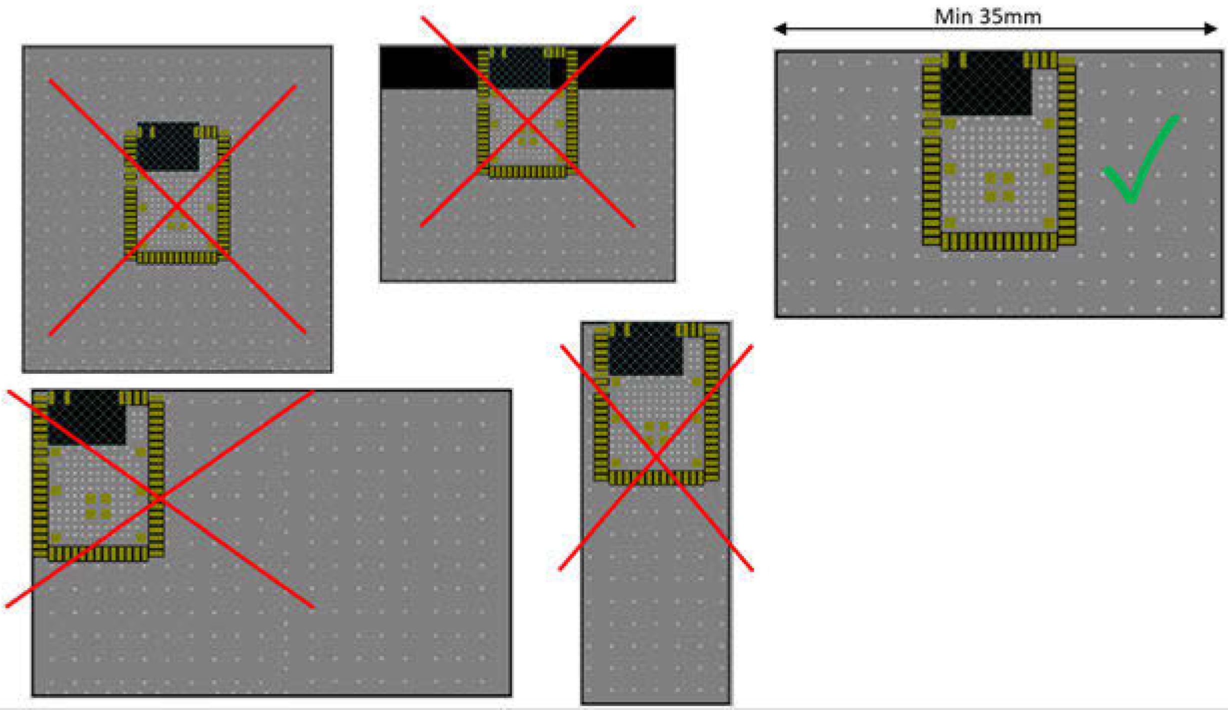


Figure 8.37. Layout Examples

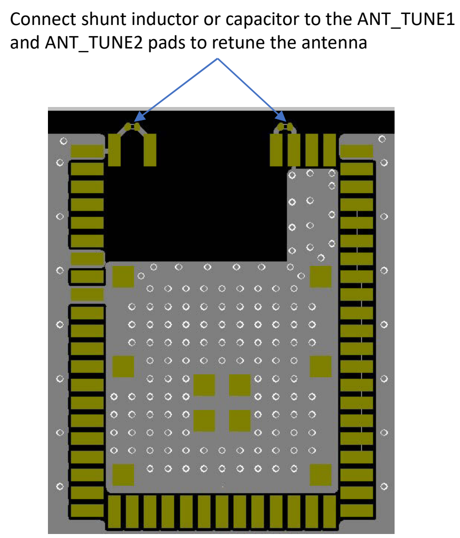


Figure 8.38. External Antenna Fine Tuning Option

8.4 SiW917Y1GA Antenna Radiation and Efficiency

Typical radiation patterns for the built-in antenna under optimal operating conditions are plotted in the figures that follow.

Table 8.5. Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 dB	Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna. Refer to 8.3.2 Installation Guide for SiW917Y1GA Module for recommendations to achieve optimal antenna performance.
Peak gain	2.26 dBi	
VSWR	2:1	

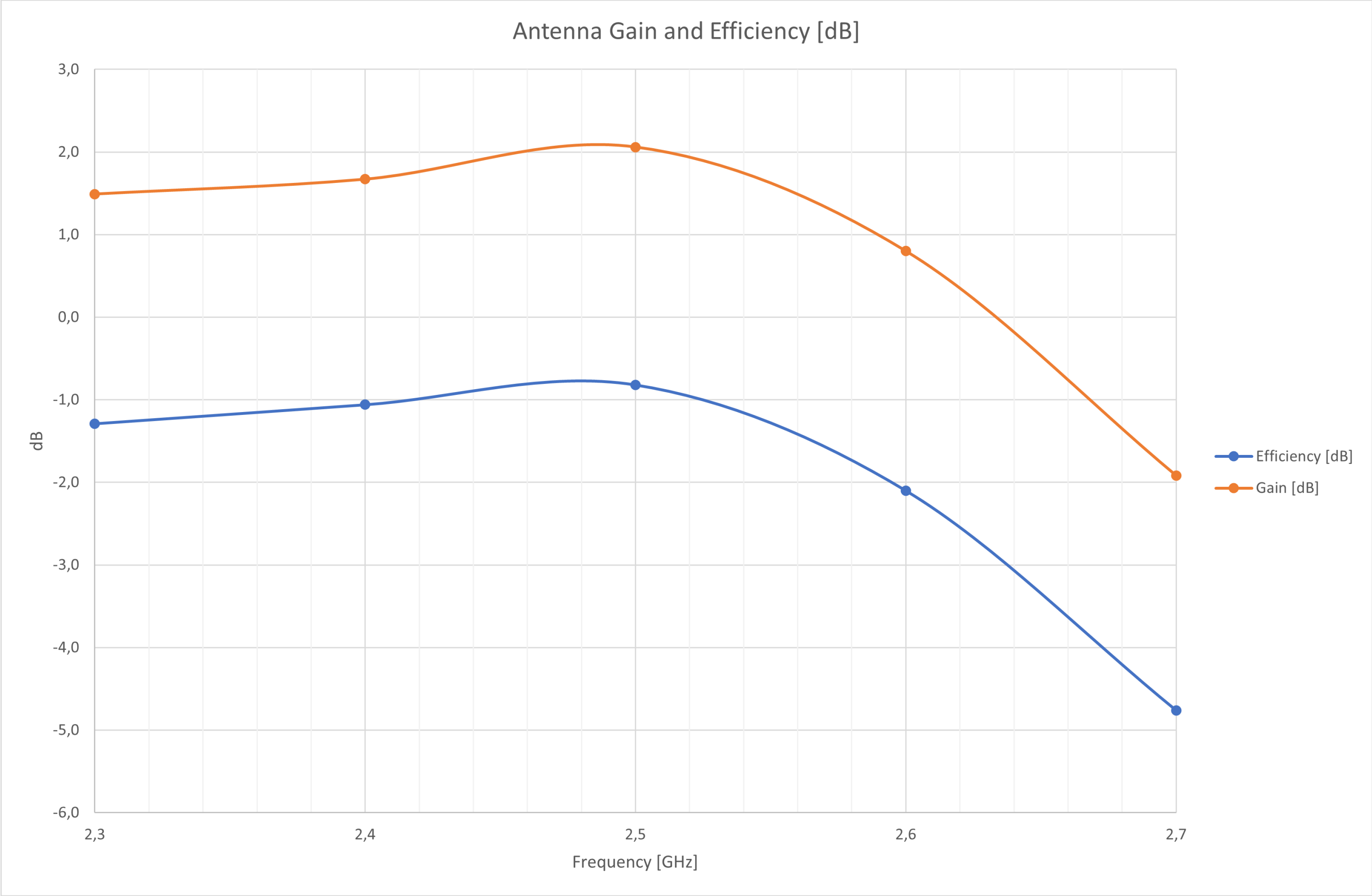


Figure 8.39. Efficiency and Gain of the Built-in Antenna

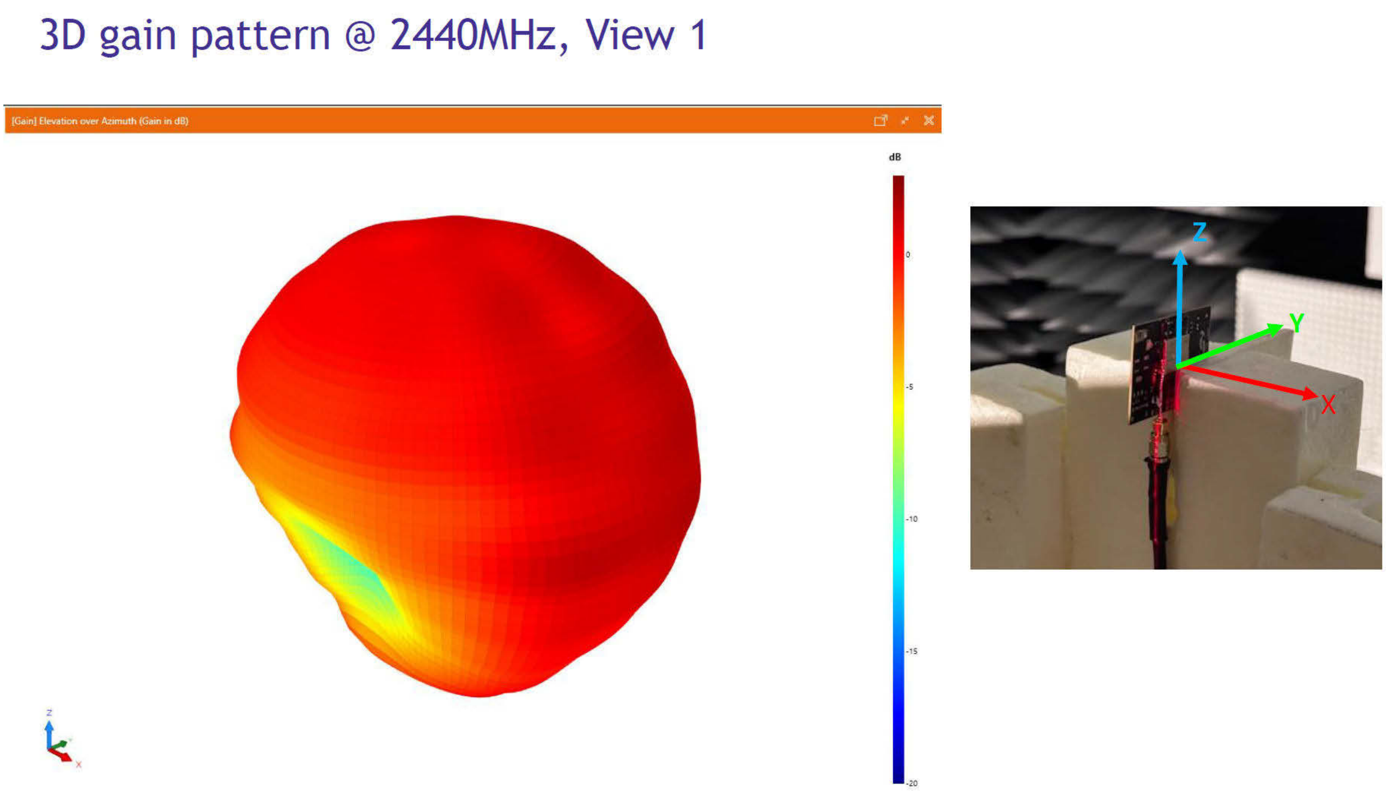


Figure 8.40. 3D Radiation Pattern of the Build-In Antenna

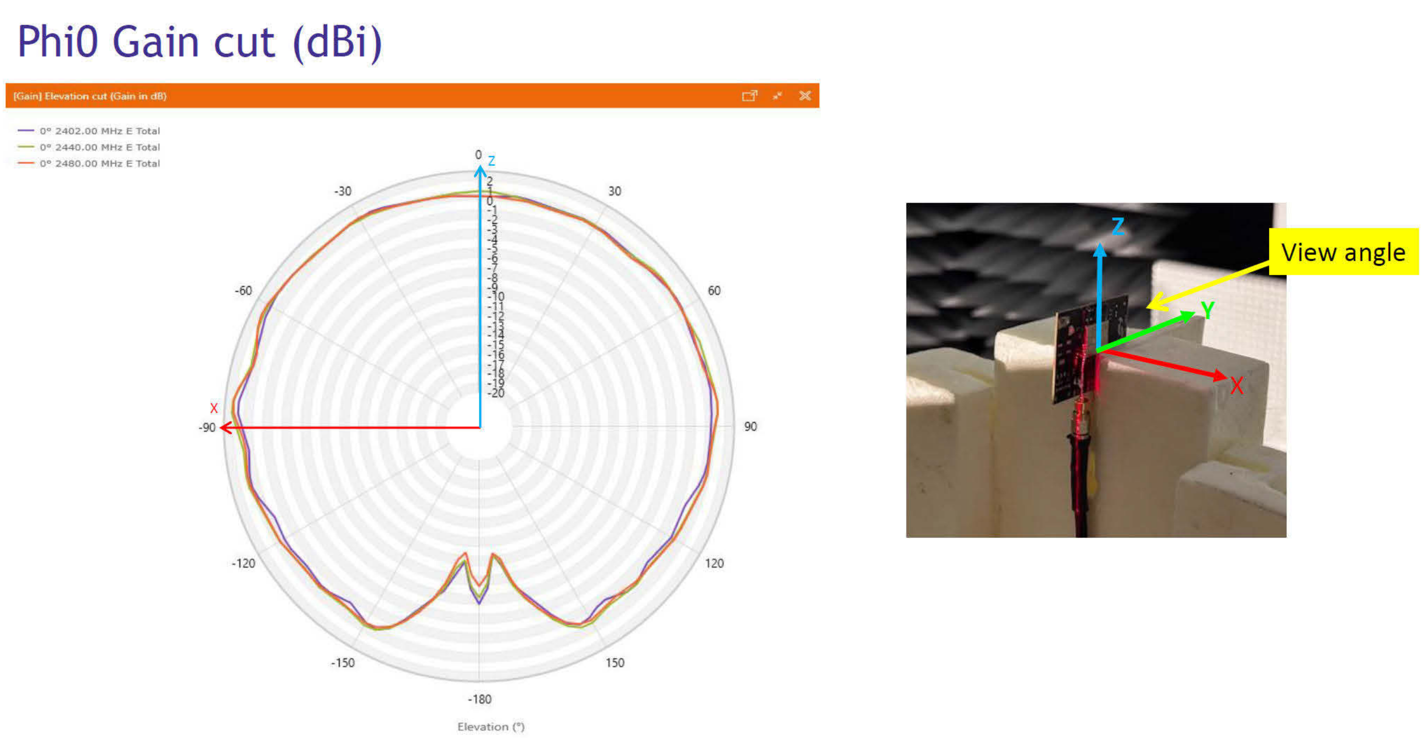


Figure 8.41. Typical 2D Antenna Radiation Patterns - Phi 0° (Side View) Gain (dBi)

Phi90 Gain cut

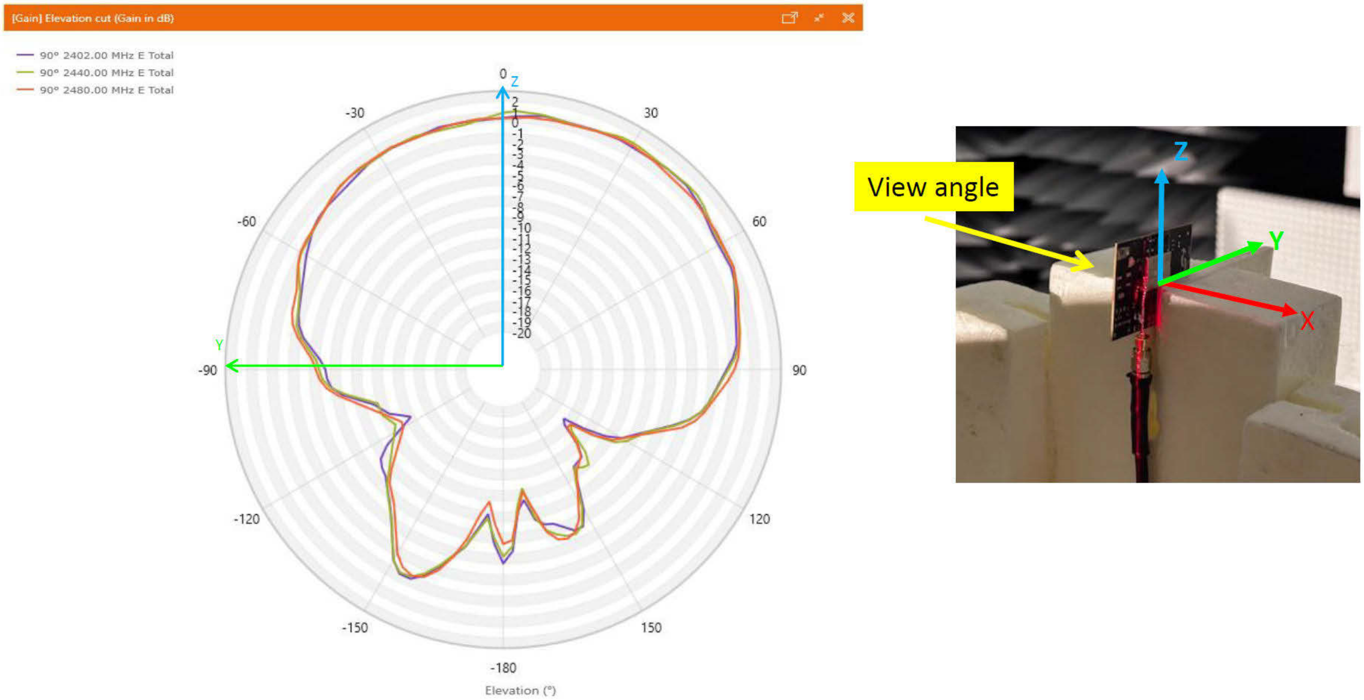


Figure 8.42. Typical 2D Antenna Radiation Patterns - Phi 90° (Top View) Gain (dBi)

Theta90 Gain cut

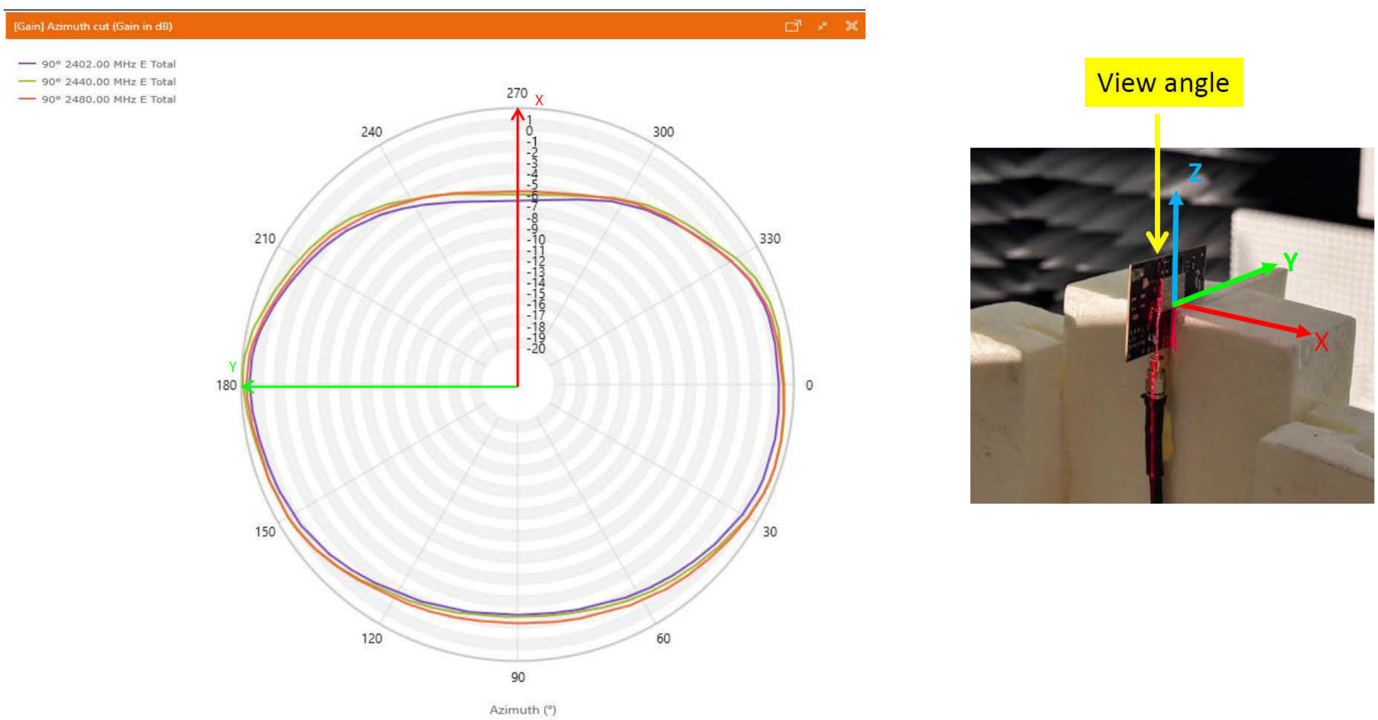


Figure 8.43. Typical 2D Antenna Radiation Patterns - Theta 90° (Front View) Gain (dBi)

8.4.1 Proximity to Other Materials

Avoid placing plastic or any other dielectric material in close proximity to the antenna. Conformal coating and other thin dielectric layers are acceptable directly on top of the antenna region, but this will also negatively impact antenna efficiency and reduce range.

Any metallic objects in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

8.4.2 Proximity to Human Body

Placing the module in contact with or very close to the human body will negatively impact antenna efficiency and reduce range.

Note: When it comes to modular certifications, following the manufacturer's design guidelines is critical for ensuring that compliance is maintained and modular approvals remain valid, in particular with regards to the carrier (host) PCB size, thickness, relative permittivity, and/or module placement. A modular certification is still valid if no antenna tuning is applied to compensate for reduced performance in terms of range, which may result from sub-optimal carrier PCB size, thickness, relative permittivity, module placement, and/or proximity to other materials such as assembly housing. Conversely, a custom antenna tuning might invalidate a modular certification, unless it is done to compensate for the degradation caused by a printed circuit board deviating from the manufacturer’s best-case reference design in terms of size, thickness, relative permittivity, and/or module placement. In such case, a Permissive Change to a modular approval might become necessary, depending on the resulting performance of the end-product relative to the certified module's test reports, in particular with regards to spurious emission levels, as found during spot-checking. For example, in the FCC case, a Class 1 Permissive Change (C1PC) is considered if the host PCB modifications do not increase emissions. Class 2 Permissive Change (C2PC) is considered if the modifications degrade the emissions but remain below regulatory limits. Whether antenna tuning is applied or not, it is strongly recommended that spot-checking is performed in any case with the end-product having the transmitter(s) operating, to confirm that the host product meets all regulatory requirements under any circumstance. In the end, the emission levels established in the module certification are limits for the end device too and determine whether or not a Permissive Change should be considered. Since this is evaluated on a case-by-case basis, integrators must consult with the company providing certification services for their final product to identify the best approach.

9. Package Specifications

9.1 Dimensions

Table 9.1. Module Dimensions

Parameter	Value (LxWxH)	Units
Module Dimensions	21.10 x 16 x 2.30	mm
Tolerance	±0.2	mm

9.2 Package Outline

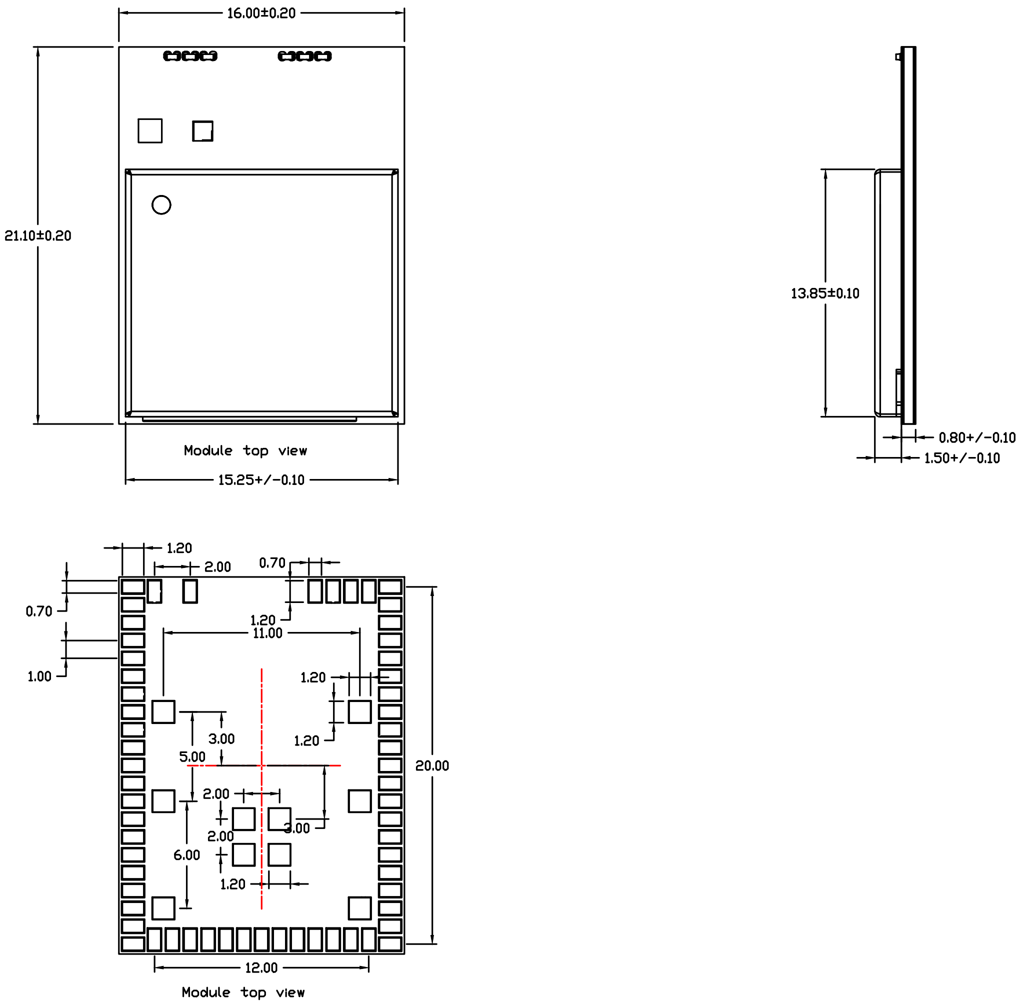


Figure 9.1. Package Outline

9.2.1 Pin Locations

Note: All coordinates in Table 9.2 Pin Locations on page 169 are in millimeters, and in TOP VIEW.

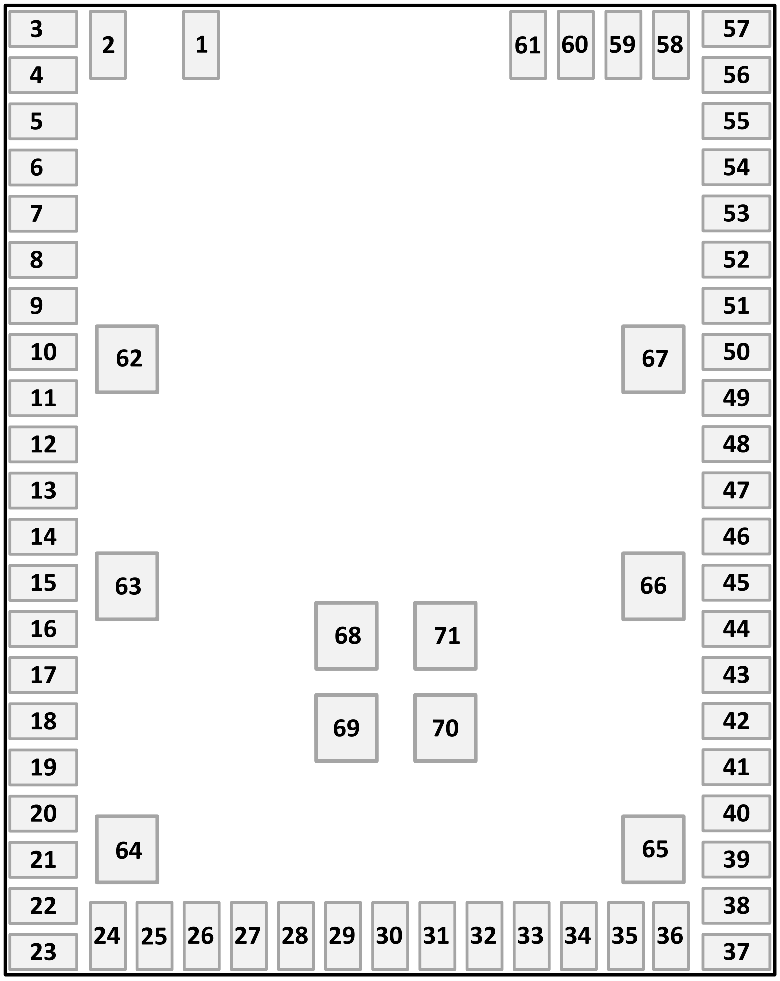


Figure 9.2. Pin Numbering

Table 9.2. Pin Locations

PAD X-Y Coordinates			
Pad #	**X**	**Y**	**Pad Size**
1	-4	9.75	(1.2 x 0.7) mm
2	-6	9.75	
3	-7.2	10	
23	-7.2	-10	
24	-6	-9.75	
36	6	-9.75	
37	7.2	-10	
57	7.2	-10	
58	6	9.75	
61	3	9.75	
62	-5.5	3	(1.2 x 1.2) mm
63	-5.5	-2	
64	-5.5	-8	
65	5.5	-8	
66	5.5	-2	
67	5.5	3	
68	-1	-3	
69	-1	-5	
70	1	-5	
71	1	-3	

9.3 PCB Landing Pattern

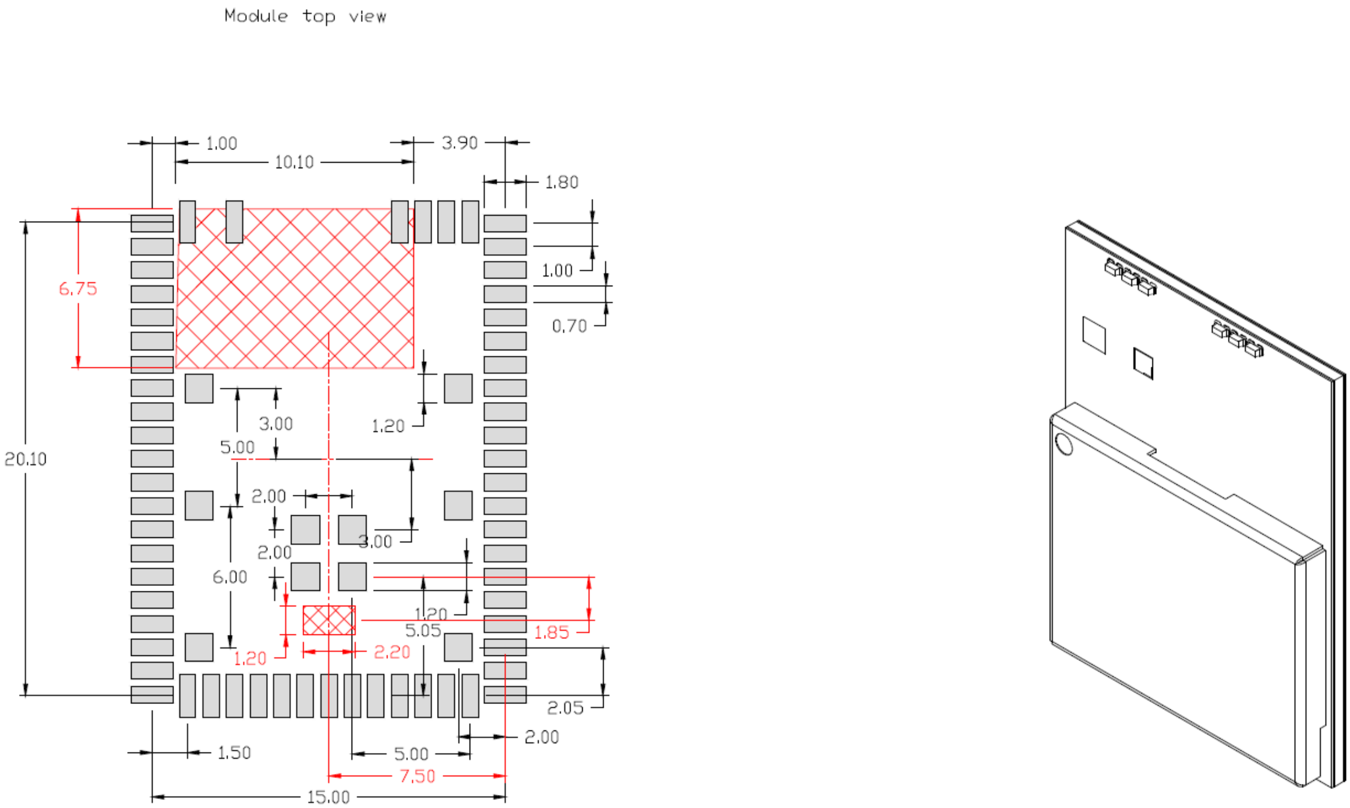


Figure 9.3. PCB Landing Pattern

Note:

1. We recommend allocating a dedicated hardware keep-out besides the antenna clearance area in the module layout to support future scalability within the same product series. Reserving this space enables smooth migration to upcoming part variants, minimizing the need for layout redesigns.
2. Both of the red-shaded areas shown above are keep-outs (metal clearance areas).

Table 9.3. PCB Landing Pattern Pin Locations

PAD X-Y Coordinates			
Pad #	**X**	**Y**	**Pad Size**
1	-4	10.05	(1.8 x 0.7) mm
2	-6	10.05	
3	-7.5	10	
23	-7.5	-10	
24	-6	-10.05	
36	6	-10.05	
37	7.5	-10	
57	7.5	10	
58	6	10.05	
61	3	10.05	
62	-5.5	3	(1.2 x 1.2) mm
63	-5.5	-2	
64	-5.5	-8	
65	5.5	-8	
66	5.5	-2	
67	5.5	3	
68	-1	-3	
69	-1	-5	
70	1	-5	
71	1	-3	

9.4 Module Marking Information

The figures below illustrate the markings on the single-band modules and the table explains the markings.

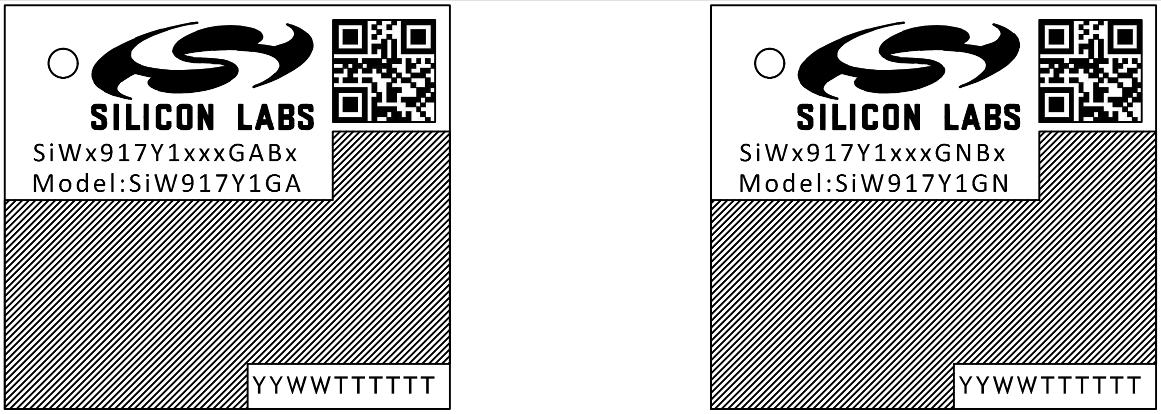


Figure 9.4. Module Marking Information

Mark Description

- SiWx917Y1xxxGABx/ SiWx917Y1xxxGNBx - Part number designation
- Model: SiW917Y1GA/ SiW917YGN - Model number designation
- QR Code: YYWWMMABCDE
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - MMABCDE – Silicon Labs unit code
- YYWWTTTTTT
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - TTTTTT – Manufacturing trace code. The first letter is the device re
- Certification marks such as the CE logo, UKCA, FCC and IC IDs, etc. will be engraved on the hatched-out area or printed on the back side of the modu according to regulatory body requirements.

Marking		Description
Part	SiWx917Y1xxxGABx/ SiWx917Y1xxxGNBx	Orderable Part Number (OPN) designation
Model	SiW917Y1GA/SiW917Y1GN	Model Name designation, respectively for parts with integral antenna and RF pin
QR Code	YYWWMMABCDE	YY – Last two digits of the assembly year WW – Two-digit workweek when the device was assembled MMABCDE – Silicon Labs unit code
Lot Code	YYWWTTTTTT	YY – Last two digits of the assembly year WW – Two-digit workweek when the device was assembled TTTTTT – Manufacturing trace code. The first letter is the device revision
Compliance Marks	CE	Certification-related information, such as the CE and Giteki compliance marks, or the FCC and IC IDs, is being engraved on the hatched-out area, and/or printed on the back side of the module (silkscreen), in accordance with the requirements by regulatory bodies.

9.5 Moisture Sensitivity Level

SiWG917 modules are rated MSL3 (Moisture Sensitivity Level 3). Reels are delivered in packing which conforms to MSL3 requirements.

10. Soldering Recommendations

It is recommended that final PCB assembly of the SiWG917 follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Note: General SMT application notes are provided in AN1223: LGA Manufacturing Guidance.

11. Tape and Reel

The SiWG917 modules are delivered to the customer in cut tape (100 pcs) or reel (700 pcs) packaging having the dimensions below. All dimensions are given in mm unless otherwise indicated.

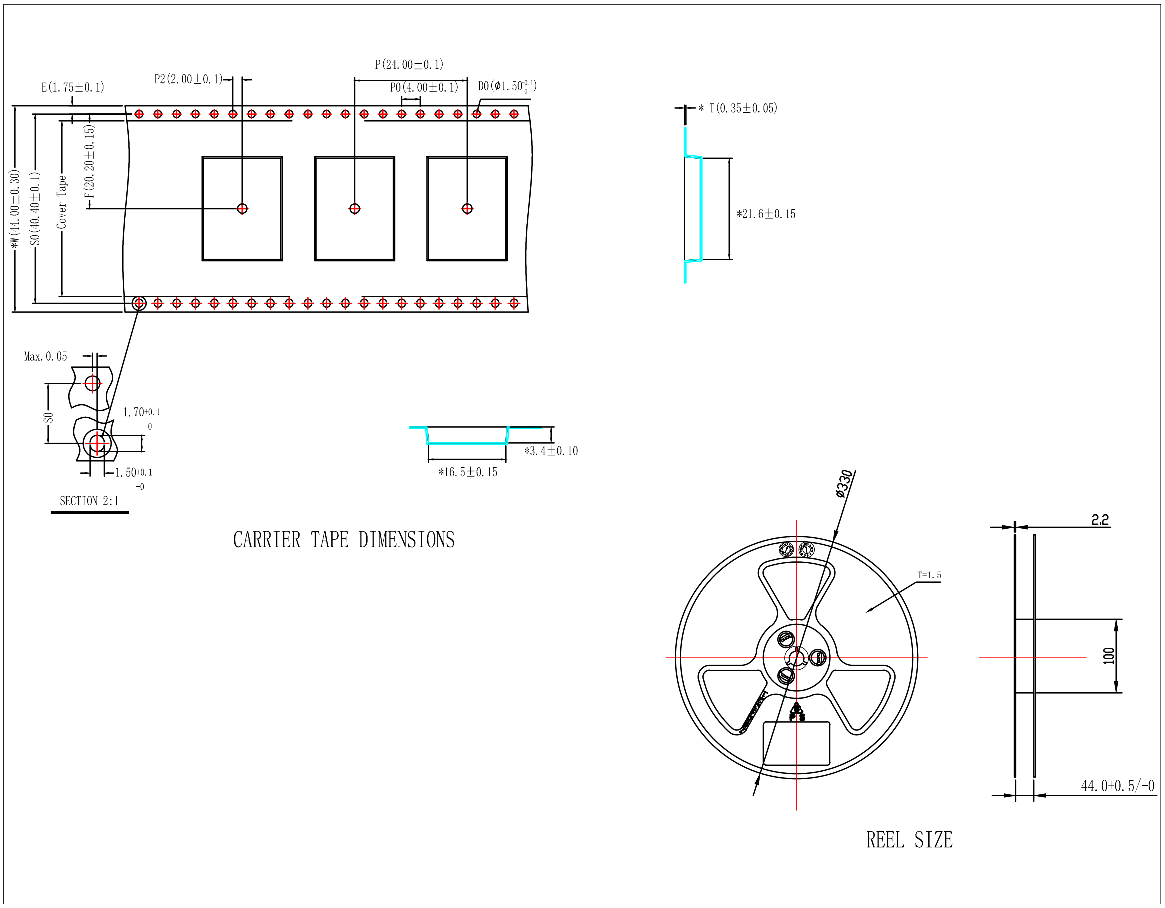


Figure 11.1. Carrier Tape Dimensions

12. Certifications

This section details the certification status of the SiW917Y1GA and SiW917Y1GN Connectivity Modules with regards to regional regulatory radio approvals. Where applicable, the status with the qualifications against the specifications of the supported global industrial wireless standards is given too.

The address of the legal manufacturer (technology owner) and certification applicant is:

SILICON LABS / SILICON LABORATORIES FINLAND OY
Alberga Business Park, Bertel Jungin aukio 3,
02600 Espoo, Finland

The SiW917Y1GA and SiW917Y1GN Connectivity Modules have brand name of "SILICON LABS".

"SILICON LABS" (and "Silicon Labs") is a trademark globally owned by the Silicon Laboratories Inc. corporation, and all branches and subsidiaries, including the above applicant, holds the right to use it.

12.1 Qualified Antennas

The SiW917Y1GA and SiW917Y1GN Connectivity Modules have been tested and certified for the use with respectively the built-in integral antenna and a reference external antenna attached to the module's RF pin denoted as RF_PORT. The intended antenna impedance is 50 Ω.

Performance characteristics for the built-in antenna are presented in 8.4 SiW917Y1GA Antenna Radiation and Efficiency. The details of the qualified external antenna(s) are summarized in Table 12.1 Qualified External Antenna(s) for the SiW917Y1GN Modules on page 175. The qualified external antenna(s) is(are) meant to be directly connected to the module's RF pin, with no active/non-linear component(s) along the RF path in between.

Table 12.1. Qualified External Antenna(s) for the SiW917Y1GN Modules

Manufacturer and Model	Type	Peak Gain	Impedance
TE Connectivity Ltd. (previously Linx Technologies Inc.), ANT-2.4-CW-CT-RPS	Connectorized Coaxial Dipole	+2.8 dBi	50 Ω

Any external antenna of the same general type and of equal or less peak directional gain compared to the one listed in the above table, and having similar in-band and out-of-band characteristics, can be used in the regulatory areas that have modular radio type approvals, such as USA and Canada, as long as spot-check testing of the host is performed to verify that no performance changes compromising compliance have been introduced. In the particular FCC case, to comply with e-CFR Title 47, Part 15, Subpart C, Section 15.203, the module integrator using an external antenna must ensure it has a unique connector or it is nondetachable.

When using instead an external antenna of a different type (such as a chip antenna, a host PCB trace antenna, or a patch) and/or having non-similar in-band and out-of-band characteristics, but still with a gain less than or equal to the maximum gain listed in the table above, in principle it can be added to the existing modular grant/certificate by means of a permissive change, for example with FCC and ISED. Typically, some radiated emission testing is demanded, but no modular or end-product re-certification is required. Please consult your certification house and/or a certification body and/or the module manufacturer for a confirmation of the correct procedures and for any authorization to perform a FCC's Change in ID and/or a ISED's Multiple Listing followed by the intended permissive changes.

On the other hand, products designed to be used with an external antenna having higher peak gain than the maximum gain listed in the table above are very likely to require full new end-product's radio type approvals, with certification IDs under the host manufacturer's ownership. Since the exact permissive change or registration or re-certification procedure is chosen on a case-by-case basis, consult your certification house and/or a certification body for understanding the correct approach based on your unique design.

In countries applying the ETSI standards, where manufacturers issue a self-Declaration of Conformity before placing their end-products in the market, like in the EU countries (and in the UK), the radiated emissions are always evaluated with the end-product and the external antenna type is not critical, but antennas with higher gain may violate some of the EIRP regulatory limits.

For Japan, where compliance testing is done conductively, the allowed external antennas are listed in the certificate and/or test report(s). Any other external antenna will have to be formally added to the list of approved antennas by the certificate holder: in this case, please reach out to the module manufacturer to discuss such addition, or consider certifying the end-product itself as an alternative.

12.2 CE and UKCA - EU and UK

The SiW917Y1GA and SiW917Y1GN modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the EU's Radio Equipment Directive (RED) (2014/53/EU) and of the UK's Radio Equipment Regulations (RER) (S.I. 2017/1206).

The modules are therefore entitled to carry the CE and UKCA compliance marks, while the respective formal Declarations of Conformity (DoCs) are available at the product web page, which is reachable starting from www.silabs.com.

Note that every final product integrating the SiW917Y1GA or the SiW917Y1GN Connectivity Module will need to go through full Safety and EMC assessments, for example in accordance with the ETSI 301 489-x applicable standards. In fact, Safety and EMC tests performed on a bare radio module are generally not supposed to provide confidence of Safety and EMC compliance of the final radio product as a whole.

Furthermore, it is ultimately the responsibility of the manufacturers to ensure the compliance of their complete final products also with respect to the RF performance. The specific product assembly is likely to have an impact on the RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, especially taking into account the gain of the external antenna if any, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI EN 300 328 standard.

OEMs must also consider the importance of applying the compliance mark(s) to a visible location on their final products, on top of the need to writing down and signing the legal manufacturer's Declaration of Conformity for the final product itself. More in general, module customers assume full responsibility with regards to learning the guidelines and meeting the requirements for the compliance in each region where their end-products are marketed.

12.3 FCC - USA

This device complies with FCC's e-CFR Title 47, Part 15, Subpart C, Section 15.247 (and related relevant parts of the ANSI C63.10 standard) when operating with the built-in integral antenna or with an external antenna type as discussed in chapter 11.1.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user’s authority to operate the equipment.

FCC RF Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying the RF exposure compliance.

This transmitter meets the Mobile requirements at a distance of 20 cm and above from the human body, in accordance to the limit(s) exposed in the RF Exposure Analysis. This transmitter also meets the Portable requirements at distances equal or above those being reported in Minimum Separation Distances for SAR Evaluation Exemption.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to Comply with FCC Regulations

This module has been tested for compliance to FCC Part 15.

OEM integrators are responsible for testing their end-product for any additional compliance requirements needed with this module installed (for example, digital device emissions, PC peripheral requirements, etc.)

Additionally, investigative measurements and spot-check testing (with all transmitters active, if other co-located radios than the module itself exist on the host), are strongly recommended in order to verify that the full system's compliance is maintained when the module is integrated, even with the module having a full modular approval, in accordance with the "Host Product Testing Guidance" in FCC's KDB 996369 D04 Module Integration Guide.

- **General Considerations**

  This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement, which is typically applicable to the final host. The final host will still need to be assessed for compliance to this portion of the rule requirements, if applicable.

- **Manual Information to the End User**

  The OEM integrator has to be aware not to provide information to the end-user regarding how to install or remove this RF module, or how to change RF related parameters, in the user’s manual of the final product which integrates this module.

  The end user manual shall include all required regulatory information/warnings as shown in this manual.

- **Host Manufacturer Responsibilities**

  Host manufacturers are ultimately responsible for the full compliance of their host system. The final product is supposed to be assessed against all the essential requirements of the FCC rules, such as FCC Part 15 Subpart B, before it can be placed on the US market. This includes re-assuring the compliance of the radio transmitter with the RF and EMF essential requirements of the FCC rules. The modular radio transmitter must not be incorporated into any other radio-equipped device or system without retesting for compliance as multi-radio and combined equipment.

For more details about integrating the Single Modular Transmitter, refer to the following FCC document:

- KDB 996369 D04 Module Integration Guide

For understanding better the process leading to obtaining a Full Modular Approval, see the following documents instead:

- KDB 996369 D01 Transmitter Module Equipment Authorization Guide
- KDB 996369 D02 Frequently Asked Questions and Answers about Modules

The two documents above give an insight of the FCC requirements from the module manufacturer's perspective, and will help to realize the need by the integrators to follow the integration instructions and design guidance, and to take into account for example the RF Exposure limitations, if any. Should a deviation occur, keep in mind the possible need to work with the manufacturer in order to proceed with a permissive change (following a *Change in ID*), in accordance with the FCC guidelines found in the following documents:

- KDB 178919 D01 Permissive Change Policy
- KDB 178919 D02 Permissive Change Frequently-Asked Questions

Separation

- To meet the SAR exemption for portable conditions, the minimum separation distances indicated in Minimum Separation Distances for SAR Evaluation Exemption must be maintained between the human body and the radiator (antenna) at all times.
- This transmitter module is tested in a standalone RF Exposure condition, and in case of any co-located radio transmitter being allowed to transmit simultaneously, or in case of portable use at closer distances from the human body than those allowing the exceptions rules to be applied, a separate additional SAR evaluation, or a reduction in the max output power or in the duty-cycle, might be required for the host, ultimately leading to a Class II Permissive Change, or more rarely to a new grant.
- **Important Note:** In the event that the conditions for the exemption cannot be met, the final product will likely have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the FCC authorization to remain valid, and a permissive change will have to be applied. The SAR evaluation (and/or reconfiguration) is in the responsibility of the end-product’s manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a *Change in ID* authorization by the module's original grant holder.

End Product Labeling

The SiW917Y1GA and SiW917Y1GN modules are labeled with their own FCC ID. In all those cases when the module's label is not visible, for example after the module becomes enclosed inside the end-product casing, or if the FCC ID is printed on the module's PCB silkscreen, then the outside of the device into which the module is installed must also have a label with a reference to the embedded module. In that case, the final product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQ-917AC"

or

"Contains FCC ID: QOQ-917AC"

Final note:

As long as all the conditions in this and all the above chapters are met, further RF testing of the transmitter will not be strictly required. However, still consider the good practice and the FCC strong recommendation to ensure the compliance of the host by spot-checking. Nevertheless, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements which might be mandatory with this module installed.

12.4 ISED - Canada

This radio transmitter (with IC: 5123A-917AC and PMN: *Bluetooth Low Energy and 802.11b/g/n/ax wireless radio module*) has been approved by *Innovation, Science and Economic Development Canada* (*ISED Canada*, formerly *Industry Canada*) to operate with the built-in integral antenna or with the external antenna type(s) listed in Qualified Antennas, having the maximum permissible gain indicated in the table. External antenna types not included in this list, or having a gain greater than the maximum gain listed, are strictly prohibited for use with this device.

This radio-equipped device complies with ISED's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference.
2. This device must accept any interference, including interference that may cause undesired operation of the device.

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The module meets the requirements for Mobile use cases when the minimum separation distance from the human body is 20 cm or greater, in accordance to the limit(s) exposed in the RF Exposure Analysis.

For Portable use cases, RF exposure or SAR evaluation is not required when the separation distances from the human body are equal or above those reported in Minimum Separation Distances for SAR Evaluation Exemption .

If the separation distance from the human body is less than the values stated in Minimum Separation Distances for SAR Evaluation Exemption, then the OEM integrator is responsible for evaluating the SAR with the end-product, or for the re-configuration of the radio module in the host in terms of lowering the max RF TX power and/or the duty-cycle. A permissive change would be required too, under the responsibility of the host manufacturer, following a *Multiple Listing* authorization by the module's original certificate holder.

OEM Responsibilities to comply with IC Regulations

The SiW917Y1GA and SiW917Y1GN modules have been certified for integration into products only by OEM integrators, under the following conditions:

- The module must be installed in such a way that the intended minimum separation distances are maintained between the radiator (antenna) and all persons at all times. Minimum Separation Distances for SAR Evaluation Exemption indicates the distances in accordance to the use cases.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

Important Note: In the event that the above conditions cannot be met, the final product will have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the ISED authorization to remain valid; a permissive change will have to be applied too**.** The RF Exposure evaluation (SAR, or possibly a re-configuration) is in the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a *Multiple Listing* authorization by the module's original certificate holder.

End Product Labeling

The SiW917Y1GA and SiW917Y1GN modules are labeled with their own IC ID. In all those cases when the module's label is not visible, for example after the module becomes enclosed inside the end-product casing, or if the IC ID is printed on the module's PCB silkscreen, then the outside of the device into which the module is installed must also have a label with a reference to the embedded module. In that case, the final product must be labeled in a visible area with the following:

“**Contains Transmitter Module IC: 5123A-917AC**”

or

“**Contains IC: 5123A-917AC**"

Final notes:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end-product.

As long as all the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.)

ISED (Français)

Le présent émetteur radio (IC: 5123A-917AC, PMN: *Bluetooth Low Energy and 802.11b/g/n/ax wireless radio module*) a été approuvé par *Innovation, Sciences et Développement Économique Canada* (*ISED Canada*, anciennement *Industrie Canada*) pour fonctionner avec l'antenne intégrée et le ou les types d'antenne énumérés à la section Qualified Antennas, avec le gain maximal admissible indiqué. Les types d'antenne non inclus dans cette liste, ayant un gainsupérieur au gain maximal indiqué, sont strictement interdits d'utilisation avec cet appareil.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Déclaration d'exposition RF

Les exceptions aux limites de l'évaluation SAR sont données dans le numéro 5 de la publication RSS-102.

Le module répond aux exigences pour les cas d'utilisation Mobile lorsque la distance minimale de séparation du corps humain est de 20 cm ou plus, conformément à la (aux) limite(s) exposée(s) dans l'analyse de l'exposition RF.

Pour les cas d'utilisation portables, l'évaluation de l'exposition RF ou l'évaluation SAR n'est pas requise lorsque les distances de séparation du corps humain sont égales ou supérieures à celles indiquées dans Minimum Separation Distances for SAR Evaluation Exemption.

Si la distance de séparation du corps humain est inférieure aux valeurs indiquées dans Minimum Separation Distances for SAR Evaluation Exemption, l'intégrateur OEM est responsable de l'évaluation du SAR avec le produit final, ou de la reconfiguration du module radio dans l'hôte en termes de réduction de la puissance RF TX maximale et/ou du rapport cyclique. Une modification permissive serait également nécessaire, sous la responsabilité du fabricant de l'hôte, suite à une autorisation de cotation multiple par le titulaire du certificat du module d'origine.

Responsabilités du fabricant de se conformer à la réglementation IC

Le module a été certifié pour l'intégration dans les produits uniquement par les intégrateurs OEM dans les conditions suivantes:

- Le module émetteur doit être installée de manière à maintenir une distance de séparation minimale, comme indiqué ci-dessus, entre le radiateur (antenne) et toutes les personnes à tout moment.
- Le module émetteur ne doit pas être localisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

Remarque Importante: au cas où ces conditions ne pourraient pas être remplies, le produit final devra être soumis à des tests supplémentaires pour évaluer l'exposition RF, ou passer par une reconfiguration de la puissance de sortie maximale et/ou du rapport cyclique, afin que l'autorisation ISED reste valable; une modification permissive devra également être appliqué. L'évaluation de l'exposition aux radiofréquences (SAR, ou éventuellement une reconfiguration) est sous la responsabilité du fabricant du produit final, ainsi que le changement permissif qui peut être effectué avec l'aide de l'organisme de certification des télécommunications du client, après autorisation de cotation multiple par le titulaire de la certification du module.

Étiquetage des produits finis

Les modules SiW917Y1GA / SiW917Y1GN sont étiquetés avec leur propre IC ID. Dans tous ces cas, si l'ID IC n'est pas visible après l'installation du module à l'intérieur d'un autre appareil, alors l'extérieur de l'appareil dans lequel le module est installé doit également afficher une étiquette faisant référence au module inclus. Dans ce cas, le produit final doit être étiqueté dans une zone visible avec les éléments suivants:

"**Contient le module transmetteur IC: 5123A-917AC**"

ou

"**Contient IC: 5123A-917AC**"

Remarques finales:

L'intégrateur OEM doit être conscient de ne pas fournir à l'utilisateur final d'informations sur la procédure d'installation ou de retrait de ce module RF ni sur la modification des paramètres liés à la RF dans le manuel d'utilisation du produit final.

Tant que toutes les conditions ci-dessus sont remplies, aucun test supplémentaire de l'émetteur ne sera nécessaire. Toutefois, l'intégrateur OEM reste responsable de l'essai de son produit final pour déterminer les exigences de conformité supplémentaires requises avec ce module installé (par exemple, émissions d'appareils numériques, exigences relatives aux périphériques PC, etc.)

12.5 MIC - Japan

The SiW917Y1GA and SiW917Y1GN modules are certified in Japan with following certification number:

- 203-JN1379

While the module manufacturer takes all reasonable steps to prevent non-compliant operation, it is still the end-product manufacturer's responsibility to ensure that a module is configured to meet the compliance requirements, for example in relation to the maximum allowed RF TX power. When applicable, refer to the SDK documentation and/or API reference manuals and/or integration and certification guides, to learn how to configure (limit) the maximum RF TX power for ensuring the compliance of the end-product during regular operation, if need be. Refer as well to the power setting table(s) and measurements in the test report(s) in order to realize the maximum output power levels allowed for the regulatory compliance in Japan.

Manufacturers integrating a certified radio module into their host equipment are supposed to make the Technical Conformity Mark and the certification number visible on the outside of their device. This combination of mark and number, and their relative placement, is depicted in the Figure 12.1 Example of "Giteki" Mark with Placeholder for Actual Certification Number on page 181 below, and depending on the overall size it might also appear among the top shield markings of the radio module. The Technical Conformity Mark and the certification number must be placed close to the text in the Japanese language which is provided below. This requirement in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio-equipped device which is approved for use in Japan.

Certification text to be placed on the outside surface of the host equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”

The "Giteki" Technical Conformity Mark, together with the actual module's certification number, as shown in the following example figures, must be affixed to an easily noticeable section of the specified radio-enabled host equipment. Notice that such section may be required to contain additional information if the end-device embedding the module is also subject to a Telecom approval.

The manufacturer of the final product is also responsible to provide a Japanese language version of the User Manual and/or Installation Instructions as a companion document coming with the final product when placed on the market in Japan. Such a document will have to mention the integrated radio component and the related certification information.

Figure 12.1. Example of "Giteki" Mark with Placeholder for Actual Certification Number

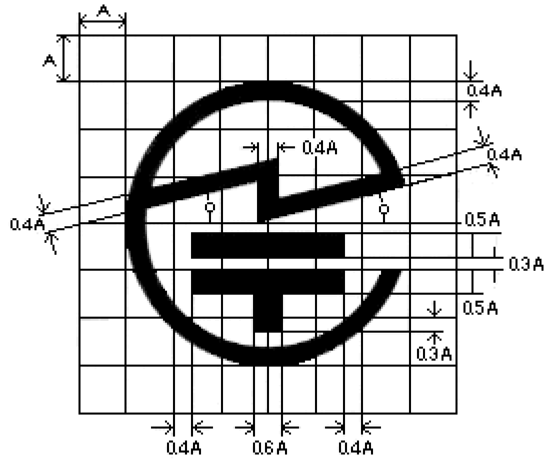


Figure 12.2. Detail of "Giteki" Compliance Mark

12.6 KC - South Korea

The SiW917Y1GA and SiW917Y1GN modules have a RF registration for import and use in South Korea.

Registration number is KC ID: R-R-BGT-917AC

These modules are meant to be integrated into end-products, which then become exempted from doing the RF emission testing, as long as the recommended design guidance is followed, and as long as, where applicable, the approved external antennas are used and any additional transmit power backoff is implemented in accordance to the measurements and configurations seen in the formal test report(s).

EMC testing and any other relevant test applicable to the end-product as a whole, plus appropriate labeling of the end-product, might still be required for the full regulatory compliance in the country.

12.7 NCC - Taiwan

The SiW917Y1GA and SiW917Y1GN modules are certified in Taiwan with NCC certification numbers as follows:

SiW917Y1GA 和 SiW917Y1GN 模組已在台灣獲得認證，NCC 認證編號如下：

SiW917Y1GA: CCAL25Y10200T5

SiW917Y1GN: CCAL25Y10201T7

Manufacturers are required to mark their end-products with the following sentence: *"This product contains a radio frequency module with certification number CCAL25Y1020xTx"*, where CCAL25Y1020xTx corresponds to the above-listed certification number of the embedded module.

系統製造商應在平台上放置以下聲明：“本產品包含認證編號為 CCAL25Y1020xTx 的無線電模組”，其中 CCAL25Y1020xTx 對應於上面列出的嵌入式模組的認證編號。

Note: The outer packaging of the final product must also be marked with the NCC conformity mark by the manufacturer.

注意：最終產品的外包裝也必須由製造商打上 NCC 合格標誌。

Additionally, the final product will have to be listed in the NCC database of approved radio-equipped devices. Consequently, the end manufacturer is also supposed to contact a certification body or the certification house that originally released the modular approval and apply for the registration of their platform under the applicable certification number above. Fees might apply, and an authorization by the module manufacturer might be required too.

此外，最終產品必須列入 NCC 的核准無線電設備資料庫中。因此，最終製造商也應聯繫最初協助頒發模組化核准的認證機構或認證公司，並申請在上述適用的認證編號下註冊其平台。可能需要列出費用和模組製造商的授權。

NCC Statement
- For low-power radio frequency equipment that has been certified, companies, firms, or users are not allowed to change the frequency, increase the power, or change the characteristics and functions of the original design without further NCC approval. - The use of low-power radio frequency equipment shall not affect flight safety and interfere with legal communications. - If interference is found, it shall be immediately stopped, and the equipment can be brought back into use only after it has been improved, so that interference is found no more. - The aforementioned legal communication refers to radio communications operating in accordance with the provisions of the Telecommunications Management Act. - Low-power radio frequency equipment must withstand interference from legitimate communications or radiating electrical equipment for industrial, scientific, and medical applications.
NCC 警語
取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。 低功率射頻器材之使用不得影響飛航安全及干擾合法通信。 經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。 前述合法通信，指依電信管理法規定作業之無線電通信。 低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

12.8 SRRC - China

The SiW917Y1GA module has a full modular radio type approval for re-use by the OEM integrators:

Certificate No.: 2025-9477

CMIIT ID: 25J99MY6Q954

The SiW917Y1GN module has a limited modular radio type approval for re-use by the OEM integrators:

Certificate No.: 2025-9493

CMIIT ID: 25J99MY60583(M)

Note for modules with a full modular approval: every end-product integrating the module must be labeled with the following statement (alternatively, in case of lack of space, the statement will have to go to the end-product's user manual):

本设备包含一个无线电发射器模块，型号核准代码为：CMIIT ID：25J99MY6Q954

(Translation: *"This equipment contains a radio transmitter module with type approval code: CMIIT ID: 25J99MY6Q954"*)

SRRC – 中国

SiW917Y1GA 模塊具有完整的模塊化認證，可供 OEM 集成商重複使用：

认证编号：2025-9477

CMIIT ID : 25J99MY6Q954

SiW917Y1GN 模塊具有有限的模塊化認證，可供 OEM 集成商重複使用：

认证编号：2025-9493

CMIIT ID : 25J99MY60583(M)

具有完全模塊化批准的模塊注意事項：以下聲明必須出現在嵌入模塊的最終產品的標籤和/或用戶手冊中：

本设备包含一个无线电发射器模块，型号核准代码为：CMIIT ID：25J99MY6Q954

12.9 ACMA - Australia

The SiW917Y1GA and SiW917Y1GN modules are in compliance with the Australian RCM requirements, and are labelled with the RCM Compliance Mark. The formal Declaration of Conformity (DoC) is available at www.silabs.com. With the DoC and RCM compliance mark, the modules are also covered for the use in New Zealand (RSM).

12.10 RF Exposure and Proximity to Human Body

When using the SiW917Y1GA and SiW917Y1GN modules in an application where the radio-equipped end-product is located close to the human body, the human RF Exposure must be taken into account. FCC, ISED, and CE/UKCA all have different standards and rules for evaluating the RF Exposure. In particular, each regulator has different requirements when it comes to the exemption from having to perform RF Exposure evaluation and/or SAR (Specific Absorption Rate) measurements, and the minimum separation distances between the module's antenna and the human body varies accordingly. The properties of the SiW917Y1GA and SiW917Y1GN modules allow the minimum separation distances detailed in Table 12.2 Minimum Separation Distances for SAR Evaluation Exemption on page 185 for the SAR measurement exemption in the Portable use cases (less than 20 cm from the human body). These modules are approved for the Mobile use case (more than 20 cm) without any need for RF Exposure evaluation.

Table 12.2. Minimum Separation Distances for SAR Evaluation Exemption

Certification	SiW917Y1GA	SiW917Y1GN
FCC	BLE: 22 mm 802.11b/g/n/ax: 37 mm All protocols in use (overall): 37 mm	BLE: 23 mm 802.11b/g/n/ax: 39 mm All protocols in use (overall): 39 mm
ISED	BLE: 30 mm 802.11b/g/n/ax: 45 mm All protocols in use (overall): 45 mm	BLE: 30 mm 802.11b/g/n/ax: 45 mm All protocols in use (overall): 45 mm
CE / UKCA	In general, the RF exposure should always be evaluated with the end-product when transmitting with EIRP power levels higher than 20 mW (13 dBm) while operating at distances closer than 20 cm from the human body. With the SiW917Y1GA and SiW917Y1GN modules, this is the case only with the 802.11b/g/n/ax protocols transmitting at full power. In all other cases, modules comply with the requirements of the relevant standard(s).	

The exemption minimum distances above, calculated for reference in the full output power use-case, are based on the rules in force at the time of originally writing this data sheet. Even though changes happen rarely, always ensure to apply the rules in force at the time of placing the end-product into the market.

In the cases of FCC and ISED, it is allowed to use a module at its max RF TX power in an end-product where the typical separation distance from the human body is smaller than mentioned above, but it requires evaluating the RF Exposure in the final assembly and applying for a *Class 2 Permissive Change* to the FCC and ISED approvals of the module. In order to proceed with the permissive changes, first the module manufacturer should be asked for an authorization to do an FCC's *Change in ID* and an ISED's *Multiple Listing*; then, the new Portable condition will be added to the new parallel grants owned by the end-product manufacturer, for extending the approvals to their unique host under their unique configuration and mode of use.

For those end-products where the embedded module is configured to implement only a single wireless protocol which would allow for the exemption at a shorter distance than the overall minimum distance, there would be no need the evaluate the RF Exposure at such a shorter distance and above. However, a permissive change would still be needed as a mean to notify the FCC / ISED of the reason why in the field the module is allowed to operate at a shorter distance than the overall minimum distance in Table 12.2 Minimum Separation Distances for SAR Evaluation Exemption on page 185.

An example of another use case where the module could operate at a shorter distance than in Table 12.2 Minimum Separation Distances for SAR Evaluation Exemption on page 185, without having to do the RF Exposure evaluation / SAR measurement, is when the power or the duty-cycle is reduced during normal operation. However, the new minimum distance for the exemption should be re-calculated, and still a permissive change would be needed to notify the regulators of the new conditions.

For the CE/UKCA compliance, RF Exposure must be considered and evaluated by the OEM in all cases (if any) when the end-product is transmitting at higher power level than indicated in Table 12.2 Minimum Separation Distances for SAR Evaluation Exemption on page 185.

Note: Placing the module in touch or very close to the human body will have a negative impact on the efficiency of the antenna thus a reduced range is to be expected.

12.11 Bluetooth Qualification

The SiW917Y1GA and SiW917Y1GN modules have the following Qualified Products with corresponding Qualified Design Identification (QDID) based on the Bluetooth Core Specification 5.4:

1. **QDID 230044**
    - This Core Layer Design is for the Low Energy RF-PHY Radio interface.
2. **QDID 226688**
    - This Core Layer Design is for Host Controller Interface and Low Energy Link Layer.
3. **QDID 227553**
    - This Core-Controller Configuration Design combines the above QDID 230044 and QDID 226688. It encompasses the Low Energy RF-PHY Radio interface and the Low Energy Link Layer, plus the Host Controller Interface, for easier integration when doing a Core-Complete Configuration Design in order to make a Product.

13. Documentation and Support

Silicon Labs offers a set of documents which provide further information required for evaluating, and developing products and applications using SiWG917. These documents will be available on the Silicon Labs website. The documents include information related to Software releases, Evaluation Kits, User Guides, Programming Reference Manuals, Application Notes, and others.

For further assistance, you can contact Silicon Labs Technical Support here.

Resource Location

SiWG917 Document Library : https://docs.silabs.com/wiseconnect/latest/wiseconnect-developing-with-wiseconnect-sdk/

Technical Support : http://www.silabs.com/support/

14. Revision History

Revision 1.1

August, 2025

- Updated the Block Diagram on the front page.
- The following are the updates in the 1. Feature List:
  - Updated PSRAM in-package memory size.
  - Removed RTC, BOD from list of ULP peripherals.
  - Changed minimum active current from 32 to 40.4 µA/MHz @ 20 MHz in low-power mode.
  - Changed minimum active current from 50 to 70.5 µA/MHz @ 20 MHz in high-performance mode.
- The following are the updates in the 2. Ordering Information:
  - AI/ML Matrix Vector Processor (MVP) features are available from WiseConnect SDK 3.5.0. Removed Note 2.
- The following are the updates in 5. System Overview:
  - Removed section "Memory Protection Unit".
  - 32-bit configuration timer option for State Configurable Timer (SCT) is not supported.
  - Removed IR peripheral address mapping in Table 5.3 ULP MCU APB Peripherals Address Mapping on page 20.
  - Modified Figure 5.2 Power States on page 26 and added a Note.
  - Updated Table 5.9 List of Wakeup Sources in Different States on page 29.
  - 5.6.1.8 Secure Digital I/O (SDIO) Secondary Interface: Updated content from " Supports up to five functions" to " Supports only function 1".
  - Corrected the table header from Flash Density (in Mbit) to 'PSRAM Density (in Mbit)' in Table 5.12 PSRAM on page 40.
  - Renamed "First-party DMA ports" to "Memory access ports" in 5.6.1.25 MVP.
- The following are the updates in 7. Electrical Specifications:
  - Note added: ADC performance not guaranteed below -20 °C in 7.5.4 Analog to Digital Converter .
  - ADC gain error (typical) changed to 2 % (removed min and max specs) in 7.5.4 Analog to Digital Converter .
  - ADC offset error (typical) changed to 10 mV (removed min and max specs) in 7.5.4 Analog to Digital Converter .
  - Note added: DAC performance not guaranteed below -20 °C in 7.5.5 Digital to Analog Converter.
- The following are the updates in 8. Reference Schematics, BOM, and Layout Guidelines.
  - 8.1.3 GPIO Connection and 8.2.3 GPIO Connection: Added resistors R12, R13, R14.
  - In Figure 8.3 GPIO Connection on page 143 and Figure 8.19 GPIO Connection on page 152. Added optional pull-up resistors R12-R14 which are required GPIOs 49:51 with Module OPNs SiWG917Y121MGNBA and SiWG917Y121MGABA.
- The following are the updates in 9.3 PCB Landing Pattern:
  - Updated Figure 9.3 PCB Landing Pattern on page 170 with additional keep-out area.
- KC (South Korea), 12.6 KC - South Koreaand SRRC (China), 12.8 SRRC - China, certifications achieved.

Revision 1.0

July, 2025

- Updated Cover page
- Updated Feature List
- Updated 3. Applications
- Updated the following in 4. Block Diagrams
  - Figure 4.3 SiWG917 SoC Software Architecture on page 13
- Updated the following in 5. System Overview
  - 5.5.1 Highlights
  - 5.5.2 Power Domains
  - 5.5.4.1 PS4 in 5.5.4 Power States
  - 5.5.6 Wakeup Sources
  - 5.6.1.5 Motor Control PWM (MCPWM) in 5.6.1 Digital Peripherals and Interfaces
  - 5.6.1.20 FLASH and PSRAM Supply Connections in 5.6.1 Digital Peripherals and Interfaces
  - Removed section "Capacitive Touch" in 5.6.2 Analog Peripherals and Interfaces
  - 5.6.2.1 Analog to Digital Converter (ADC) in 5.6.2 Analog Peripherals and Interfaces
  - 5.6.2.2 Digital to Analog Converter (DAC) in 5.6.2 Analog Peripherals and Interfaces
  - 5.7 Bootloader
  - 5.8.1 Security Features in 5.8 Security
  - Heading updated from Security Bootup to 5.8.2 Secure Boot
  - Heading updated from Security XiP to 5.8.3 Encrypted XiP
  - 5.8.5 Secure Zone
  - 5.8.6 In-System Programming (ISP)
  - 5.13.1 Security
  - 5.15 Wireless Subsystem Memory
- Updated the following in 6. Pinout and Pin Description
  - 6.2.3 Peripheral Interfaces
  - 6.3.1 SoC GPIO Pin Multiplexing
  - 6.3.4 Analog Functions
  - 6.4 Valid GPIO Sets for Peripherals
  - 6.5.2 Analog Functions in 6.5 Functional Description
- Updated the following in 7. Electrical Specifications:
  - 7.3.5 Thermal Characteristics
  - 7.4.1 Clock Specifications
  - 7.4.1.2 High-Frequency Crystal (HFXO)
  - 7.4.4 GPIO Pins
  - 7.6 RF Characteristics
  - 7.7 Typical Current Consumption
  - 7.3.1 RESET_N Pin and POC_IN Pins
  - 7.3.2 Power On Control (POC) and Reset
  - 7.3.3 Blackout Monitor
  - 7.3.6 Digital I/O Signals
  - 7.3.6.1 Open-Drain I2C Pins
- Updated the following in 8. Reference Schematics, BOM, and Layout Guidelines
  - 8.1 SiW917Y1GN Schematics for Parts with RF Pin
  - 8.2 SiW917Y1GA Schematics for Parts with Integral Antenna
  - 8.3 Layout Guidelines
  - 8.4 SiW917Y1GA Antenna Radiation and Efficiency
- Updated the following in 9. Package Specifications
  - 9.1 Dimensions
- Updated 11. Tape and Reel

Revision 0.7

November, 2024

- Updated Cover page
- Updated Feature List
- Added the following sections:
  - 5.2.1.1 Flash Architecture
  - 5.2.1.2 SRAM Memory Sharing between Cortex M4 and Network Wireless Processor
  - 5.3 Advanced Peripheral Bus (APB)
  - 5.4 Interconnect
- Removed IR Decoder
- Updated Figure 5.2 Power States on page 26
- Updated 5.6.1 Digital Peripherals and Interfaces
- Updated Table 6.2 Chip Packages - RF and Control Interfaces on page 58
- Updated Table 6.4 Chip Packages - Peripheral Interfaces on page 60
- Updated 6.3 GPIO Pin Multiplexing and reformatted subsection tables.
- Updated 6.4 Valid GPIO Sets for Peripherals
- Updated 6.5.1 Digital Functions
- Updated 6.5.2 Analog Functions
- Updated the following Electrical Specifications:
  - 7.1 Absolute Maximum Ratings
  - 7.2 Recommended Operating Conditions
  - Added 7.3.5 Thermal Characteristics
  - 7.3.1 RESET_N Pin and POC_IN Pins
  - 7.3.2 Power On Control (POC) and Reset
  - 7.3.3 Blackout Monitor
  - 7.3.6 Digital I/O Signals
  - 7.3.6.1 Open-Drain I2C Pins
  - 7.4.2 SDIO 2.0 Secondary
  - 7.4.3 HSPI Secondary
  - Removed UART
  - 7.4.4 GPIO Pins
  - 7.4.5 In-Package Flash Memory
  - 7.4.6 QSPI
  - 7.4.7 PSRAM
  - 7.4.8 I2C
  - 7.4.9 I2S/PCM Primary and Secondary
  - 7.4.10 ULP I2S/PCM Primary and Secondary
  - 7.4.11 SSI Primary/Secondary
  - 7.4.12 ULP SSI Primary
  - Removed SGPIO/MC-PWM/QEI/SCT Timer/SIO Interfaces and USART
  - 7.4.13 GSPI Primary
  - 7.4.14 Cortex-M4 JTAG
  - 7.4.15 Cortex-M4 Trace
  - 7.5 Analog Peripherals
  - 7.5.4 Analog to Digital Converter
  - 7.5.5 Digital to Analog Converter
  - 7.5.6 Op-Amp
  - 7.5.7 Temperature Sensor
- Added Note to 8.4.2 Proximity to Human Body

Revision 0.52

October, 2024

- Updated Notes in 1. Feature List
- Updated 2. Ordering Information
- Reformatted all the tables in Section
- Updated Section 7.6 RF Characteristics
- Updated Table 12.2 Minimum Separation Distances for SAR Evaluation Exemption on page 185
- Updated 12.11 Bluetooth Qualification

Revision 0.5

June, 2024

- Updated Features List
- Update Block Diagrams
- Updated System Overview
- Updated Pin Definitions
- Updated Electrical Specifications
- Updated Reference Schematics, BOM and Layout Guidelines
- Updated Certifications

Revision 0.4

April, 2024

NDA release and full update from previous version.

Revision 0.1

August, 2023

Preliminary version.

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SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

www.silabs.com