8-bit MCU Family
C8051F93x/92x Errata History

This document contains the errata history for C8051F93x/92x devices.

For errata on latest revision, please refer to the errata for the device. The device data sheet explains how to identify chip revision, either from package marking or electronically.

Errata history effective date: January 12th, 2016.

1. Errata Summary

Table 1.1. Errata Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Fixed Revision
1	OSC_E101	Maximum Clock Speed	No	B	C
2	CUR_E101	Increased Device Leakage for Supply Voltage Above 3.0 V	No	B	C
3	RTC_E101	SmaRTClock Capture Interferes with Auto Reset Function	Yes	B	C
4	DCDC_E101	SYNC Bit Does Not Always Provide Best SNR Performance	Yes	B	C
5	PWR_E102	Entry into Debug Mode Upon Wakeup from Sleep	No	C	D
6	CUR_E102	Increased Supply Current in One-Cell Mode for VBAT < 0.9 V and VDD/DC+ > 2.7 V	Yes	C	D
7	DBG_E101	Development Tool Update to Support Run/Stop Function in Sleep and Suspend Modes	No	C	D
8	POR_E101	POR Threshold Calibration Value	No	C	D
9	PWR_E104	System Clock Setting upon Entry into Suspend or Sleep Mode	Yes	All	E

2. Detailed Errata Descriptions

2.1 OSC_E101 – Maximum Clock Speed

Description of Errata
A timing path which does not allow the device to operate at 25 MHz under all specified operating conditions has been identified.
Affected Conditions / Impacts
The following restrictions regarding the system clock frequency should be followed: • If the 24.5 MHz Precision Oscillator is selected as the system clock source, the device may be operated in temperatures up to 50 °C. For operation at higher temperatures, the global system clock divider should be set to the divide by 2 setting. • If the External Oscillator is selected as the system clock source, the maximum system clock frequency is 22 MHz when the duty cycle is between 45 % and 55 %. • There are no restrictions when using the Low Power Oscillator or the smaRTClock oscillator as the system clock source.
Workaround
There is no workaround for this issue.
Resolution
Fixed in revision C and later.

2.2 CUR_E101 – Increased Device Leakage for Supply Voltage Above 3.0 V

Description of Errata
An incorrectly wired device that causes increased leakage at supply voltages above 3.0 V has been identified.
Affected Conditions / Impacts
The measured supply current in sleep mode increases at supply voltages above 3.0 V.
Workaround
There is no workaround for this issue.
Resolution
Fixed in revision C and later.

2.3 RTC_E101 – SmaRTClock Capture Interferes with Auto Reset Function

Description of Errata
Capture of the smaRTClock timer interferes with the auto reset function.
Affected Conditions / Impacts
The capture and auto reset functions of the smaRTClock timer cannot be used simultaneously.
Workaround
Use the capture function when auto reset is disabled, or vice versa.
Resolution
Fixed in revision C and later.

2.4 DCDC_E101 – SYNC Bit Does Not Always Provide Best SNR Performance

Description of Errata
Under some operating conditions, the SYNC bit in the DC0CN register does not provide the best SNR performance for the 10-bit SAR ADC.
Affected Conditions / Impacts
When the device is powered from the dc-dc converter, setting the SYNC bit will synchronize the clocking of the ADC to that of the dc-dc converter. On revision B devices, only the ADC tracking period is synchronized with the dc-dc converter and under some operating conditions, the ADC SNR can still be degraded by dc-dc switching activity.
Workaround
For best ADC SNR performance with revision B devices, do not set the SYNC bit in the dc-dc converter.
Resolution
Fixed in revision C and later. For revision C and later, setting the SYNC bit will synchronize both the tracking and conversion periods of the ADC to the dc-dc converter clock.

2.5 PWR_E102 – Entry into Debug Mode Upon Wakeup from Sleep

Description of Errata
A certain percentage of devices are exhibiting a behavior which causes the MCU to enter a debug state upon wakeup from sleep mode.
Affected Conditions / Impacts
Devices exhibiting this behavior may stop executing code or may output internal digital signals onto GPIO pins upon wakeup from sleep mode.
Workaround
There is currently no workaround for this issue.
Resolution
Revision C production test has been updated to screen for devices having a high risk of exhibiting this behavior. Fixed in revision D and later.

2.6 CUR_E102 – Increased Supply Current in One-Cell Mode for VBAT < 0.9 V and VDD/DC+ > 2.7 V

Description of Errata
In one-cell mode, if the VDD/DC+ supply voltage (dc-dc converter output) is greater than 2.7 V and the VBAT supply voltage (dc-dc converter input) is less than 0.9 V, the device supply current may reach an increased level until power is cycled.
Affected Conditions / Impacts
If powered by a battery, the battery may be discharged at a faster rate as soon as its voltage drops below 0.9 V.
Workaround
Monitor the VBAT supply voltage and place the device in a low power state before the battery voltage drops below 0.9 V if the dc-dc converter is programmed to an output voltage greater than 2.7 V.
Resolution
Fixed in revision D and later.

2.7 DBG_E101 – Development Tool Update to Support Run/Stop Function in Sleep and Suspend Modes

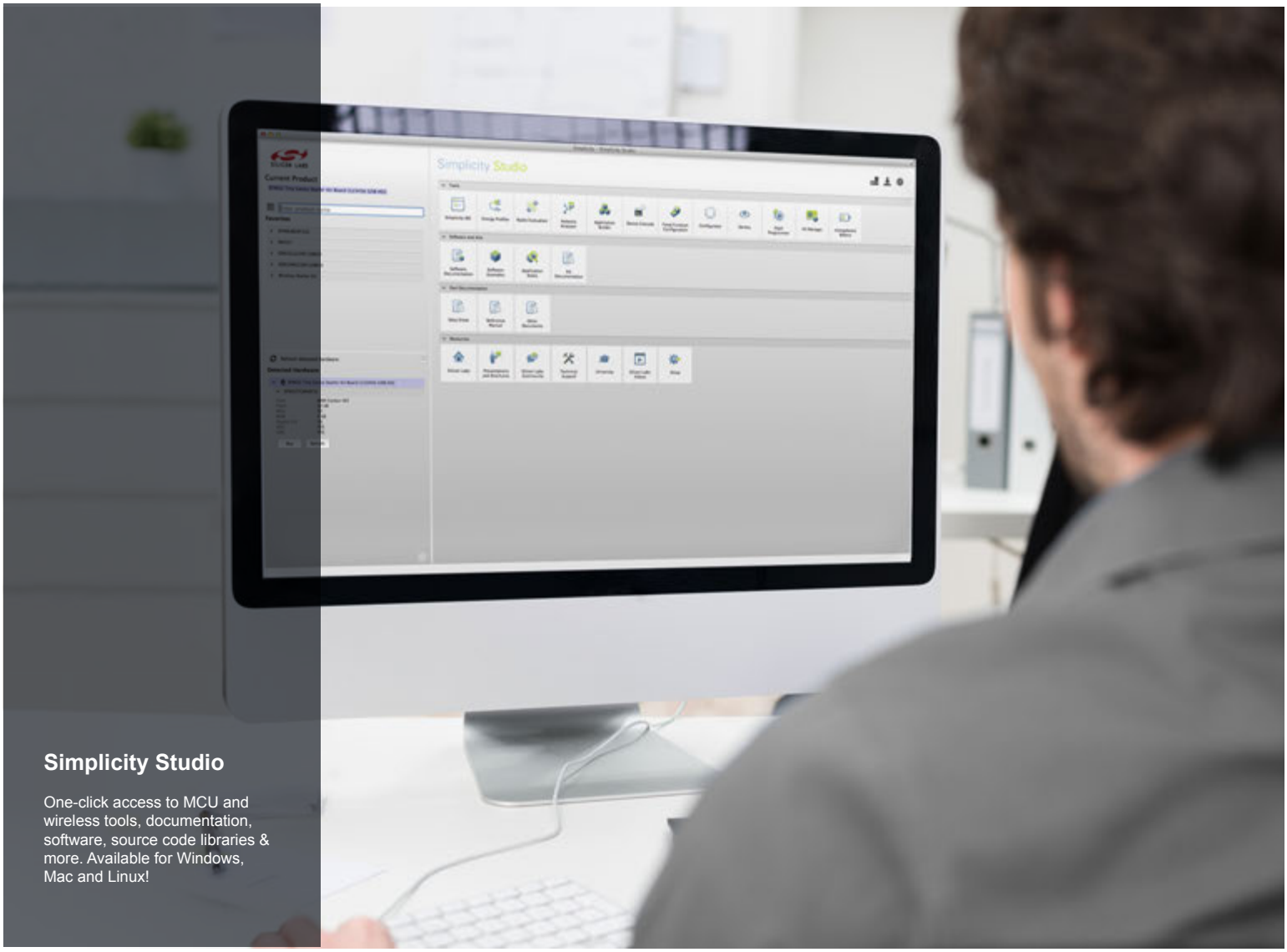
Description of Errata
On revision D devices, a development tool update is required to support Run/Stop functionality while the MCU is in sleep or suspend mode.
Affected Conditions / Impacts
Without the development tool update, the connection with the IDE/debugger will be disconnected if the user attempts to stop the MCU while it is in sleep or suspend mode.
Workaround
There is currently no workaround for this issue.
Resolution
When using revision D and later production silicon the following development tool revisions are required to enable full debug capability: • Silicon Labs IDE – Revision 3.41 or later • Keil µVision Driver – Revision 2.81 or later • Flash Programming Utilities – Revision 3.11 or later • Production Programming Utility – Revision 1.41 or later

2.8 POR_E101 – POR Threshold Calibration Value

Description of Errata
On some revision C devices, the POR threshold was calibrated to a value higher than the datasheet specification.
Affected Conditions / Impacts
The device may enter the reset state at a voltage higher than the voltage specified in the datasheet.
Workaround
There is currently no workaround for this issue.
Resolution
Fixed in revision D and later.

2.9 PWR_E104 – System Clock Setting upon Entry into Suspend or Sleep Mode

Description of Errata
Due to a clock synchronization issue inside the power management unit, if a wakeup event occurs during the same clock cycle that places the device into sleep or suspend mode, then the device may partially enter the low power mode and remain in this state until the next power-on reset. The supply current in this state is approximately 2 mA.
Affected Conditions / Impacts
This behavior may cause the device to become unresponsive to all wake-up sources and to the reset pin. It can only be recovered with a power-on reset.
Workaround
Since the power management unit is clocked from the low power oscillator, setting the system clock to low power oscillator divided by 2 before entering suspend or sleep mode will ensure that the clock synchronization issue inside the power management unit is not exercised and that the device will be able to safely enter and exit the low power state. The CLKRDY bit (CLKSEL.7) should be polled after changing the clock divide setting to ensure that the divide by 2 setting is applied to the system clock before allowing the device to enter the low power mode.
Resolution
Fixed in revision E and later.



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