



EFM8 Sleepy Bee Family

EFM8SB2 Errata



This document contains information on the errata of revision A of EFM8SB2.

For errata on older revisions, please refer to the errata history for the device. The device data sheet explains how to identify chip revision, either from package marking or electronically.

Errata effective date: August 22nd, 2016.

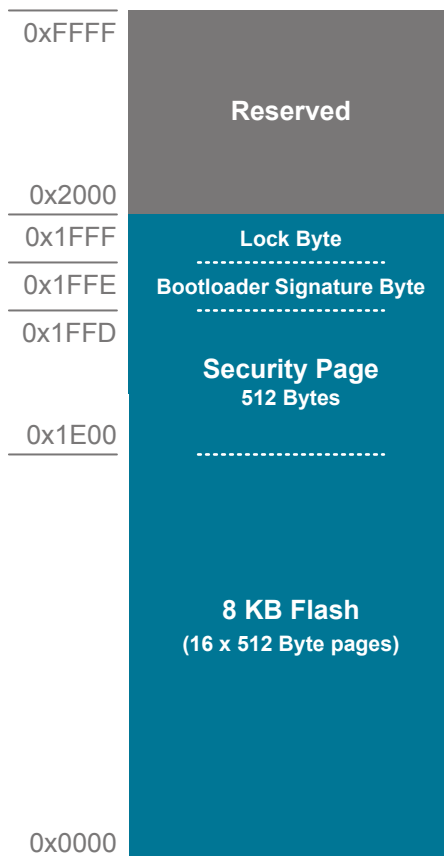
1. Errata Summary

Table 1.1. Errata Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Fixed Revision
1	BL_E101	UART Bootloader Not Available	No	A	B
2	RST_E102	VDD Monitor Disabled	Yes	A, date codes 1531 or earlier	A, date codes 1532 or later

2. Detailed Errata Descriptions

2.1 BL_E101 – UART Bootloader Not Available

Description of Errata	
The revision 1.1 data sheet mentions a UART bootloader in device flash. This bootloader is not available on revision A devices.	
Affected Conditions / Impacts	
<p>Systems intending to use a UART bootloader will need to implement and download a custom bootloader to the devices received from the factory. The factory bootloader in AN945 will not work on revision A devices.</p> <p>Devices with the factory bootloader and Bootloader Signature Byte support will use the byte immediately before the Lock Byte as a Bootloader Signature Byte to determine if the bootloader is present in flash. For example, in a device with 8 KB of flash:</p>	
 <p>The diagram illustrates the memory layout of the 8 KB flash. It shows a vertical stack of memory addresses from 0x0000 at the bottom to 0xFFFF at the top. The main section, from 0x0000 to 0x1E00, is labeled '8 KB Flash (16 x 512 Byte pages)'. Within this section, the address 0x1FFD is marked as the 'Security Page 512 Bytes'. Above this, at address 0x1FFE, is the 'Bootloader Signature Byte', and at address 0x1FFF is the 'Lock Byte'. The memory from 0x2000 to 0xFFFF is designated as 'Reserved'.</p>	
<p>For applications that do not use the bootloader, the Bootloader Signature Byte can be any value other than 0xA5 to enable normal operation.</p> <p>Note that the devices placed on a Starter Kit board may not have the Bootloader Signature Byte support included, so these parts may behave differently than loose parts ordered separately.</p>	
Workaround	
<p>A bootloader is not required for normal operation. However, if a bootloader is required by the application, a custom-written bootloader can be downloaded to devices received from the factory. The factory bootloader will not work on revision A devices.</p> <p>Systems using the device should not write the Bootloader Signature Byte to 0xA5 when the intent is to not use the bootloader.</p>	
Resolution	

This issue will be resolved in revision B devices.

More information on the bootloader can be found in the device data sheet and in AN945: "EFM8 Factory Bootloader User Guide". Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) and in Simplicity Studio using the [Application Notes] tile.

2.2 RST_E102 – VDD Monitor Disabled

Description of Errata

When an EFM8SB2 device is subjected to a slowly decaying VDD ramp (for example, 100 $\mu\text{V}/\text{sec}$), oscillations on the /RST pin caused by the VDD monitor can result in the VDD monitor getting disabled. The oscillations result from the slow reaction time of the VDD monitor hysteresis circuit combined with VDD ripple caused by the changing device current demands as it transitions from its operating state to the reset state. The oscillation behavior is exacerbated by:

1. Slow VDD decay timing resulting from powering the device from a discharging battery or super capacitor, for example.
2. A high active supply current in comparison to the supply current of the device when it is held in reset. This can be caused by high system clock frequency or high GPIO sourcing load.
3. Device dependencies, with some part-to-part variations that affect the probability of the failure occurring.

Affected Conditions / Impacts

The VDD monitor enable bit is unique in that it is only affected by a power-on reset (POR) (which sets the bit to a '1') and an SFR write, which can clear the bit to '0' or set it to '1' under software control. All other reset sources have no effect on the VDD monitor enable bit. Thus, if any action sets the bit to a '0', it will remain '0' until a POR occurs or software sets the bit to a '1'.

Workaround

Firmware can enable the VDD monitor as the first instruction executed after a reset. On systems written in C, this means editing the startup routine (i.e. STARTUP.A51 for Keil) to enable the VDD monitor as the first instruction. This will minimize any duration that the system is operating while the VDD monitor is disabled.

Resolution

Fixed in revision A devices with date codes of 1532 and later.

3. Revision History

3.1 Revision 0.5

August 22, 2016

BL_E101: Updated fixed revision to B. The previous version of this errata stated the bootloader was available on revision A devices with a date code of 1544 or later. This is incorrect. The bootloader is available in revision B devices.

3.2 Revision 0.4

February 29, 2016

Added RST_E102.

3.3 Revision 0.3

November 24, 2015

Updated Errata #1 (USB Bootloader Not Available)

- Added designator BL_E101.
- Updated fixed revision to A, date code 1544 and later.

3.4 Revision 0.2

June 10, 2015

Updated Errata #1 (USB Bootloader Not Available)

- Updated affected condition with expected behavior.
- Updated workaround with warning to not write 0xA5 to Bootloader Signature Byte.

3.5 Revision 0.1

January 30, 2015

Initial release.

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