March 5, 2013

SiM3U1xx and SiM3C1xx Revision B Errata

Hardware Errata

Erratum #	Title	Impact
H1	AES Status Flags Auto-Clear (AES0)	Minor
H2	Debug Adapter Hardware Reset	Minor
H3	USART TCPTI Interrupt Flag Repeatedly Sets (USART0, USART1)	Minor
H4	I2C Repeated Start (I2C0, I2C1)	Minor
H5	USB Module Clock (USB0)	Minor
H6	Extra VIOHD current on SiM3U1x4 and SiM3C1x4 Devices (40-pin Packages)	Minor
H7	Disabled VDD Monitor does not prevent flash write or erase operations	Minor

Impact definition: Each erratum is marked with an impact, as defined below:

- Minor – Workaround exists.
- Major – Errata that do not conform to the data sheet or standard.
- Information – The device behavior is not ideal but acceptable. Typically, the data sheet will be changed to match the device behavior.

Hardware Errata Details

H1. **AES Status Flags Auto-Clear (AES0)**

Description:
The three status flags XOR Data FIFO Overrun (XORF), Input/Output Data FIFO Overrun (DORF), and Input/Output Data FIFO Underrun (DURF) will auto-clear after being set by the AES module.

Impacts:
If the AES error interrupt occurs, firmware will not be able to directly determine which of these flags set the Error Interrupt Flag (ERRI) in the Status Register. When any of these three status flags are set by hardware, they do not retain the value. All three status flags are auto-cleared by hardware.

Workaround:
Firmware enabling the AES error interrupt (ERRI flag) should not decode the interrupt source using the XORF, DORF, and DURF flags. Instead, firmware can always reset the AES module to clear all faults.

Resolution:
None.

H2. **Debug Adapter Hardware Reset**

Description:
Using the 'HW RESET' debug reset option causes the IDE to lose the connection to the MCU after issuing a reset.

Impacts:
When the debugger issues a pin reset, the debug logic on the MCU is also reset, which results in the loss of connection to the IDE.

Workaround:
Do not select 'HW RESET' as the debug reset option. Instead, use the 'SYSRESETREQ' or "VECTRESET' options.

Resolution:
None.

H3. **USART TCPTI Interrupt Flag Repeatedly Sets (USART0, USART1)**

Description:
The Transmit Complete Interrupt Flag (TCPTI) is repeatedly set throughout the last bit transfer when the following three criteria are met:

- Transmit Complete Threshold (TCPTTH) is configured to trigger an interrupt at the end of each transmission (TCPTTH = 0)
- The USART is configured for synchronous mode (TSYNCEN = 1)
- The Clock Idle State (CLKIDLE) setting equals the Clock Edge Select (CLKESEL) setting.

Impacts:
If the conditions in the description match the USART settings and the Transmit Complete Interrupt is enabled (TCPTIEN = 1), the interrupt will repeatedly trigger during the last bit of transmission.

Workaround:
To avoid this behavior:

- Use the Transmit Data Request Interrupt (TDREQI) instead of the Transmit Complete Interrupt (TCPTI). The difference between the two interrupts is that the Transmit Data Request Interrupt will trigger whenever FIFO contains enough empty slots as specified in Transmit FIFO Threshold (TFTH), and the Transmit Complete Interrupt (TCPTI) will trigger after each byte is sent.
- Firmware can delay at least one USART bit-time before clearing the Transmit Complete Interrupt Flag (TCPTI).
- Configure the USART to operate in a synchronous mode (TSYNCEN = 1) where the Clock Idle State (CLKIDLE) setting does not equal the Clock Edge Select (CLKESEL) setting.

Resolution:
None.

H4. **I2C Repeated Start (I2C0, I2C1)**

Description:
The I2C peripheral will not issue a repeated start when the Data Setup Time Extension (SETUP) is 0.

Impacts:
When attempting to access an EEPROM or I2C device that requires a repeated start, the MCU will not issue the repeated start of the I2C transaction if the Data Setup Time Extension (SETUP) value is 0.

Workaround:
Write a non-zero value to the Data Setup Time Extension (SETUP) register when repeated starts are necessary.

Resolution:
None.

H5. **USB Module Clock (USB0)**

Description:
Accessing USB Control registers without enabling the USB APB clock will cause the MCU core to lock up.

Impacts:
Firmware that accesses the USB registers without enabling the USB APB clock can cause an MCU to lock up. Performing a hard reset will still result in the same condition if the code that causes the core to lock up is still executed.

Workaround:
The latest USB Debug Adapter DLL (SLAB_CM_Keil.dll version 1.0.0.4) allows the debug adapter to connect to a device that is in this state. If this condition occurs, uVision will display a message that gives the user an option to use a core reset method to halt the CPU. This method allows the user to download a new code image to the device that will not induce the condition.

Resolution:
None.

H6. **Extra VIOHD current on SiM3U1x4 and SiM3C1x4 Devices (40-pin Packages)**

Description:
Devices using the 40-pin package (SiM3U1x4 and SiM3C1x4) will draw extra current (~150 µA) from the VIOHD supply in the lowest power mode (Power Mode 9 or PM9) using the reset settings of the device. Setting the PBDRVEN bit after a reset will remove the extra current draw.

Impacts:
Systems using devices in the 40-pin package (SiM3U1x4 or SiM3C1x4) may experience extra current consumption (~150 µA) in the lowest power mode.

Workaround:
Setting the PBDRVEN bit in the PBDRV High Drive I/O register releases the PB4 port drivers and removes the extra current draw. Firmware should always assert PBDRVEN after a reset to reduce the power consumption to the values specified in the data sheet. This bit ensures the PB4 pins are tristate on a power-up, and no adverse effects occur if this bit is set when the PB4 pins are unused.

Resolution:
None.

H7. **Disabled VDD Monitor does not prevent flash write or erase operations**

Description:
The SiM3U1xx/SiM3C1xx Reference Manual states (revision 1.0, page 380):

Firmware cannot modify flash through the interface when the supply monitor in the VMONn module is disabled or disabled as a reset source (device reset source module). Any write or erase operations initiated while the supply monitor is disabled or disabled as a reset source will be ignored.

For devices with a trace code before 1311, flash modification will occur even if the VMON0 supply monitor is disabled or is disabled as a reset source.

Impacts:
Systems containing flash modification code running with the VMON0 supply monitor disabled or disabled as a reset source may experience inadvertent flash modification if VDD drops below the minimum Operating Supply Voltage on VDD specified by the data sheet.

Workaround:
Devices with firmware modifying flash with write or erase operations using the FLASHCTRL module must ensure that the VMON0 supply monitor is enabled and is enabled as a reset source prior to executing the flash modification operation.

Resolution:
Devices with date codes later than 1311 will behave as described in revision 1.0 of the SiM3U1xx/SiM3C1xx Reference Manual. These devices will ignore flash write and erase operations if the VDD Monitor (VMON0) is not enabled or is not enabled as a reset source.

Documentation Errata

The Documentation Errata is applicable to the following documents:

- SiM3U1xx Data Sheet Revision 1.0
- SiM3C1xx Data Sheet Revision 1.0
- SiM3U1xx-SiM3C1xx Reference Manual Revision 1.0

Erratum #	Title	Impact
D1	Delay When Updating Capsense Registers (CAPSENSE0) [Reference Manual, chapter 13]	Information
D2	Input High Voltage on High Drive I/O with V_{IOHD} between 1.8 V and 2.0 V [Data Sheet, Table 3.18 (U) Table 3.17 (C)]	Major
D3	Low Frequency Oscillator Lower Frequency Limit at 25 °C and 3.3 V [Data Sheet, Table 3.8]	Major
D4	Comparator Inputs Swapped on 40-pin Packages [Data Sheet, Table 6.3]	Information

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- Minor – Workaround exists.
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Documentation Errata Details

D1. **Delay When Updating Capsense Registers (CAPSENSE0) [Reference Manual, chapter 13]**

Description:
Capacitive sensing registers can take up to 2 CAPSENSE clocks to update after an end-of-scan or comparator interrupt.

Impacts:
After completing an end-of-scan or comparator interrupt, firmware should wait for 2 CAPSENSE clocks before reading the values of the CAPSENSE registers. A delay loop can be used, but the number of iterations required in the loop will depend on the system clock frequency.

Workaround:
None.

Resolution:
This will be fixed in revision 1.1 of the SiM3U1xx/SiM3C1xx Reference Manual.

D2. **Input High Voltage on High Drive I/O with V_{IOHD} between 1.8 V and 2.0 V [Data sheet, Table 3.18 (U) Table 3.17 (C)]**

Description: The minimum input voltage (VIH) on the High Drive I/O is 0.75 x VIOHD when VIOHD is between 1.8 V and 2.0 V, when the expected minimum input voltage (VIH) is 0.7 x VIOHD in this VIOHD range.

Impacts: A high signal of 0.7 x VIOHD may not always be interpreted correctly by the High Drive I/O on the device when VIOHD is between 1.8 V and 2.0 V.

Workaround: Systems interfacing with the High Drive I/O on the device when VIOHD is between 1.8 V and 2.0 V should use a minimum input high voltage of 0.75 x VIOHD to ensure the device always interprets a high input signal correctly.

Resolution: The next revision of the data sheet, revision 1.1, will include an updated specification for the High Drive I/O input voltage range with VIOHD is between 1.8 V and 2.0 V. The specification for VIOHD between 2.0 V and 6 V is unchanged.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	1.8 V ≤ V_{IOHD} < 2.0 V	**0.75 x V_{IOHD}**	—	—	V
		2.0 V ≤ V_{IOHD} < 6 V	V_{IOHD} – 0.6	—	—	V

D3. **Low Frequency Oscillator Lower Frequency Limit at 25 °C and 3.3 V [Data Sheet, Table 3.8]**

Description: The minimum frequency of the Low Frequency Oscillator at 25 °C and 3.3 V is 15.6 kHz, when the expected minimum frequency is 15.8 kHz.

Impacts: Systems expecting a minimum Low Frequency Oscillator limit of 15.8 kHz at 25 °C and 3.3 V may count or interrupt slightly slower due to the reduced limit of 15.6 kHz.

Workaround:
None.

Resolution: The next revision of the data sheet, revision 1.1, will include an updated specification for the Low Frequency Oscillator at 25 °C and 3.3 V. The specification for the full temperature and supply range is unchanged.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Low Frequency Oscillator (LFOSC0)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	13.4	16.4	19.7	kHz
		TA = 25 °C, VDD = 3.3 V	**15.6**	16.4	17.3	kHz

D4. **Comparator Inputs Swapped on 40-pin Packages [Data Sheet, Table 6.3]**

Description: Table 6.3 of the SiM3U1xx and SiM3C1xx data sheets lists PB1.2 as the negative input (CMP0N.0/CMP1N.0) and PB1.3 as the positive input (CMP0P.1/CMP1P.1) for the comparators (CMP0 and CMP1). These inputs are swapped such that PB1.2 is the positive input (CMP0P.0/CMP1P.0) and PB1.3 is the negative input (CMP0N.0/CMP1N.0). This information is correct in the Reference Manual.

Impacts: Systems expecting PB1.2 to be the positive input and PB1.3 to be the negative input to the comparators must swap the inputs or expect opposite polarity from the comparator.

Workaround:
None.

Resolution: The next revision of the data sheet, revision 1.1, will swap these signals in Table 6.3.