CP2114 Errata

This document contains information on the CP2114 errata. The latest available revision of this device is revision B02.

For errata on older revisions, refer to the errata history section for the device. The revision information is typically specified in or near the trace code on the device. Refer to the package marking information in the data sheet for more information.

Errata effective date: March, 2019.

1. Active Errata Summary

These tables list all known errata for the CP2114 and all unresolved errata in revision B02 of the CP2114.

Table 1.1. Errata History Overview

Designator	Title/Problem	Exists on Revision:	
		B01	B02
CP2114_E101	Dropouts in Asynchronous-Mode Playback Audio on 64-bit Systems	X	—
CP2114_E102	Record Sample Values Intermittently Corrupted	X	—
CP2114_E103	Playback Mute-by-Zero Can Cause Record Corruption	X	—
CP2114_E104	USB Descriptor Not Correct for Synchronous Mode	X	—
CP2114_E105	Resume May Fail on Externally-Clocked Systems	X	—
CP2114_E106	UART is Unusable if GPIO.9 is Reconfigured	X	—
CP2114_E107	Record Can Fail After Rebooting PC	X	—
CP2114_E108	UART Can Deliver Duplicated RX Character	X	—
CP2114_E109	Failure to Enumerate with Unprogrammed Configuration When External Clock is Missing	X	—
CP2114_E110	Host PC Record Mute Icon Controls CP2114 Playback Muting	X	—
CP2114_E111	GPIO and Suspend	X	—
CP2114_E112	Right-channel ADC data lags by one sample	X	—
CP2114_E113	Configuration write fails when SYSCLK is driven by the internal 49.152 MHz oscillator	X	X
CP2114_E114	Left-Justified ADC data is incorrect for signals greater than -6 dBFS	—	X
CP2114_E115	Failure to switch back to using external clock after resuming from USB suspend mode	—	X

Table 1.2. Active Errata Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
1	CP2114_E113	Configuration write fails when SYSCLK is driven by the internal 49.152 MHz oscillator	Yes	B02	—
2	CP2114_E114	Left-Justified ADC data is incorrect for signals greater than -6 dBFS	Yes	B02	—
3	CP2114_E115	Failure to switch back to using external clock after resuming from USB suspend mode	Yes	B02	—

2. Detailed Errata Descriptions

2.1 CP2114_E113 – Configuration write fails when SYSCLK is driven by the internal 49.152 MHz oscillator

Description of Errata
Writing new configuration can fail when SYSCLK is currently being driven by the internal 49.152 MHz oscillator.
Affected Conditions / Impacts
This problem can intermittently occur on systems that configure SYSCLK to be driven by the internal oscillator at 49.152 MHz. The problem does not occur on systems that operate in on of the other three permissible clocking modes: • SYSCLK driven by internal oscillator at 48.0 MHz • SYSCLK driven by external clock at 49.152 MHz • SYSCLK driven by external clock at 48.0 MHz
Workaround
When programming configurations, use one of the three clock modes listed above that are not susceptible to the problem. For example, factory-programmed configuration[0] uses the internal 48.0 MHz oscillator to drive USBCLK and SYSCLK.
Resolution
There is currently no resolution for this issue.

2.2 CP2114_E114 – Left-Justified ADC data is incorrect for signals greater than -6 dBFS

Description of Errata
When configured in Left-Justified mode, the analog input (ADC) sample values are corrupted for signals that exceed -6 dBFS.
Affected Conditions / Impacts
Problem occurs when CP2114 is configured for Left-Justified mode and used with ADC. Problem does not occur for analog output.
Workaround
• Operate ADC in I2S mode rather than Left-Justified mode. • Configure the ADC gain such that input signals will not exceed -6dBFS.
Resolution
There is currently no resolution for this issue.

2.3 CP2114_E115 – Failure to switch back to using external clock after resuming from USB suspend mode

Description of Errata
Prior to entering USB suspend mode, the CP2114 configures itself to drive USBCLK and SYSCLK from its internal oscillator. This allows the external clock oscillator to be disabled by the active-high or active-low SUSPEND pins, to meet the USB maximum suspend-mode current of 2.5 mA for bus-powered devices. (External clock oscillators typically draw more than 2.5 mA when active) If the USB host performs a device reset upon resuming from suspend mode, the CP2114 operates as expected. However, if the host does not perform a device reset upon resuming from suspend mode, the CP2114 will continue to drive its USBCLK and SYSCLK from the internal 48 MHz oscillator.
Affected Conditions / Impacts
Systems that use an external clock for USBCLK or SYSCLK are susceptible to the problem. For systems that operate in Async mode with an external 49.152 MHz clock, the problem will likely result in dropouts of the DAC/ADC data. For other configurations the problem may not be evident, e.g. SYSCLK is configured for external 48 MHz clock but after resuming is being driven by the internal 48 MHz oscillator.
Workaround
There are several workarounds for this issue: • Configure the host (e.g. BIOS setting) to remove USB power in Sleep mode. • For Windows systems: Add the 'ResetOnResume' registry key by executing the following command with Administrator privilege: `REG ADD HKLM\SYSTEM\ControlSet001\Control\usbflags\10C48A270100 /v ResetOnResume /t REG_BINARY /d 01 /f` • For Linux systems: Add a 'USB_QUIRK_RESET_RESUME' entry for the CP2114 VID/PID to `drivers/usb/core/quirks.c`. • Manually reset or power-cycle the CP2114 after resuming from sleep mode. • Use a codec that accepts 12.0 MHz MCLK and configure the CP2114 to use the internal 48 MHz oscillator.
Resolution
There is currently no resolution for this issue.

3. Errata History

This section contains the errata history for CP2114 devices.

For errata on latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 Errata History Summary

This table lists all resolved errata for the CP2114.

Table 3.1. Errata History Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
1	CP2114_E101	Dropouts in Asynchronous-Mode Playback Audio on 64-bit Systems	Yes	B01	B02
2	CP2114_E102	Record Sample Values Intermittently Corrupted	No	B01	B02
3	CP2114_E103	Playback Mute-by-Zero Can Cause Record Corruption	No	B01	B02
4	CP2114_E104	USB Descriptor Not Correct for Synchronous Mode	No	B01	B02
5	CP2114_E105	Resume May Fail on Externally-Clocked Systems	No	B01	B02
6	CP2114_E106	UART is Unusable if GPIO.9 is Reconfigured	Yes	B01	B02
7	CP2114_E107	Record Can Fail After Rebooting PC	No	B01	B02
8	CP2114_E108	UART Can Deliver Duplicated RX Character	No	B01	B02
9	CP2114_E109	Failure to Enumerate with Unprogrammed Configuration When External Clock is Missing	Yes	B01	B02
10	CP2114_E110	Host PC Record Mute Icon Controls CP2114 Playback Muting	Yes	B01	B02
11	CP2114_E111	GPIO and Suspend	No	B01	B02
12	CP2114_E112	Right-channel ADC data lags by one sample	No	B01	B02

3.2 Detailed Errata Descriptions

3.2.1 CP2114_E101 – Dropouts in Asynchronous-Mode Playback Audio on 64-bit Systems

Description of Errata
Periodic audio playback dropouts can occur when using Asynchronous Mode on 64-bit systems. The dropouts are caused by playback FIFO underruns or overruns which occur because the 64-bit host fails to periodically request feedback packets from the CP2114. The CP2114's Synchronization Endpoint 'bRefresh' element has a value of 1, which corresponds a requested feedback rate of 2 ms. Although a bRefresh value of 1 works on 32-bit systems and is compliant with the USB Audio Class Specification, it has been discovered that some 64-bit host machines do not work properly using bRefresh values less than 4.
Affected Conditions / Impacts
Systems using the CP2114 in asynchronous mode with 64-bit operating systems may hear audible glitches in the audio playback.
Workaround
The workaround for this problem is to program a new configuration that uses Synchronous mode. As long as the internal oscillator is used for the CP2114 clock, synchronous mode can produce glitch-free audio.
Resolution
This issue is resolved in revision B02 devices.

3.2.2 CP2114_E102 – Record Sample Values Intermittently Corrupted

Description of Errata
When simultaneously streaming In and Out audio data in Synchronous mode, there can be intermittent invalid samples on the Analog Input stream. The invalid values are multiples of 256 (i.e. the LSB is always 0).The problem was observed only when the CP2114 Record (i.e. Analog Input) data is being monitored on the CP2114 Playback, not when the Record data is being monitored on another playback device, even if the CP2114 is simultaneously playing back a different audio stream. The problem usually is precipitated by excessive host activity which may perturb the USB isochronous IN/OUT packets, causing FIFO underrun/overrun.
Affected Conditions / Impacts
Systems using record and playback simultaneously in synchronous mode may see intermittent invalid record samples.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B02 devices.

3.2.3 CP2114_E103 – Playback Mute-by-Zero Can Cause Record Corruption

Description of Errata
The Mute-by-Zero (MBZ) bit sets the playback samples to zero as it's supposed to, but if Record is also active, there are intermittent glitches in the left-channel audio data when the playback is muted.
Affected Conditions / Impacts
Systems using the MBZ feature may see intermittent glitches in the record data.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B02 devices.

3.2.4 CP2114_E104 – USB Descriptor Not Correct for Synchronous Mode

Description of Errata
The CP2114 HID USB-to-UART interface does not show up in Linux when using synchronous mode. This issue has been replicated using Ubuntu 12.04/64bit and 14.04/32bit. This issue does not occur on Windows hosts.
Affected Conditions / Impacts
The CP2114 HID USB-to-UART interface is not available with Linux hosts.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B02 devices.

3.2.5 CP2114_E105 – Resume May Fail on Externally-Clocked Systems

Description of Errata
Disconnecting and reconnecting an externally-clocked CP2114 to a USB host may sometimes cause the CP2114 to fail enumeration.
Affected Conditions / Impacts
Systems in an externally-clocked configuration may need a power-on or reset cycle to enumeration properly after a disconnect-and-reconnect event.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B02 devices.

3.2.6 CP2114_E106 – UART is Unusable if GPIO.9 is Reconfigured

Description of Errata
The CP2114 UART pins do not function correctly if the GPIO.9 pin is not configured for CLKOUT mode.
Affected Conditions / Impacts
Systems intending to use the UART must keep GPIO.9 in CLKOUT mode.
Workaround
Systems intending to use the UART must keep GPIO.9 in CLKOUT mode.
Resolution
This issue is resolved in revision B02 devices.

3.2.7 CP2114_E107 – Record Can Fail After Rebooting PC

Description of Errata
If Record is active when the PC is rebooted, the Record feature does not work after reboot.
Affected Conditions / Impacts
Systems using Record may not be able to Record after a reboot. This condition is cleared by another reboot of the PC.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B02 devices.

3.2.8 CP2114_E108 – UART Can Deliver Duplicated RX Character

Description of Errata
The UART can intermittently deliver a duplicated RX (received) character.
Affected Conditions / Impacts
Systems using the UART feature may see an intermittently duplicated receive character.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B02 devices.

3.2.9 CP2114_E109 – Failure to Enumerate with Unprogrammed Configuration When External Clock is Missing

Description of Errata
If the DAC Select pins specify an unprogrammed configuration, the device expects an external clock and will not enumerate if an external clock is not present.
Affected Conditions / Impacts
Systems using the CP2114 should not select an unprogrammed configuration using the DAC Select pins. If an unprogrammed configuration is selected, provide an external clock to recover the device.
Workaround
Configure the DAC Select pins to indicate a valid configuration.
Resolution
This issue is resolved in revision B02 devices.

3.2.10 CP2114_E110 – Host PC Record Mute Icon Controls CP2114 Playback Muting

Description of Errata
Toggling the Record Mute icon on the host PC actually controls the CP2114 playback mute function.
Affected Conditions / Impacts
Systems using a CODEC with Record and Playback supported may see an unexpected mute condition on playback when the Record Mute icon is toggled.
Workaround
If the user mutes playback by activating the Record Mute icon, playback can be unmuted by toggling Record Mute back to unmuted, or by muting and unmuting playback via the host icon or board buttons.
Resolution
This issue is resolved in revision B02 devices.

3.2.11 CP2114_E111 – GPIO and Suspend

Description of Errata
CP2114 GPIO pins are briefly set to open-drain, drive low mode when entering Suspend mode. The pins will be in this state for approximately 2 µs before the Suspend mode GPIO settings are applied.
Affected Conditions / Impacts
Systems with a GPIO high before entering Suspend and setting a GPIO high while in Suspend will see a 2 µs pulse low on the GPIO pin when the CP2114 enters Suspend.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B02 devices.

3.2.12 CP2114_E112 – Right-channel ADC data lags by one sample

Description of Errata
For analog input, the right-channel (ADC) data lags the left-channel data by one sample.
Affected Conditions / Impacts
Systems using a CODEC with Record (ADC) functionality.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B02 devices.

4. Revision History

Revision 0.2

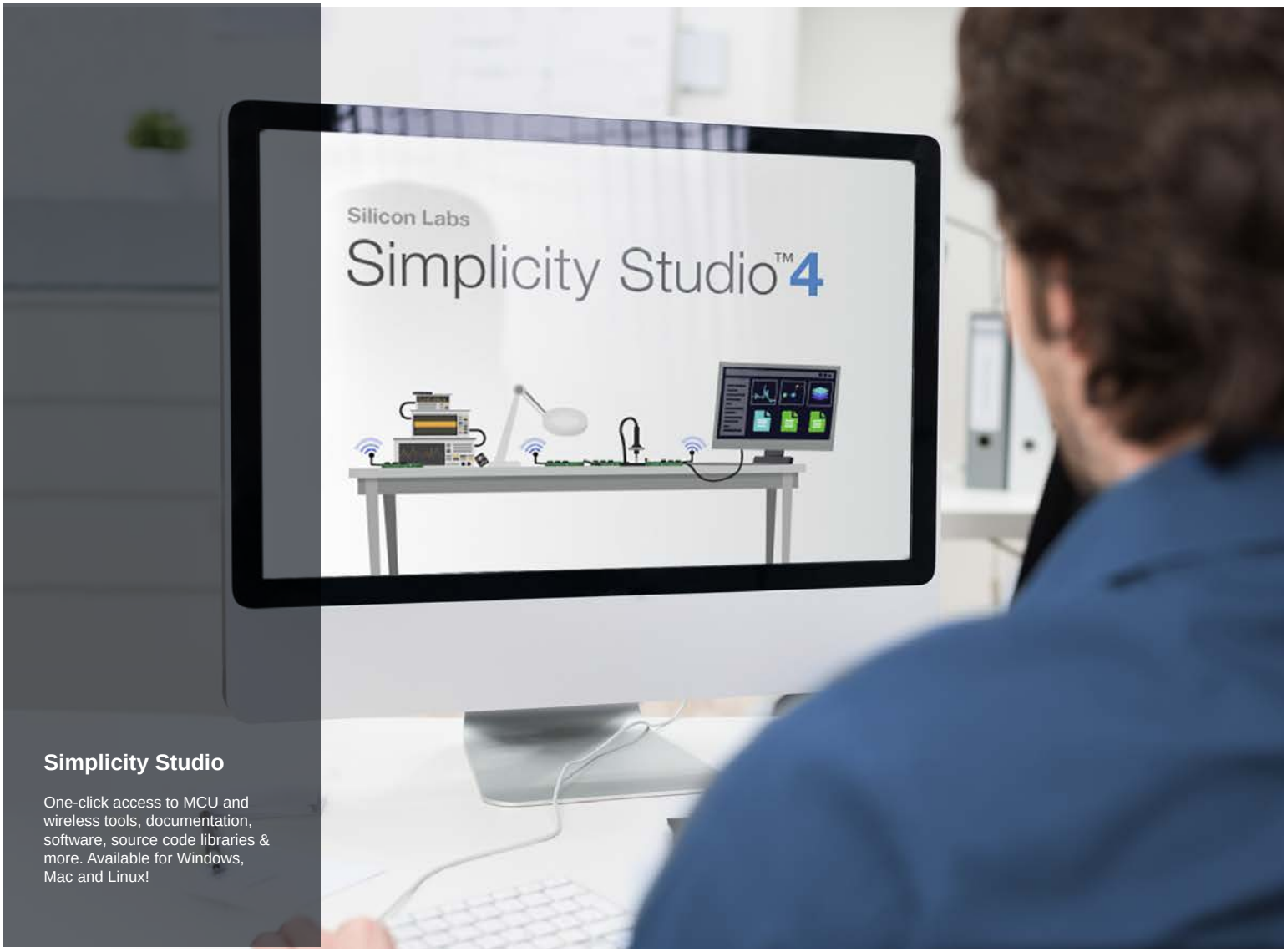
March, 2019

- Added CP2114_E113, CP2114_E114 and CP2114_E115.
- Added CP2114_E112 to the errata history section.
- Resolved CP2114_E101, CP2114_E102, CP2114_E103, CP2114_E104, CP2114_E105, CP2114_E106, CP2114_E107, CP2114_E108, CP2114_E109, CP2114_E110 and CP2114_E111 and moved to the errata history section.
- Merged errata history and errata into one document.
- Updated revision history format.

Revision 0.1

October, 2015

- Initial release.



Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

IoT Portfolio
www.silabs.com/IoT

SW/HW
www.silabs.com/simplicity

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com