Busy Bee
EFM8BB52 Errata

This document contains information on the EFM8BB52 errata. The latest available revision of this device is revision C.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from the package marking or electronically.

Errata effective date: April, 2023.

1. Errata Summary

The table below lists all known errata for the EFM8BB52 and all unresolved errata of the EFM8BB52.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision:		
			A	B	C
ADC_E201	Incorrect Output Upon MUX Switch	Yes	X	—	—
BL_E201	UART Bootloader Bootload Mode Entry Pin Not Available	Yes	X	X	X; resolved on devices with date code 2330 and later
CLK_E201	Incorrect SYSCLK Transition Restrictions	Yes	X	—	—
CLU_E201	Incorrect CLU to SPI Connections	Yes	X	—	—
CORE_E201	Prefetch Engine May Get Incorrect Flash Data When Exiting Snooze Mode	Yes	X	—	—
CUR_E201	Excess Current Consumption	No	—	X	—
POR_E201	POR Circuit Does Not Start Up	No	X	—	—
PWR_E201	Wakeup From Shutdown Mode Fails at High VDD and Low Temperatures	No	X	X	—
VREF_E201	RTS Noise Present In Reference Voltage Output	No	X	—	—

2. Current Errata Descriptions

This section contains known errata for revision C of this device.

2.1 BL_E201 – UART Bootloader Bootload Mode Entry Pin Not Available

Description of Errata
The data sheet states all devices come pre-programmed with UART bootloader in device flash. The pre-programmed factory bootloader for QFN20 and TSSOP20 packaged EFM8BB52 devices use an unavailable pin for bootload mode entry.
Affected Conditions / Impacts
When bootloader firmware executes on EFM8BB52 devices with QFN20 and TSSOP20 packaging, the unavailable pin used for bootload entry always reads logic low, putting the device in bootload mode. Application firmware can execute *after* an application firmware upload via bootloader, however following a reset, the device will revert back to bootload mode and will not progress to an uploaded application. The factory bootloader does not work as intended on QFN20 or TSSOP20 packaged EFM8BB52 devices.
Workaround
A bootloader is not required for normal operation. For applications that do not use the bootloader, the Bootloader Signature Byte can be modified to any value other than 0xA5 to enable normal operation. This is most commonly achieved by erasing the code security page in flash, which will also erase the pre-programmed factory bootloader. If a bootloader is required by the application, a custom-written bootloader can be downloaded to the device, replacing the pre-programmed factory bootloader image. A bootloader binary is also provided in *AN945: "EFM8 Factory Bootloader User Guide"* which utilizes the bootload entry pin specified in the device data sheet, and can be used to replace the factory bootloader.
Resolution
This issue is resolved in revision C devices with date code 2330 and later. More information on the bootloader can be found in the device data sheet and in *AN945: "EFM8 Factory Bootloader User Guide"*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) and in Simplicity Studio using the [**Application Notes**] tile.

3. Resolved Errata Descriptions

This section contains previous errata for EFM8BB52 devices.

For errata on the latest revision, refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 ADC_E201 – Incorrect Output Upon MUX Switch

Description of Errata
Incorrect ADC output can occur when the ADC is always on (i.e. IPOEN = 0) and the channel sequencer switches between certain channels.
Affected Conditions / Impacts
For the 32- and 28-pin packages: When IPOEN = 0 and the sequencer changes from a multiplexer channel ≤ 7 to a channel ≥ 8, the ADC conversion results for channels 8 and higher will be incorrect. For the 20-pin packages, When IPOEN = 0 and the sequencer changes from a multiplexer channel ≤ 6 to a channel ≥ 7, the ADC conversion results for channels 7 and higher will be incorrect.
Workaround
For the 32- and 28-pin packages: When using the sequencer with IPOEN = 0, avoid configurations in which the sequencer will change from channel 7 to channel 8. If ADC0MX is ≤ 7, then ADC0MX + NASCH must also be ≤ 7. The problem is not observed when the ADC powers down between conversions (when IPOEN = 1). For the 20-pin packages: When using the sequencer with IPOEN = 0, avoid configurations in which the sequencer will change from channel 6 to channel 7. If ADC0MX is ≤ 6, then ADC0MX + NASCH must also be ≤ 6. The problem is not observed when the ADC powers down between conversions (when IPOEN = 1).
Resolution
This issue is resolved in revision B devices.

3.2 CLK_E201 – Incorrect SYSCLK Transition Restrictions

Description of Errata
The clock selection logic does not allow switching to the HFOSC0 49 MHz or 49/1.5 MHz output when SYSCLK is currently using an HFOSC0 output and clock divider combination that results in a frequency less than 24.5 MHz. This means that SYSCLK can switch to the HFOSC0: • 49 MHz or • 49/1.5 MHz output only when SYSCLK is already: • 49 MHz, • 49/1.5 MHz, • 49 MHz with a 2x divider or • 24.5 MHz. On revision A devices, the clock selection logic permits SYSCLK to switch to: • 49 MHz, • 49/1.5 MHz or • 49 MHz with a 2x divider only when SYSCLK is already: • 49 MHz, • 49/1.5 MHz, • 49 MHz with a 2x divider, • 24.5 MHz, • 49 MHz with a 3x divider or • 49/1.5 MHz with a 2x divider.
Affected Conditions / Impacts
Switching SYSCLK to the 49MHz (CLKSL = 0x3) HFOSC0 output with a 2x divider (CLKDIV = 0x1) will only work when switching from one of the listed HFOSC0 output and clock divider combinations allowed for revision A. When switching SYSCLK from an HFOSC0 output and clock divider combination that results in a frequency less than 24.5 MHz to 49 MHz or 49/1.5 MHz, the core logic voltage regulator may experience a drop-out condition that potentially causes the device to lock-up. A power-on-reset is required to recover from the lock-up.
Workaround
Before switching SYSCLK to the 49 MHz HFOSC0 output with a 2x divider, first select one of the listed HFOSC0 output and clock divider combinations allowed for revision A. Do not select the 49 MHz or 49/1.5 MHz HFOSC0 output when SYSCLK is currently using an HFOSC0 output and clock divider combination that results in a frequency less than 24.5 MHz. First select one of the listed HFOSC0 output and clock divider combinations that results in a frequency greater than or equal to 24.5 MHz, then select the 49 MHz or 49/1.5 HFOSC0 output.
Resolution
This issue is resolved in revision B devices.

3.3 CLU_E201 – Incorrect CLU to SPI Connections

Description of Errata

The connections between the CLUn outputs and the SPI0 inputs are incorrect.

Affected Conditions / Impacts

The CLUn to SPI0 connections are incorrect on revision A devices. Specifically, there is no connection between the CLU0 output and SPI0. Connections exist between each of the CLU1, CLU2, and CLU3 outputs and the SPI0 inputs. When using CLUn to SPI0 connections, users should be aware that:

1. The CLU0 output cannot be used as an input to SPI0 on revision A.
2. Each output from CLU[3:1] can be used as an input to SPI0 on revision A.
3. The fix for the CLU0-to-SPI0 connections on revision B and later will require firmware that configures any CLU[3:1] outputs for use as inputs to SPI0 on revision A devices to be rewritten.

Workaround

User firmware can still assign CLU1, CLU2, and CLU3 outputs to SPI0 input signals as shown below, however the CLU0 output is not available as a SPI0 input. Table 3.1 CLU Output Configuration on page 6 shows the connections between CLUn and SPI0 in Revision A devices.

Table 3.1. CLU Output Configuration

CLU0.OUT	CLU1.OUT	CLU2.OUT	CLU3.OUT	Register Configuration	Output Type
-	SPI MOSI	SPI SCK	SPI MISO	Set via SPI0PCF	Asynchronous
-	SPI MISO	SPI MOSI	SPI SCK		

Table 3.2 SPI0PCF: SPI0 Pin Configuration on page 7 shows the SPI0 input signal configuration options in the SPI0PCF register for Revision A devices.

Table 3.2. SPI0PCF: SPI0 Pin Configuration

Bit	7	6	5	4	3	2	1	0
Name	SCKSEL		Reserved	MISEL		Reserved	SISEL	
Access	RW		R	RW		R	RW	
Reset	0x0		0	0x0		0	0x0	
SFR Page = 0x20; SFR Address: 0xDF								

Bit	Name	Reset	Access	Description
7:6	SCKSEL	0x0	RW	**Slave Clock Input Select.**
	This bit selects the source of the SCK clock input signal in slave mode.			
	Value	Name		Description
	0x0	CROSSBAR		SCK (slave mode clock input) is connected to the pin assigned by the crossbar.
	0x1	CLU2		SCK (slave mode clock input) is connected to the CLU2 output.
	0x2	CLU3		SCK (slave mode clock input) is connected to the CLU3 output.
5	*Reserved*	*Must write reset value.*		
4:3	MISEL	0x0	RW	**Master MISO Input Select.**
	This bit selects the source of the MISO data input signal in master mode.			
	Value	Name		Description
	0x0	CROSSBAR		MISO (master mode data input) is connected to the pin assigned by the crossbar.
	0x1	CLU1		MISO (master mode data input) is connected to the CLU1 output.
	0x2	CLU3		MISO (master mode data input) is connected to the CLU3 output.
2	*Reserved*	*Must write reset value.*		
1:0	SISEL	0x0	RW	**Slave MOSI Input Select.**
	This bit selects the source of the MOSI data input signal in slave mode.			
	Value	Name		Description
	0x0	CROSSBAR		MOSI (slave mode data input) is connected to the pin assigned by the crossbar.
	0x1	CLU1		MOSI (slave mode data input) is connected to the CLU1 output.
	0x2	CLU2		MOSI (slave mode data input) is connected to the CLU2 output.

Resolution

This issue is resolved in revision B devices.

3.4 CORE_E201 – Prefetch Engine May Get Incorrect Flash Data When Exiting Snooze Mode

Description of Errata
When the prefetch engine is enabled and the device enters then exists Snooze mode, the prefetch engine may read incorrect data from the flash and propagate it to the instruction register.
Affected Conditions / Impacts
When the prefetch engine is enabled and the device enters then exits Snooze mode, the CPU may receive an invalid instruction, resulting in unexpected behavior.
Workaround
Before entering Snooze mode, ensure that: • The SYSCLK is less than 25 MHz • The prefetch engine is disabled by setting PFE0CN.FLRT = 0
Resolution
This issue is resolved in revision B devices.

3.5 CUR_E201 – Excess Current Consumption

Description of Errata
Current consumption is higher than specified in all power modes except Shutdown mode.
Affected Conditions / Impacts
In any power mode other than Shutdown mode, the device consumes about 100 µA excess current at 25 degrees Celsius.
Workaround
There is no workaround for this issue.
Resolution
This issue is resolved in revision C devices.

3.6 POR_E201 – POR Circuit Does Not Start Up

Description of Errata
The POR circuit does not start on about 5% of revision A devices.
Affected Conditions / Impacts
The device cannot enter Shutdown mode. If Shutdown mode is enabled, the device remains stuck between Active mode and Shutdown mode. A power-on-reset is needed to recover the device.
Workaround
There is no workaround for this issue.
Resolution
This issue is resolved in revision B devices.

3.7 PWR_E201 – Wakeup From Shutdown Mode Fails at High VDD and Low Temperatures

Description of Errata
The device immediately gets stuck in Shutdown mode when it powers up with VDD greater than 5V and an ambient temperature lower than 0 degrees Celsius.
Affected Conditions / Impacts
With a VDD greater than 5 V at 0 degrees Celsius or below, the inrush current into the startup circuit is too high and causes the device to immediately enter and stay in Shutdown mode, preventing the device from starting up at all.
Workaround
There is no workaround for this issue.
Resolution
This issue is resolved in revision C devices.

3.8 VREF_E201 – RTS Noise Present In Reference Voltage Output

Description of Errata
Certain devices suffer from RTS (random telegraph signal) noise, also known as “popcorn noise” or “burst noise,” in the on-chip voltage reference. This is observed as random, intermittent jumps of the reference between two different voltages.
Affected Conditions / Impacts
Affected devices may exhibit sporadic RTS noise at the output of the on-chip reference source. The noise is typically less than 0.2% of the reference voltage, but may be higher on some devices. Due to the low-frequency, intermittent nature of RTS noise, it is not feasible to screen large device quantities to eliminate the issue at production test. The on-chip reference source is available internally as an ADC reference, or can be buffered to the VREF pin to be used by the ADC, DAC, or external circuitry. Any circuit using the on-chip reference source will be affected, and the performance of these circuits will be impacted as a result. For example, the full scale input of the ADC is based directly on its voltage reference, and RTS noise at the reference may appear as sudden slope changes or linearity errors in the ADC output. Likewise, RTS noise on the DAC reference will be observed as sudden small changes in the output voltage, proportional to the change on the reference. There is no direct solution to correct for the RTS noise in the on-chip reference. Systems adversely affected by this issue should select a different reference source. Both the ADC and DAC have the option to use the VDD supply as a reference, as well as an externally-derived reference connected to the VREF pin.
Workaround
There is currently no workaround for this issue.
Resolution
This issue is resolved in revision B devices.

4. Revision History

Revision 0.3

April, 2023

- Added BL_E201.

Revision 0.2

August, 2021

- Updated the latest revision to revision C.
- Added CLK_E201, CORE_E201, CUR_E201, POR_E201, and PWR_E201.

Revision 0.1

November, 2020

- Initial release.

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