Zen Gecko
EFR32ZG14 Errata

This document contains information on the EFR32ZG14 errata. The latest available revision of this device is revision B.

Errata that have been resolved remain documented and can be referenced for previous revisions of this device.

The device data sheet explains how to identify the chip revision, either from the package marking or electronically.

Errata effective date: August, 2025.

1. Errata Summary

The following table lists all the known and unresolved errata for the EFR32ZG14.

Table 1.1. Errata Overview

Designator	Title/Problem	Workaround Exists	Exists on Revision
			B
CUR_E205	Elevated Current Consumption in EM4H and EM4S when SWCLK and SWDIO MODEn is Disabled	No	X
EMU_E220	DECBOD Reset During Voltage Scaling After EM2 or EM3 Wakeup	Yes	X
DBG_E204	Debug Recovery with JTAG Does Not Work	Yes	X
RMU_E202	External Debug Access Not Available After Watchdog or Lockup Full Reset	Yes	X

2. Current Errata Descriptions

2.1 CUR_E205 – Elevated Current Consumption in EM4H and EM4S when SWCLK and SWDIO MODEn is Disabled

Description of Errata
In EM0, EM1, EM2, and EM3, the input buffer for the SWCLK and SWDIO pins are disabled when MODEn is DISABLED for these pins, as expected. However, in EM4H and EM4S, the input buffer for the SWCLK and SWDIO pins are enabled by hardware and cannot be disabled by firmware. As a result, when MODEn is set to DISABLED for SWCLK and SWDIO and the device enters EM4H or EM4S, current consumption is elevated. To minimize EM4H/S current consumption, MODEn for these two pins should not be configured as DISABLED prior to EM4H/S entry. Instead, SWCLK should be configured as MODEn = INPUTPULL with pull-down enabled, and SWDIO should be configured as MODEn = INPUTPULL with pull-up enabled.
Affected Conditions / Impacts
Systems that use EM4H or EM4S may see elevated EM4H/EM4S current consumption up to approximately 100 uA when SWCLK and SWDIO MODEn is DISABLED.
Workaround
There is no known workaround for this issue
Resolution
There is currently no resolution for this issue.

2.2 EMU_E220 – DECBOD Reset During Voltage Scaling After EM2 or EM3 Wakeup

Description of Errata
An infrequent, asynchronous and unrelated internal event can intermittently delay normal BOD state-machine transition sequencing during voltage scaling from VSCALE0 (1.0 Vdc) to VSCALE2 (1.2 Vdc) when emerging from EM2/EM3 to EM0. This delay can cause erroneous DECBOD resets on some devices.
Affected Conditions / Impacts
Systems operating with core voltage scaling can experience a decouple voltage brownout reset (DECBOD) when exiting EM2 or EM3.
Workaround
Systems that use core voltage scaling need to enter EM2 or EM3 via a RAM executed wait for interrupt instruction with interrupts disabled. After wakeup and before voltage scaling, the system should delay for 14 µs, then check if an EMU calibration is active, and if so, wait for it to complete. **Note:** This workaround is included in `em_emu.c` in the v4.5 or later of the Gecko SDK. It is recommended to workaround this issue by using the latest Gecko SDK version. ```#define EMU_STATUS_CALIBRATION (0x1UL << 28)// Execute from RAM with interrupts disabled__WFI();ERRATA_FIX_EMU_E220_DELAY_CYCLES(); //delay 14 microsecondswhile (EMU->STATUS & EMU_STATUS_CALIBRATION);```
Resolution
There is currently no resolution for this issue.

2.3 DBG_E204 – Debug Recovery with JTAG Does Not Work

Description of Errata
The debug recovery algorithm of holding down pin reset, issuing a System Bus Stall AAP instruction, and releasing the reset pin does not work when using the JTAG debug interface. When using the JTAG debug interface, the core will continue to execute code as soon as the reset pin is released.
Affected Conditions / Impacts
The debug recovery sequence will not work when using the JTAG debug interface.
Workaround
Use the Serial Wire debug interface to implement the debug recovery sequence.
Resolution
There is currently no resolution for this issue.

2.4 RMU_E202 – External Debug Access Not Available After Watchdog or Lockup Full Reset

Description of Errata
When a reset is triggered in full-reset mode, a debugger will not be able to read AHB-AP or ARM core registers.
Affected Conditions / Impacts
Systems using the full reset mode for watchdog or lockup resets will see limited debugging capability after one of these resets triggers.
Workaround
There are three possible workarounds: • Software should configure peripherals to either LIMITED or EXTENDED mode if full debugger functionality is needed after a watchdog or lockup reset. • When using FULL reset mode, appending at least 9 idle clock cycles to the last debug command will allow the transaction to complete. • A power cycle or hard pin reset will restore normal operation.
Resolution
There is currently no resolution for this issue.

3. Revision History

Revision 0.2

August, 2025

- Added CUR_E205 and EMU_E220.

Revision 0.1

March, 2019
- Initial release.

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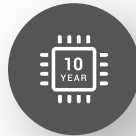
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