Wireless MCU Family
Si106x/8x Errata

This document contains information on the errata of revision A of Si106x/8x.

For errata on older revisions, please refer to the errata history for the device. The device data sheet explains how to identify chip revision, either from package marking or electronically.

Errata effective date: February 23rd, 2016.

1. Errata Summary

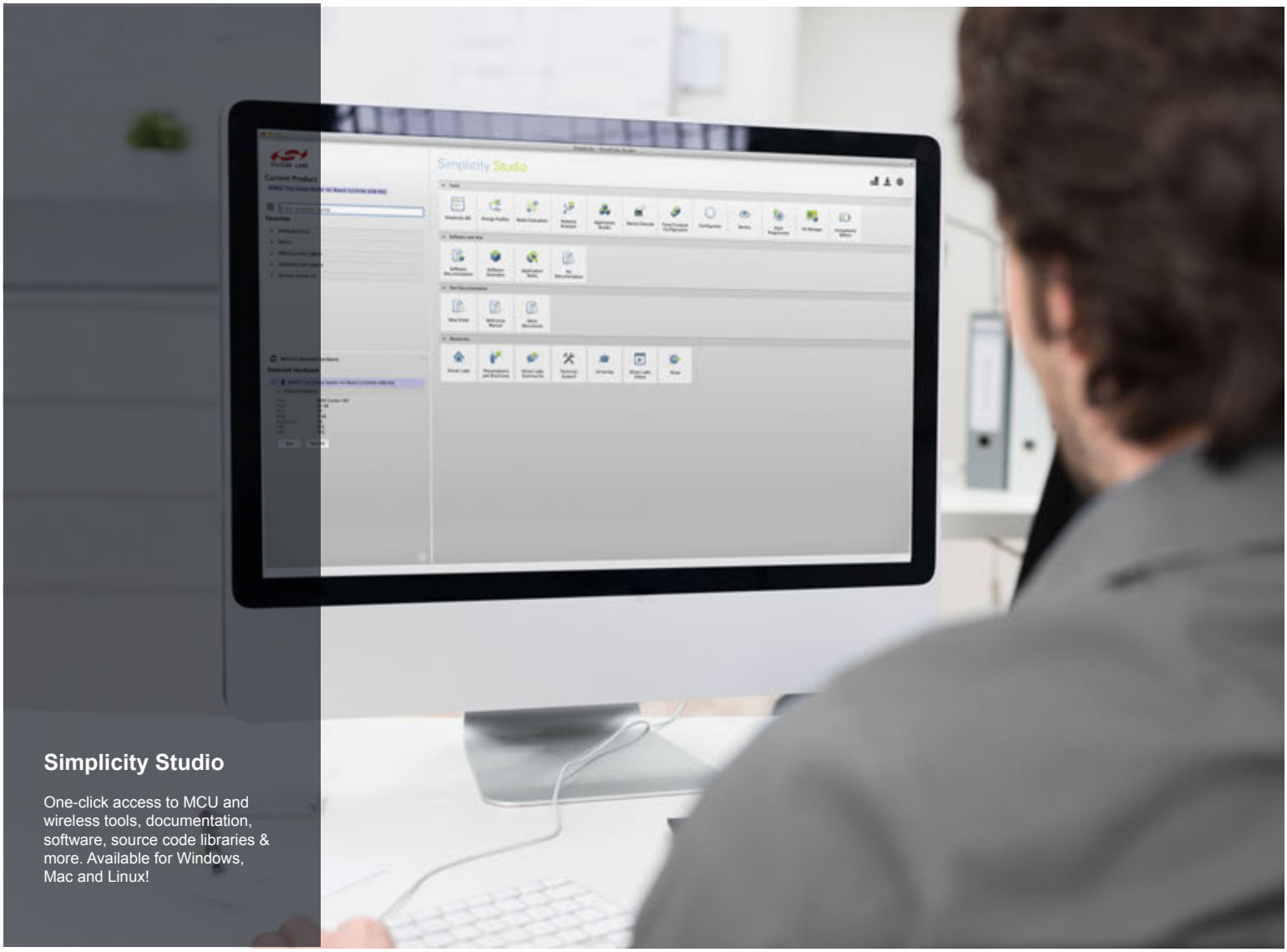
Table 1.1. Errata Status Summary

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Fixed Revision
1	RST_E102	VDD Monitor Disabled	Yes	Si106x revision A, date codes 1538 or earlier (does not apply to Si108x)	Si106x revision A, date codes 1539 or later (does not apply to Si108x)

2. Detailed Errata Descriptions

2.1 RST_E102 – VDD Monitor Disabled

Description of Errata
When an Si106x device is subjected to a slowly decaying VDD ramp (for example, 100 µV/sec), oscillations on the /RST pin caused by the VDD monitor can result in the VDD monitor getting disabled. The oscillations result from the slow reaction time of the VDD monitor hysteresis circuit combined with VDD ripple caused by the changing device current demands as it transitions from its operating state to the reset state. The oscillation behavior is exacerbated by: 1. Slow VDD decay timing resulting from powering the device from a discharging battery or super capacitor, for example. 2. A high active supply current in comparison to the supply current of the device when it is held in reset. This can be caused by high system clock frequency or high GPIO sourcing load. 3. Device dependencies, with some part-to-part variations that affect the probability of the failure occurring.
Affected Conditions / Impacts
The VDD monitor enable bit is unique in that it is only affected by a power-on reset (POR) (which sets the bit to a ‘1’) and an SFR write, which can clear the bit to ‘0’ or set it to ‘1’ under software control. All other reset sources have no effect on the VDD monitor enable bit. Thus, if any action sets the bit to a ‘0’, it will remain ‘0’ until a POR occurs or software sets the bit to a ‘1’.
Workaround
Firmware can enable the VDD monitor as the first instruction executed after a reset. On systems written in C, this means editing the startup routine (i.e. STARTUP.A51 for Keil) to enable the VDD monitor as the first instruction. This will minimize any duration that the system is operating while the VDD monitor is disabled.
Resolution
Fixed in revision A devices with date codes of 1539 and later.



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