Si117x/8x Errata

This document contains information on the errata of Si117x/8x. The latest available revision of this device is revision B3.

For errata on older revisions, please refer to the errata history section for the device. The revision information is specified in the REV_ID register or near the trace code on the device. Refer to the package marking information in the data sheet for more information.

Errata effective date: October 2018.

1. Active Errata Summary

The following tables list all known errata for the Si117x/8x and all unresolved errata in revision B3 of the Si117x/8x.

Table 1.1. Errata History Overview

Designator	Title/Problem	Exists on Revision	
		B2	B3
RMU_E101	Restriction on VDD Ramp Time	X	X
RMU_E102	Brownout During Measurement Causes Lockup	X	X
INT_E101	INT Output Drive and Clear Mechanism Changed	X	—

Table 1.2. Active Errata History Overview

Designator	Title/Problem	Workaround Exists	Affected Revision	Resolution
RMU_E101	Restriction on VDD Ramp Time	No	B3	—
RMU_E102	Brownout During Measurement Causes Lockup	Yes	B3	—

2. Detailed Errata Description

2.1 RMU_E101—Restriction on VDD Ramp Time

Table 2.1. RMU_E101—Restriction on VDD Ramp Time

Description of Errata
If a Si117x/8x device is subject to a VDD ramp to the minimum supply voltage of longer than 10 ms, the device can become unresponsive. The device will not respond to I^2C or SPI. LEDs connected to the LED drivers can brightly turn on. Slow VDD ramp rate in optical heart rate hardware designs is most commonly caused by large VLED capacitance.
Affected Conditions / Impacts
If the VDD rail takes longer than 10 ms to ramp to the minimum supply voltage, the device can become unresponsive and draw a large supply current.
Workaround
The power rail must be modified to reduce the VDD ramp time. Slow VDD ramp time is often due to large capacitance. VLED capacitors should be isolated from VDD through a current limiting series resistor. See AN1049 for details.
Resolution
There is currently no resolution for this issue.

2.2 RMU_E102—Brownout During Measurement Causes Lockup

Table 2.2. RMU_E102—Brownout During Measurement Causes Lockup

Description of Errata
If a Si117x/8x device is subject to a brownout event (VDD < 1.5 V) while in suspend mode, the device will become unresponsive to host communication and operation will halt. In this locked up state, the device will: • Draw a suspend current of ~1 mA from VDD. • NACK all I^2C transactions. • Respond with 0x27 to any SPI transaction.
Affected Conditions / Impacts
If a brownout event occurs during a suspend state, sensor operation will halt. The suspend state is used during ADC measurements for PPG and ECG, and during idle time if the ECG_ADCCONFIG.ECG_SUSPEND bit is set.
Workaround
If the ECG_ADCCONFIG.ECG_SUSPEND bit is used, disable the suspend mode. Increasing the VDD voltage will increase the voltage margin between the nominal operating voltage and the reset voltage and can help avoid this issue. If the brownout is caused by Si117x LED current draw, the power rail should be redesigned to minimize the VDD droop. Large VDD droop is typically caused by the lack of a current limiting series resistor between VDD and VLED or insufficient VDD/VLED capacitance. See AN1049 for details on sizing the series resistor and the VDD and VLED capacitances.
Resolution
There is currently no resolution for this issue.

3. Errata History

This section contains the errata history for Si117x/8x devices.

For errata on latest revision, please refer to the beginning of this document. The device data sheet explains how to identify chip revision, either from package marking or electronically.

3.1 Errata History Summary

The following table lists all resolved errata for the Si117x/8x.

Table 3.1. Errata History Status Summary

Designator	Title/Problem	Exists on Revision	
		B2	B3
INT_E101	INT_E101 - INT Output Drive and Clear Mechanism Changed	X	—

3.2 Detailed Errata Description

3.2.1 INT_E101 — INT Output Drive and Clear Mechanism Changed

Table 3.2. INT_E101 — INT Output Drive and Clear Mechanism Changed

Description of Errata
The INT pin was changed from an open-drain output to a push-pull output. The interrupt clear mechanism was changed from sending CMD_CLEAR_IRQ_STATUS to automatically clear the interrupt flag on the read of the REG_IRQ_STATUS (0x12) register. The REG_IRQ_STATUS (0x12) should be used instead of REG_IRQ_STATUS_B2 (0x18). The external INT pullup resistor can be left in place or removed. A detailed description of the interrupt clear mechanism is provided in AN1038 (rev > 2.0) Section 3.7 “Interrupts”. The si117xdrv library (rev ≥ 1.0.0) function Si117xGetIrqStatus implements both mechanisms and will handle the interrupt appropriately based on the REV_ID. The use of the si117xdrv library is recommended. This change was implemented in the B3 revision.
Affected Conditions / Impacts
Devices which are migrating from a B2 revision to a newer revision must update their interrupt handling mechanism. The use of the si117xdrv is recommended to automatically select the correct interrupt behavior based on REV_ID.
Workaround
The CMD_SET_INT_OE command will revert the interrupt clear mechanism, IRQ_STATUS register, and the INT pin output drive to the B2 behavior. The command should be issued after startup, before any interrupt has occurred. The effects will persist until the next reset. See AN1038 (rev ≥ 2.0) section 5.14 “SET_INT_OE Command” for details.
Resolution
This change was implemented in the B3 revision. Users should update their interrupt handling mechanism.

4. Revision History

Revision 0.2

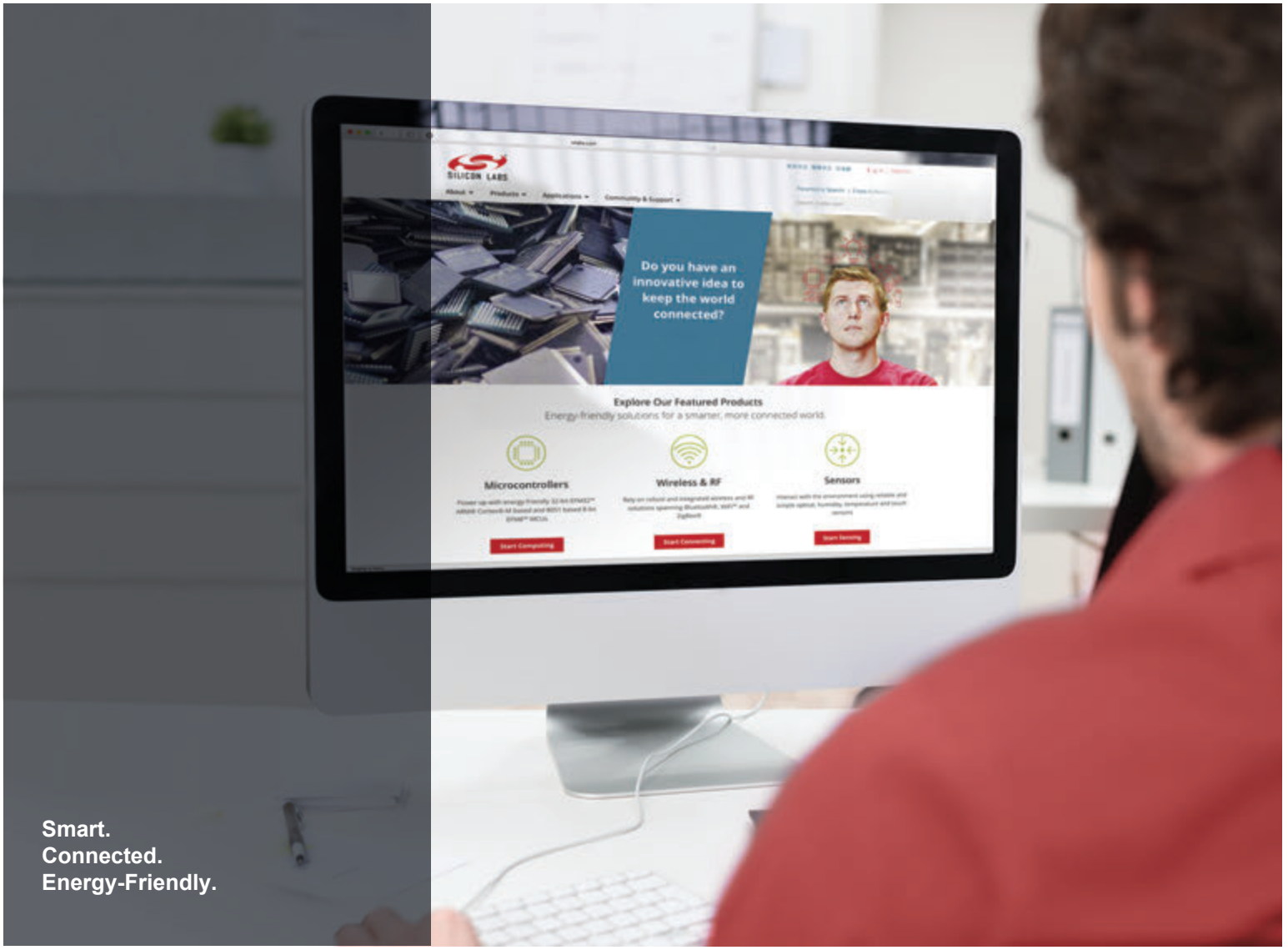
October 2018

- Added INT_E101

Revision 0.1

September 2018

- Initial release.



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