SiWG917 SoC Errata

This document contains information on the SiWG917 SoC Errata. The latest available revision of this device is revision B. Errata that have been resolved remain documented and can be referenced for previous revisions of this device. The device datasheet explains how to identify the chip revision either from the package marking or electronically.

Errata effective date: June **TBD**, 2025.

Errata Summary

Designator	Title/Problem	Workarounds	Exists on Revision A	Exists on Revision B
OSC_32kHz_E301	Recommendation for an external XTAL as a mandatory requirement	No	X	X
OSC_32kHz_E302	Device hangs on application reset and after FW upgrade by commander	Yes	X	X
OSC_32kHz_E303	Calendar Timer is inaccurate	No	X	X
EXIP_E301	Devices with a certain eFuse configuration cannot support encrypted XiP for Cortex-M4	No	X	X
EXIP_E302	Encrypted XiP for Cortex-M4 disabled in default MBR configuration flash for SoC OPNs with in-package flash	No	X	X
CONFIG_TIMER_E301	32-bit State Configurable Timer option removed from the datasheet	No	X	X

1. OSC_32kHz_301: Recommendation for External XTAL as Mandatory Requirement

Description

The SiWG917 datasheet 0.7 and earlier revisions provide options for two types of external clock, an external 32 kHz oscillator or an external 32 kHz XTAL. In future revisions of the datasheet, an external 32 kHz XTAL will be mandatory for Wi-Fi, BLE, and Coex Power saving use-cases and ULP MCU applications with accurate timing requirements.

Affected Condition/Impacts

Timing accurate ULP MCU applications and wireless power consumption will be impacted.

Workaround

No workaround available.

Resolution

Hardware Design Change: Use an external 32 kHz XTAL for high timing accuracy use-case on pins XTAL_32KHz_P and XTAL_32KHz_N.

2. OSC_32kHz_302: Device Hangs on Application Reset and After FW Upgrade by Commander

Description

When the SiWG917 is designed with an external 32 kHz oscillator connected to the UULP_VBAT_GPIO_3 pins and used with SW SDK versions 3.3.2 or before, hardware hang issues have been observed during the FW update via Simplicity Commander or programmatic reset by applications.

Affected Condition/Impacts

The SiWG917 will hang and will not reset after FW upgrade via JTAG or Serial Wire Debug (SWD), or application-based reset.

Workaround

In the affected condition, the device will need an externally triggered power cycle or hard reset (POC_IN).

Resolution

This issue is resolved by upgrading to the latest SiSDK (with WiSeConnect SDK 3.3.4 or above) and Commander version 1.17.0 or above.

3. OSC_32kHz_303: ULP MCU Calendar Peripheral is Inaccurate

Description

When the SiWG917 is designed with an external 32 kHz oscillator connected to the UULP_VBAT_GPIO_3 pin, the ULP MCU Calendar peripheral is inaccurate.

Affected Condition/Impacts

The device cannot maintain accurate real-time calendar for MCU applications.

Workaround

No workaround available.

Resolution

Hardware Design Change: Use a 32 kHz XTAL for high timing accuracy use-case on pins XTAL_32KHz_P and XTAL_32KHz_N.

4. EXIP_301 – Devices with a Certain eFuse Configuration cannot Support Encrypted XiP for Cortex-M4

Description

eFuse configuration has a bit called disable_m4_kh_access which disables encrypted XiP for M4. This bit is set to 1 by default. However, if this configuration is programmed in the OTP of the device for the OPNs listed below, it cannot be set to 0 and causes Encrypted XiP of Cortex-M4 to be permanently disabled.

Affected Condition/Impacts

SoC devices with date code 2440 or earlier where this eFuse configuration is programmed in OTP will be impacted.

OPNs:

- SIWG917M141XGTBA
- SIWG917M141XGTBAR
- SIWG917M121XGTBA
- SIWG917M121XGTBAR
- SIWG917M111XGTBA
- SIWG917M111XGTBAR

Workaround

No workaround available.

Resolution

Devices manufactured with date code 2441 and above will have this bit set to 0. Contact Silicon Labs if your application is using Encrypted XiP and you have parts with affected date codes.

5. EXIP_302 – Encrypted XiP for Cortex-M4 Disabled in Default MBR Configuration Flash for SoC OPNs with In-Package Flash

Description

MBR configuration has a bit called disable_m4_kh_access which disables encrypted XiP for M4. This bit is set to 1 by default in the MBR on the flash of the device for the listed OPNs below.

Affected Condition/Impacts

SoC devices where default MBR configurations are programmed in flash will be impacted in the execution of Cortex-M4 applications with encryption.

OPNs:

- SIWG917M111MGTBA
- SIWG917M111MGTBAR
- SIWG917M110LGTBA
- SIWG917M110LGTBAR
- SIWG917M100MGTBA
- SIWG917M100MGTBAR

Workaround

No workaround available.

Resolution

Simplicity Commander version 1.17.3 and beyond can clear encrypted XiP bit in MBR while enabling SiWG917 security configurations automatically to resolve the issue.

6. CONFIG_TIMER_E301 – 32-bit State Configurable Timer option removed from the datasheet

Description

The 32-bit configuration timer option for State Configurable Timer (SCT) is not supported and has been removed from the device data sheet. Only Dual 16-bit timer operation is supported.

Affected Condition/Impacts

All SoC OPNs with MCU applications that utilize SCT are impacted.

Workaround

No workaround available.

Resolution

No resolution is available.

7. Revision History

Revision 0.3

July, 2025

- Added 6. CONFIG_TIMER_E301 – 32-bit State Configurable Timer option removed from the datasheet.

Revision 0.2

February, 2025

- Added 4. EXIP_301 – Devices with a Certain eFuse Configuration cannot Support Encrypted XiP for Cortex-M4.
- Added 5. EXIP_302 – Encrypted XiP for Cortex-M4 Disabled in Default MBR Configuration Flash for SoC OPNs with In-Package Flash.

Revision 0.1

December, 2024

- Initial release.

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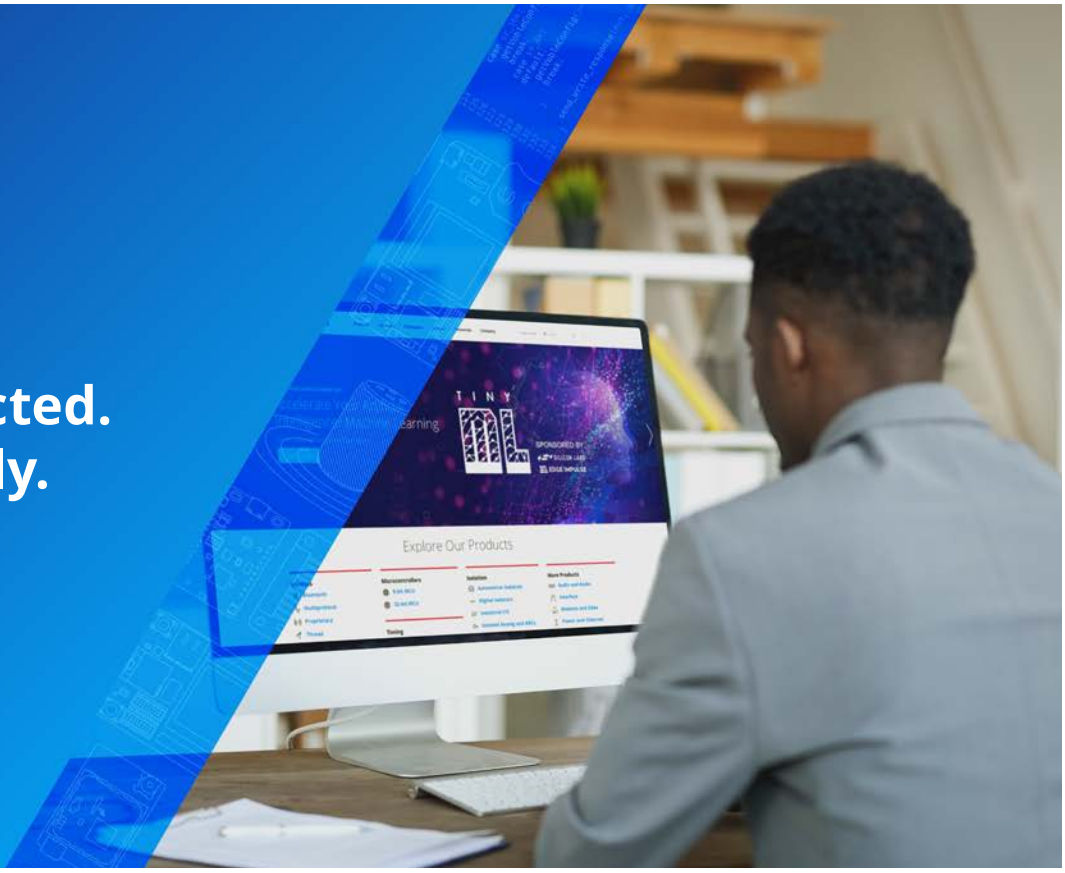

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