

# SiWG917 SoC Errata

This document contains information on the SiWG917 SoC Errata. The latest available revision of this device is revision B. Resolved errata remain documented as reference for previous revisions of this device. The device data sheet explains how to identify the chip revision either from the package marking or electronically.

Errata effective date: March 25, 2026.

## Errata Summary

Designator	Title/Problem	Workarounds	Exists on Revision A	Exists on Revision B
OSC_32kHz_E301	Recommendation for an external XTAL as a mandatory requirement	No	X	X
OSC_32kHz_E302	Device hangs on application reset and after FW upgrade by commander	Yes	X	X
OSC_32kHz_E303	Calendar Timer is inaccurate	No	X	X
EXIP_E301	Devices with a certain eFuse configuration cannot support encrypted XiP for Cortex-M4	No	X	X
EXIP_E302	Encrypted XiP for Cortex-M4 disabled in default MBR configuration flash for SoC OPNs with in-package flash	No	X	X
CONFIG_TIMER_E301	32-bit State Configurable Timer option removed from the data sheet	No	X	X
ANTIROLLBACK_E301	Anti-rollback functionality requires M4 firmware version must be same or greater than NWP firmware version	No	X	X
DCACHE_E301	PSRAM Data Corruption whenever D-Cache is Enabled	Yes	X	X
GPIO_TIMESTAMP_E301	GPIO Timestamp removed from the data sheet	No	X	X

## 1. OSC\_32kHz\_301: Recommendation for External XTAL as Mandatory Requirement

### Description

The SiWG917 data sheet revision 0.7 and earlier provide options for two types of external clocks, an external 32 kHz oscillator or an external 32 kHz XTAL. In future revisions of the data sheet, an external 32 kHz XTAL will be mandatory for Wi-Fi, BLE, and Coex Power saving use cases and ULP MCU applications with accurate timing requirements.

### Affected Condition/Impacts

Timing accurate ULP MCU applications and wireless power consumption will be impacted.

### Workaround

No workaround available.

### Resolution

**Hardware Design Change:** Use an external 32 kHz XTAL for high-accuracy timing use cases on pins XTAL\_32KHz\_P and XTAL\_32KHz\_N.

## 2. OSC\_32kHz\_302: Device Hangs on Application Reset and After FW Upgrade by Commander

### Description

When the SiWG917 is designed with an external 32 kHz oscillator connected to the UULP\_VBAT\_GPIO\_3 pins and used with SW SDK versions 3.3.2 or before, hardware hang issues have been observed during the FW update via Simplicity Commander or programmatic reset by applications.

### Affected Condition/Impacts

The SiWG917 will hang and will not reset after FW upgrade via JTAG or Serial Wire Debug (SWD), or application-based reset.

### Workaround

In the affected condition, the device will need an externally triggered power cycle or hard reset (POC\_IN).

### Resolution

This issue is resolved by upgrading to the latest SiSDK (with WiSeConnect SDK 3.3.4 or above) and Commander version 1.17.0 or above.

### 3. OSC\_32kHz\_303: ULP MCU Calendar Peripheral is Inaccurate

#### Description

When the SiWG917 is designed with an external 32 kHz oscillator connected to the UULP\_VBAT\_GPIO\_3 pins, the ULP MCU Calendar peripheral is inaccurate.

#### Affected Condition/Impacts

The device cannot maintain an accurate real-time calendar for MCU applications.

#### Workaround

No workaround available.

#### Resolution

**Hardware Design Change:** Use a 32 kHz XTAL for high-accuracy timing use cases on pins XTAL\_32KHz\_P and XTAL\_32KHz\_N.

## 4. EXIP\_301 – Devices with a Certain eFuse Configuration cannot Support Encrypted XiP for Cortex-M4

### Description

eFuse configuration has a bit called `disable_m4_kh_access` which disables encrypted XiP for M4. This bit is set to 1 by default. However, if this configuration is programmed in the OTP of the device for the OPNs listed below, it cannot be set to 0 and causes Encrypted XiP of Cortex-M4 to be permanently disabled.

### Affected Condition/Impacts

SoC devices with date code 2440 or earlier where this eFuse configuration is programmed in OTP will be impacted.

OPNs:

- SIWG917M141XGTBA
- SIWG917M141XGTBAR
- SIWG917M121XGTBA
- SIWG917M121XGTBAR
- SIWG917M111XGTBA
- SIWG917M111XGTBAR

### Workaround

No workaround available.

### Resolution

Devices manufactured with date code 2441 and above will have this bit set to 0. Contact Silicon Labs if your application is using Encrypted XiP and you have parts with affected date codes.

## 5. EXIP\_302 – Encrypted XiP for Cortex-M4 Disabled in Default MBR Configuration Flash for SoC OPNs with In-Package Flash

### Description

MBR configuration has a bit called `disable_m4_kh_access` which disables encrypted XiP for M4. This bit is set to 1 by default in the MBR on the flash of the device for the listed OPNs below.

### Affected Condition/Impacts

SoC devices where default MBR configurations are programmed in flash will be impacted in the execution of Cortex-M4 applications with encryption.

OPNs:

- SIWG917M111MGTBA
- SIWG917M111MGTBAR
- SIWG917M110LGTBA
- SIWG917M110LGTBAR
- SIWG917M100MGTBA
- SIWG917M100MGTBAR

### Workaround

No workaround available.

### Resolution

Simplicity Commander version 1.17.3 and beyond can clear encrypted XiP bit in MBR while enabling SiWG917 security configurations automatically to resolve the issue.

## 6. CONFIG\_TIMER\_E301 – 32-bit State Configurable Timer option removed from the data sheet

### Description

The 32-bit configuration timer option for State Configurable Timer (SCT) is not supported and has been removed from the device data sheet. Only Dual 16-bit timer operation is supported.

### Affected Condition/Impacts

All SoC OPNs with MCU applications that utilize SCT are impacted.

### Workaround

No workaround available.

### Resolution

No resolution is available.

## 7. ANTIROLLBACK\_E301 – Anti-rollback functionality requires M4 firmware version must be same or greater than NWP firmware version

### Description

Whenever the anti-rollback settings for both M4 and NWP are programmed through eFuse, the bootloader requires that the M4 firmware version must be equal to or higher than the NWP firmware version.

This restriction does not apply whenever anti-rollback settings for both M4 and NWP are programmed through MBR.

### Affected Condition/Impacts

All SoC OPNs are impacted.

### Workaround

No workaround available.

### Resolution

Keep M4 firmware version greater than or equal to NWP firmware version.

## 8. DCACHE\_E301 – PSRAM Data Corruption whenever D-Cache is Enabled

### Description

When PSRAM is used with Data Cache (D-cache) enabled, incorrect data may be returned under a specific back-to-back memory access sequence.

The Cortex-M4 processor accesses PSRAM through the D-cache → AHB → QSPI path. The D-cache line size is 32 bytes and operates in write-through mode.

The issue is observed under the following conditions:

- PSRAM is configured in memory-mapped mode
- D-cache is enabled
- An incremental (INCR) write is immediately followed by a wrap (WRAP) read
- No wait cycles occur between transactions

The QSPI controller may not correctly reset the burst-mode state between transactions. As a result, a cache-line fill that should occur in WRAP mode may instead execute in INCR mode. If the read begins at a non-zero offset within a 32-byte cache line, incorrect partial cache-line data may be returned.

This issue is limited to memory-mapped PSRAM accesses through the D-cache line fill path.

### Affected Condition/Impacts

All SoC OPNs using PSRAM with D-cache enabled are impacted.

### Workaround

Disable D-cache in Software to avoid corruption in WiSeConnect SDK releases before v4.0.0.

**Option 1:** Upgrade to WiSeConnect SDK v4.0.0 or 4.0.1 (whenever available) to disable cache allocation for PSRAM accesses that avoids the QSPI WRAP burst corruption issue.

**Option 2:** Upgrade to WiSeConnect SDK v4.0.2 or later versions whenever available, to completely disable D-Cache.

**Option 3:** For older WiSeConnect SDKs prior to v4.0.0.

- Update `sl_si91x_psrainit()` and `rsi_d_cache_invalidate_all()` functions by adding the following code snippet at the end of each of these function to disable the D-Cache path for PSRAM.

```
// Disable D-Cache allocation for the PSRAM
DCACHE_CTRL_AND_STATUS &= ~(HPORT_ALLOCATE_SIGNAL);
```

- The following macros must be added to `rsi_d_cache.h` file.

```
// D-Cache Control and Status Register
#define DCACHE_CTRL_AND_STATUS (*(uint32_t volatile *) (0x460081F8))

// This is BIT(10) in D-Cache Control and Status Register using to disable D-Cache Allocate signal
#define HPORT_ALLOCATE_SIGNAL 0x400
```

### Resolution

No resolution is available. Use the documented software workaround to disable D-Cache for PSRAM.

## 9. GPIO\_TIMESTAMP\_E301 – GPIO Timestamp removed from the data sheet

### Description

GPIO Timestamp (also called as “Timestamping Controller”) is not supported and has been removed from the device data sheet.

### Affected Condition/Impacts

All SoC OPNs with MCU applications that utilize GPIO Timestamp are impacted.

### Workaround

No workaround available.

### Resolution

No resolution is available.

## 10. Revision History

### Revision 0.4

March, 2026

- Added 7. [ANTIROLLBACK\\_E301](#) – Anti-rollback functionality requires M4 firmware version must be same or greater than NWP firmware version.
- Added 8. [DCACHE\\_E301](#) – PSRAM Data Corruption whenever D-Cache is Enabled.
- Added 9. [GPIO\\_TIMESTAMP\\_E301](#) – GPIO Timestamp removed from the data sheet.
- Minor text revisions: updated wording and sentence structure for clarity.

### Revision 0.3

July, 2025

- Added 6. [CONFIG\\_TIMER\\_E301](#) – 32-bit State Configurable Timer option removed from the data sheet.

### Revision 0.2

February, 2025

- Added 4. [EXIP\\_301](#) – Devices with a Certain eFuse Configuration cannot Support Encrypted XiP for Cortex-M4.
- Added 5. [EXIP\\_302](#) – Encrypted XiP for Cortex-M4 Disabled in Default MBR Configuration Flash for SoC OPNs with In-Package Flash.

### Revision 0.1

December, 2024

- Initial release.

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