SiWG917 SoC Module Errata

This document contains information on the SiWG917 SoC Module Errata. The latest available revision of this device is revision B. Errata that has been resolved remain documented and can be referenced for previous revisions of this device. The device data sheet explains how to identify the chip revision from the package marking.

Errata effective date: August 8, 2025.

Errata Summary

Designator	Title/Problem	Workarounds	Exists on Revision A	Exists on Revision B
OSC_32KHz_E401	Recommendation for external oscillator as mandatory requirement	No	X	X
OSC_32KHz_E402	Device hangs on application reset and after FW upgrade by commander	Yes	X	X
OSC_32KHZ_E403	Calendar time is inaccurate	No	X	X
EXIP_E401	Devices with a certain eFuse configuration programmed in OTP memory cannot support Encrypted XiP for Cortex-M4	No	X	X
CONFIG_TIMER_E401	32-bit state configurable timer option removed from the data sheet	No	X	X

1. OSC_32 kHz_401: Recommendation for an External Oscillator as Mandatory Requirement

Description of Errata:

SiWG917 Module Data Sheet 0.5 and earlier provides an option for an external 32 kHz Oscillator on pin UULP_VBAT_GPIO_3. In future revisions of the data sheet, this external 32 kHz Oscillator will be mandatory for Wi-Fi, BLE, and Co-Ex power saving use cases and high accuracy MCU applications.

Affected Condition/Impacts:

Timing accurate ULP MCU applications and low power wireless use cases (Wi-Fi, BLE, and Co-Ex) will be impacted.

Workaround:

No available workaround.

Resolution:

Hardware Design Change- Use an external 32 kHz Oscillator on pin UULP_VBAT_GPIO_3 for high timing accuracy use cases.

2. OSC_32 kHz_402: Device Hangs on Application Reset and after FW Upgrade by Commander

Description of Errata:

When the SiWG917 module is designed with an external 32 kHz oscillator connected to the UULP_VBAT_GPIO_3 pins and used with SW SDK versions 3.3.2 or before, hardware hang issues have been observed during FW Update via Simplicity Commander or programmatic reset by applications.

Affected Condition/Impacts:

SiWG917 Module will hang and will not reset after FW upgrade via JTAG or Serial Wire Debug (SWD), or application-based reset.

Workaround:

In the affected condition, the device will need an externally triggered power cycle or hard reset (POC_IN).

Resolution:

This issue is resolved by upgrading to the latest SiSDK (with SDK 3.3.4 or later) and Commander version 1.17.0 or above.

3. OSC_32 kHz_403: ULP MCU Calendar Peripheral is Inaccurate

Description of Errata:

When SiWG917 module is designed with an external 32 kHz oscillator connected to UULP_VBAT_GPIO_3 pin, ULP MCU Calendar peripheral is inaccurate.

Affected Condition/Impacts:

Device cannot maintain accurate real-time calendar for MCU applications.

Workaround:

No available workaround.

Resolution:

No available resolution yet.

4. EXIP_E401: Devices with a Certain eFuse Configuration cannot Support Encrypted XiP for Cortex-M4

Description of Errata:

eFuse configuration has a bit called disable_m4_kh_access which disables encrypted XiP for Cortex-M4. This bit is set to 1 by default. However, if this configuration is programmed in the OTP of the device for the listed OPNs below, it cannot be set to 0 and causes Encrypted XiP of Cortex-M4 to be permanently disabled.

Affected Condition/Impacts:

SoC mode modules with date code 2414-2452 where this eFuse configuration is programmed in OTP will be impacted.

OPNs:

- SIWG917Y110LGABA
- SIWG917Y110LGABAR
- SIWG917Y110LGNBA
- SIWG917Y110LGNBAR
- SIWG917Y111MGABA
- SIWG917Y111MGABAR
- SIWG917Y111MGNBA
- SIWG917Y111MGNBAR
- SIWG917Y121MGABA
- SIWG917Y121MGABAR
- SIWG917Y121MGNBA
- SIWG917Y121MGNBAR
- SIWG917YXZ113ABA
- SIWG917YXZ113ABAR
- SIWG917YXZ115NBA
- SIWG917YXZ115NBAR

Workaround:

No available workaround.

Resolution:

Devices manufactured with date code 2504 and above will have this bit set to 0. Contact Silicon Labs if your application is using Encrypted XiP and you have parts with affected date codes.

5. CONFIG_TIMER_E401: 32-bit State Configurable Timer Option Removed from the Data Sheet

Description of Errata:

The 32-bit configuration timer option for the State Configurable Timer (SCT) is not supported and has been removed from the device data sheet. Only the Dual 16-bit timer operation is supported.

Affected Condition/Impacts:

All SoC OPNs with MCU applications that utilize SCT are impacted.

Workaround:

No available workaround.

Resolution:

No resolution is available.

6. Revision History

Revision 0.3

August, 2025

- Added 5. CONFIG_TIMER_E401: 32-bit State Configurable Timer Option Removed from the Data Sheet

Revision 0.2

February, 2025

- Added 4. EXIP_E401: Devices with a Certain eFuse Configuration cannot Support Encrypted XiP for Cortex-M4

Revision 0.1

December, 2024

- Initial release.

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