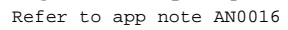


Refer to app note AN0002



Pin configuration diagram for the P1 header. The header is a 2x10 pin connector. Pin 1 is labeled VMCU. Pin 2 is labeled 2. Pin 3 is labeled 3. Pin 4 is labeled 4. Pin 5 is labeled 5. Pin 6 is labeled 6. Pin 7 is labeled 7. Pin 8 is labeled 8. Pin 9 is labeled 9. Pin 10 is labeled 10. Pin 11 is labeled 11. Pin 12 is labeled 12. Pin 13 is labeled 13. Pin 14 is labeled 14. Pin 15 is labeled 15. Pin 16 is labeled 16. Pin 17 is labeled 17. Pin 18 is labeled 18. Pin 19 is labeled 19. Pin 20 is labeled 20. The diagram shows connections for DBG\_SWIO, DBG\_SWCLK, DBG\_SWO, and MCUDBG\_#RESET to pins 9, 10, 11, and 12 respectively. The VMCU signal is connected to pin 1. The GND signal is connected to pin 20. The header is labeled P1 and HEADER\_2X10\_2.54MM\_TH.