# Table of Contents

## Design and Layout
- Exposed Ground Pin ......................................................... 5
- Synthesizer Loop Structure ........................................... 5
- Synthesizer Selection Guide ........................................... 5
- QFN Recommended Land Pattern ....................................... 5
- Synthesizer Output Buffer Circuit Model ............................. 5
- Unused Inductor Terminals .............................................. 6
- Unused power and ground pins ......................................... 6
- Layout considerations ..................................................... 6
- RF shielding ...................................................................... 6
- Frequency reference source recommendations ..................... 6
- Frequency reference source sharing ................................... 7
- Synthesizer power supply .................................................. 7
- Frequency reference source waveform ................................. 7
- XIN input impedance ........................................................ 7
- Tuning inductor Q-factor .................................................... 7
- Extending the ±5% tuning range ......................................... 7
- Extending the ±5% tuning range for a specific device .......... 8
- Extending the ±5% tuning range using external circuitry .... 8
- Si4133 RF1 VCO extended tuning range ............................... 8
- Maximum update rate ....................................................... 8
- External modulation .......................................................... 8
- Military applications ....................................................... 8

## Operation
- Synthesizer Power Consumption ......................................... 9
- Synthesizer powerup default states ..................................... 9
- Powerup and powerdown modes ......................................... 9
- Programming in powerup or powerdown modes ..................... 9
- Causes of loss-of-lock ....................................................... 9
- Triggering self-tuning ...................................................... 9
- Self-tuning algorithm ...................................................... 9
- Self-tuning phase/frequency transients ............................... 9
- Self-tuning phase/frequency transients predictability .......... 10
- Reducing self-tuning phase/frequency transients ................ 10
- Disabling self-tuning ...................................................... 10
- Self-tuning with two active PLLs ..................................... 10
- LDETB with two active PLLs ............................................ 10
Design and Layout

Q: Can the ground paddle in the QFN package be left floating?
A: Yes, but we recommend it be grounded to guarantee performance.

Q: Is the synthesizer loop a Type I or Type II?
A: Type I.

Q: Is there a Synthesizer selection guide available?

Q: What is the recommended PCB footprint for the QFN packages?
A:

Q: What is the equivalent circuit model for RFOUT and IFOUT?
A:

Approximate Si4133 and Si4133G Output Network, QFN and TSSOP Package

QFN:
- RF1 and RF2 Synthesizers
  - R1 = 200 Ω
  - C1 = 1.25 pF
  - R2 = 0 Ω
  - C2 = 0 pF
  - L_{bond} = 3.5 nH
- IF Synthesizers
  - R1 = 100 Ω
  - C1 = 1 pF
  - R2 = 50 Ω
C2 = 0.25 pF  
L_{bond} = 3.5 nH  

**TSSOP:**  
- RF1 and RF2 Synthesizers  
  R1 = 200 Ω  
  C1 = 1.25 pF  
  R2 = 0 Ω  
  C2 = 0 pF  
  L_{bond} = 7 nH  
- IF Synthesizers  
  R1 = 100 Ω  
  C1 = 1 pF  
  R2 = 50 Ω  
  C2 = 0.25 pF  
  L_{bond} = 7 nH  

**Q:** Should unused RF/IF PLL tuning inductor terminals be left floating?  
**A:** Unused inductor terminals can be left floating. A conservative approach is to ground the unused inductor terminals so as to minimize noise pick-up, especially in noisy environments. If the unused inductor terminals of a PLL are connected to ground, the PLL should NOT be turned on since this might damage the device.  

**Q:** Should the power and ground terminals of unused PLLs be left floating or unconnected?  
**A:** No. If a PLL will not be utilized, its power and ground terminals should still be connected to power and ground respectively. If only one PLL is required for your application, consider using the various synthesizer derivative devices. Information about the available derivative devices is located on the back of the synthesizer device data sheets.  

**Q:** Does the synthesizer have any special layout considerations?  
**A:** For synthesizers requiring external inductances, refer to "AN31: Inductor Design for the Si41xx Synthesizer Family" for details on how to implement the external inductors. A rule of thumb is to use discrete inductors if the required external inductance is greater than 3 nH.  
Inductance values for chip inductors progress in discrete steps. To implement specific inductances therefore, a combination of both PCB and trace inductances may be required.  
Precautions should be taken to isolate the reference frequency input trace, the RF output traces, and the inductor traces from potential sources of interference or coupling. The Si4133/33G-EVB data sheet contains layouts for various evaluation boards.  
Good grounding techniques should be employed to minimize unwanted signal coupling. This involves ensuring that each RF signal has a continuous ground return path back to its source. The return path should closely follow the sourcing signal’s trace. For QFN packages, connect the ground paddle located in the center of the package to PCB ground. The VDD supply of the synthesizer should be locally bypassed as close to the part as possible. Refer to the "Typical Applications Circuit" diagram in the synthesizer device data sheet for the recommended bypass capacitance.  

**Q:** Is shielding required or recommended when using the synthesizers?  
**A:** It is recommended that shielding be used. If the synthesizer is used in a noisy environment, it is possible for the surrounding noise to couple into the tuning LC tank circuit. This could result in the output of the synthesizer being modulated with the surrounding noise. Additionally, the fields present in the LC tank circuit might couple into a nearby circuit and affect it.  

**Q:** Does Silicon Laboratories recommend any frequency reference sources?  
**A:** The best performance is obtained when temperature compensated crystal oscillators (TCXOs) are used for the reference. Examples of such TCXOs include Kyocera's KT18 series, Toyocom TCO-9131 series and Raltron RTVY-124 series.
Q: Can the reference source be used to provide a reference signal to more than one synthesizer?

A: Two or more synthesizers can share the same reference source if the reference source has enough drive capability. In other words, the reference source should possess sufficient voltage and current levels to drive all the synthesizers.

It is important to note that powering any of the individual synthesizers up or down will result in impedance changes at the XIN input. As such, transients may be present at the reference source output (and therefore at the other synthesizer XIN inputs) during such instances. These transients may show up as phase noise at the synthesizer outputs. If an application is sensitive to such transients, buffers can be used to isolate the reference source output from each of the XIN inputs.

Q: Are separate power supplies required in applications with more than one synthesizer?

A: Separate power supplies are not required if each synthesizer contains the recommended bypass capacitors for power supply filtering. Refer to the "Typical Applications Circuit" diagram in the synthesizer device data sheet for the recommended bypass capacitance. The bypass capacitors should be located next to the package. As a general layout precaution, good grounding techniques should be employed to minimize unwanted signal coupling.

Q: Should the reference source have a sine wave or a square wave output?

A: The reference source can have either a square wave or sine wave output. The reference amplifier has a large gain that converts the incoming sine wave to a square wave. Therefore, both sine and square wave references are processed identically.

Q: What is the impedance looking into XIN input?

A: As the equivalent circuit below shows, the XIN input is effectively an RC circuit consisting of a 500 Ω resistor and 5 pF capacitor in series.

Q: What is the recommended minimum quality factor (Q-factor) for the discrete tuning inductor?

A: The discrete inductor should be selected such that the Q-factor is greater than 40. For better phase noise performance, inductors with Q-factors greater than 50 should be utilized. In general, higher Q-factors for the tuning inductors will lead to better phase noise.

Q: Is it possible to increase the frequency generation range beyond ±5%?

A: This may be possible depending on the tolerance of the tuning inductor. Also, it may require the use of more than one PLL. The ±5% tuning range is designed to compensate for tuning inductor tolerances of up to ±10%. Therefore, if the synthesizer is used with a tuning inductor whose tolerance is ±10%, the entire ±5% tuning range will be used to compensate for the tuning inductor variation.

On the other hand, if an external inductor with a tolerance of ±2% is used, approximately ±1% of the tuning range will be used to compensate for the variation of the inductor. The rest of the tuning range (approximately ±4%) can then be used for frequency generation.

Using more than one PLL can reliably extend the frequency range. For example, the RF1 and RF2 PLLs of the Si4133 can be used, with the PLLs assigned to different but slightly overlapping bands. The tuning inductor tolerances must be taken into account.

For all applications (especially those requiring generation of a range of frequencies), always ensure that the
tolerance of the tuning inductor is taken into account. This is an important step in guaranteeing a good manufacturing yield.

**Q:** The PLL I am using has a tuning range larger than ±5%. Can I use this larger range in my application?

**A:** This is not recommended and should only be done after extensive experimentation. The ±5% tuning range is designed to compensate for tuning inductor variations and provide sufficient margin for PCB manufacturing process variations. Therefore, the tolerance of the tuning inductor should always be taken into account. Ranges as large as ±12% have been observed during laboratory experiments. However, such large ranges cannot be guaranteed due to concerns about changes in the operating conditions (temperature, supply voltage, etc.) as well as the tolerance of the tuning inductor.

**Q:** Is it possible to extend the synthesizer frequency generation range beyond ±5% using switches in conjunction with various tuning inductors?

**A:** This is not recommended. Such an arrangement can result in an increase of the series resistance of the tuning inductance. A higher series resistance can lead to a lower Q-factor or poor VCO performance.

**Q:** There appears to be a “dead-zone” between the Si4133 RF1 VCO’s normal and extended tuning ranges. What is the effect of operating the RF1 VCO in this range?

**A:** The Si4133 RF1 VCO data sheet limits are 900–1806 MHz and 1850–2050 MHz for the normal and extended frequency operations, respectively. Operation in the 1806–1850 MHz range is possible. However, this range falls outside the guaranteed data sheet specifications. The device should be used in the extended frequency mode. Also, only the QFN package should be used. The extended frequency operation is implemented by setting the D1 bit of the main configuration register to 1 and setting VDD to between 3.0 and 3.6 V. For more details, refer to “AN41: Extended Frequency Operation of Silicon Laboratories Radio Frequency Synthesizers” and “AN31: Inductor Design for the Si41xx Synthesizer Family”.

**Q:** How do I determine the maximum update rate for my application?

**A:** The required channel spacing and choice of reference frequency limit the maximum update rate. The channel spacing resolution is equal to the update rate. Therefore, the update rate cannot exceed the required channel resolution. Since the R and N dividers are both integer dividers, the maximum update rate is the greatest common divisor of the reference frequency and required output frequency. If the maximum update rate for your application is being limited by the reference frequency, consider using a different reference frequency. Please note that in general, a higher update rate leads to better phase noise performance.

**Q:** Can the synthesizer support external modulation?

**A:** Modulation of the synthesizer is not recommended as it may result in a reduced operating range for the device. The synthesizer is designed to lock to a ±0.5% range after calibration (or self-tuning) to correct for temperature drifts. If a portion of the ±0.5% tuning range is used for modulation, the temperature range of the synthesizer will decrease by that portion. Rudimentary frequency modulation can be implemented by modulating the reference source. This implementation is limited as described above. Amplitude modulation cannot be implemented using the synthesizers.

**Q:** Can the Silicon Laboratories synthesizers be used for military applications?

**A:** Silicon Laboratories synthesizers can be used for military applications as long as the operational environment and test conditions do not exceed those specified in the synthesizer device data sheets.
Operation

Q: **What is the typical power consumption of the synthesizer?**

A: For the Si4133, when RF and IF are operating, typical current is 18 mA. (See device data sheet, Table 3.) To calculate power consumption, multiply the current by the operating voltage. Typical power consumption is 3.0 V x 18 mA = 54 mW

When the synthesizer is powered down, typical current consumption is approximately 1 µA and power consumption is 3 µW.

Q: **What is the initial state of the synthesizer when power is applied?**

A: The synthesizer registers do not have a definite start-up mode. Therefore, all the appropriate registers should be programmed after power is applied to the device.

Q: **What determines the powerup and powerdown operational modes in the synthesizer?**

A: The synthesizer is in powerup mode when the PWDN pin is held HIGH. When the PWDN is LOW, the synthesizer is in powerdown mode. In powerdown mode, the synthesizer draws very little current (on the order of 1 µA). Please note that in both the powerup and powerdown modes, the supply voltage must still be applied to the device.

Q: **Can the synthesizer registers be programmed in both the powerup and powerdown modes?**

A: Yes. The synthesizer registers can be programmed with the device in either the powerup or powerdown modes as long as the supply voltage is present. Transitions between the powerup and powerdown modes will not affect the register contents.

Q: **What conditions can cause the synthesizer to lose lock?**

A: The conditions that can trigger a loss of lock in the synthesizer include the following:

- A temperature drift in excess of ±30 °C after the self-tuning algorithm has been run. (For the Si4133W, a wider -50 °C to 80 °C temperature range is applicable)
- The reference source being turned off.
- A large change in the operating conditions. For example, a change in the reference source frequency larger than ±0.5%.

If the synthesizer does not function normally after the initial power up, ensure that all the registers are correctly programmed.

Q: **What conditions will trigger the self-tuning mechanism of the synthesizer?**

A: Any of the following conditions will initiate the self-tuning algorithm:

- Powering up the device (or power-cycling the device).
- Powering up the individual PLLs (through the PDIB or PDRB bits for instance).
- Toggling the PWDN pin LOW and then HIGH (a LOW corresponds to a powerdown state while a HIGH corresponds to a powerup state).
- Programming the N or R registers.

Q: **What role does the self-tuning algorithm play in the synthesizer PLLs?**

A: The algorithm is used to coarse tune the VCO such that it is within 1% of the desired output frequency. In so doing, the algorithm compensates for manufacturing tolerance errors in the value of the external inductor connected to the VCO. After the self-tuning process is complete, the PLL controls the VCO's oscillation frequency.

Q: **What is the frequency or phase transient on the synthesizer output during self-tuning?**

A: The output frequency can vary widely during self-tuning. The deviation can be as large as several MHz. If such transients are undesirable, the synthesizer output should be temporarily disconnected from its load. This can be accomplished by using a buffer for example.
Q: Do the phase and frequency transients present during self-tuning follow a predictable or reproducible path?
A: The phase/frequency trajectory followed by the synthesizer during the self-tuning varies each time the self-tuning algorithm is run. As such, the phase and frequency transients do not follow a predictable or reproducible path.

Q: Can the phase and frequency transients present during self-tuning be reduced or eliminated?
A: The phase and frequency transients present during self-tuning cannot be reduced or eliminated altogether. In applications where such transients are especially undesirable, buffers (that can be enabled and disabled) can be used to mask the transients from the synthesizer load.

Q: Can the self-tuning feature of the synthesizer be disabled?
A: The self-tuning mechanism cannot be disabled. The mechanism plays a very important role in correcting for both ambient temperature drifts and manufacturing variations.

Q: If both the IF PLL and one of the RF PLLs (either RF1 or RF2) are active, will reprogramming the N or R register of one of the PLLs result in both the active PLLs undergoing the self-tuning process?
A: No. Only the PLL whose N or R register values have been changed will undergo self-tuning. However, during power-up (both initial and transition from powerdown mode) both the active PLLs will undergo self-tuning.

Q: If both RF and IF PLLs are active, will the LDETB signal indicate an impending out-of-lock status if only one of the PLLs is about to lose lock?
A: Yes. If both PLLs are active, the LDETB signal can be thought of as an OR function of both the PLLs lock-detect status. In other words, if one of the active PLLs is about to lose lock, the LDETB signal will transition to a HIGH level to indicate the potential loss-of-lock.

Q: What is the recommended procedure for disabling the RF or IF PLLs?
A: The AUTOPDB bit should be set to 0. To disable the RF PLL, the PDRB bit should be set to 0. To disable the IF PLL, the PDIB bit should be set to 0. Setting the AUTOPDB bit to 1 overrides the individual PDIB and PDRB settings and enables both the RF and IF PLLs.

Q: In synthesizers containing both RF1 and RF2 PLLs, how is the active PLL determined?
A: The last N or R divider registers written into determines the active RF PLL. For example, if the R divider register for RF1 is programmed, the active RF PLL becomes RF1, and its output is available in the RFOUT output.

Q: What is the temperature window provided between the LDETB transition (to HIGH) and the actual loss of lock when a temperature drift occurs?
A: For the Si4136/26, Si4136XM and Si4133W, the temperature window (from LDETB transitioning to a HIGH to loss of lock) is on the order of 4 °C. The other synthesizers have a much narrower warning window. In some instances, the LDETB transition occurs almost simultaneously with, or is closely followed by, the loss of lock. In applications utilizing synthesizers with a narrow warning window, regular re-tuning of the PLL is recommended. This enables robust performance with minimal overhead.
Q: What are the ambient and lock temperature ranges of the Silicon Laboratories synthesizers?
A: The table below summarizes both the ambient and lock temperature ranges. The lock temperature range is formed around the ambient temperature in which the self-tuning algorithm is run.

<table>
<thead>
<tr>
<th>Device</th>
<th>Ambient Temperature Range ($T_A$)</th>
<th>Lock Maintenance Temperature Range</th>
<th>Large LDETB Warning Window</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si4113G-X5</td>
<td>−20 to +85 ºC</td>
<td>±30 ºC</td>
<td>No</td>
</tr>
<tr>
<td>Si4133/23/22/13/12</td>
<td>−40 to +85 ºC</td>
<td>±30 ºC</td>
<td>No</td>
</tr>
<tr>
<td>Si4133G/23G/22G</td>
<td>−20 to +85 ºC</td>
<td>±30 ºC</td>
<td>No</td>
</tr>
<tr>
<td>Si4133W</td>
<td>−25 to +85 ºC</td>
<td>−50 to +80 ºC</td>
<td>Yes</td>
</tr>
<tr>
<td>Si4126/36</td>
<td>−40 to +85 ºC</td>
<td>±30 ºC</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Q: Is the lock temperature range fixed or does it shift each time the synthesizer is retuned?
A: The lock maintenance range is centered on the ambient temperature in which the retuning or self-tuning algorithm is carried out. For instance, the Si4133 has a ±30 ºC lock maintenance range. If the self-tuning algorithm is carried out at 25 ºC, the Si4133 can maintain lock in the −5 to 55 ºC temperature range. If the self-tuning algorithm is carried out at 55 ºC on the other hand, the Si4133 can maintain lock in the 25 to 85 ºC temperature range.

Q: If loss-of-lock occurs due to a temperature drift, what is the state of the LDETB signal?
A: After a loss-of-lock has occurred, the LDETB signal will pulse HIGH and LOW continuously. The pulse rate is indeterminate. Therefore, if the LDETB signal is used for detecting a loss-of-lock condition, it should be continuously polled.

For devices with a large LDETB warning window, the LDETB signal is held HIGH prior to the loss-of-lock. In this case, the LDETB pulsing only occurs after the synthesizer has lost lock. The attached plots show the relationship between temperature drift and the LDETB signal for synthesizers.
Q: Can the LDETB signal function as a loss-of-signal (LOS) indicator?
A: No. The LDETB signal can only indicate LOS if the active PLL is already locked to the reference signal. In such an instance, the LDETB signal will transition to a HIGH state if the reference signal is withdrawn. However, if the PLL undergoes self-tuning in the absence of a reference signal, the state of the LDETB signal will be indeterminate.

Q: Can the LDETB signal be used to indicate that the PLL has settled to within 0.1 ppm of its final frequency?
A: No. The LDETB is also designed to provide an indication whether the active PLL is about to lose lock due to a temperature drift. Therefore, a HIGH LDETB signal can indicate either the PLL is in the process of achieving lock, or it is about to lose lock.

Q: How is extended frequency operation implemented on the Si4133?
A: To implement the extended frequency option, the RFLA and RFLB pins should be connected with the shortest trace possible. The extended frequency is available only for the QFN package of the Si4133 family. In addition, bit D1 of the main configuration register should be set to 1 and VDD set to between 3.0 and 3.6 V. For more details, refer to “AN41: Extended Frequency Operation of Silicon Laboratories Radio Frequency Synthesizers”.

Q: Are the RF and IF PLLs completely isolated?
A: There is an adequate amount of isolation between the RF and IF PLLs. However, if the RF VCO frequency is almost the same as the IF VCO frequency or its harmonics, interference might be observed. Frequency plans should be chosen with harmonic coupling of IF to RF in mind.
Manufacturing/Quality Control

Q: **What is the Lead Finish on the synthesizer package?**
   A: All of our synthesizer products are available in lead-free, RoHS-compliant packages. These parts have a 10 µm thick Matte Tin surface finish that is annealed for 1 hour at 150 °C to mitigate tin whisker formation. In addition, we continue to offer our synthesizers with a Sn85/Pb15 solder finish to support our customer’s legacy applications.

Q: **What is the Moisture Sensitivity Level (MSL) rating for the synthesizers?**
   A: All synthesizer models are MSL 3.

Q: **Is reliability data (FIT, MTBF, etc) for the synthesizer available?**
   A: Yes. Please contact Silicon Laboratories for the reliability data.
Serial Interface

Q: Does the synthesizer programmer work with both Windows2000 and Windows XP operating systems?

A: Yes. The latest programmer may be downloaded from our website http://www.silabs.com

Q: Can the synthesizer I/O pins be connected directly to a microcontroller?

A: Yes, but we recommend using pull-up resistors on the synthesizer serial lines. This will prevent the synthesizer from being programmed to an unknown state during microcontroller power-up.

Q: What is the minimum wait time between power-up and the first register write to the Synthesizer?

A: Registers may be written to the serial port once the supply voltage reaches the minimum supply voltage as specified in the data sheet. Ensure that the input voltage to the serial port does not exceed $V_{DD} + 0.3 \, V$ as specified in the data sheet.

Q: What is the serial interface and how does it function?

A: The serial interface is a simple 3-wire interface that is used to write into the registers required for normal synthesizer operation. The interface is made up of the clock (SCLK), data (SDATA) and write enable (SEN) signals. To commence writing into the synthesizer, the SEN signal is first transitioned to a LOW state and held there. The data present at the SDATA signal is then clocked into the synthesizer at the rising edges of the SCLK signal. To complete the writing operation, the SEN signal is transitioned to a HIGH state and held there.

In total, twenty-two (22) bits are required for each register write. The first eighteen (18) bits represent the data field while the next four (4) bits represent the address field. Both the data and address fields are clocked in MSB first. The synthesizer data sheets contain timing diagrams and details about the serial interface timing. Please note that a third party parallel port driver (DLPortIO) must be installed for the Silicon Laboratories synthesizer evaluation software to be functional. DLPortIO can be installed by running the port95nt.exe file, which is available for download along with the synthesizer evaluation board control software at www.silabs.com.

Q: What is the effect of shifting in more than 22 bits during a register write?

A: The synthesizer registers operate in a FIFO (First-In, First-Out) format. Therefore, if more than 22 bits are shifted in during a register write, only the last 22 bits will be captured in the register. If fewer than 22 bits are shifted in, the more significant portions of the register being written into will be loaded with contents previously loaded into the FIFO.

Q: Is it possible to program the synthesizer when the device is in powerdown mode?

A: Yes. The synthesizer can be programmed when the device is in powerdown mode.

Q: Can I use the synthesizer evaluation board software to configure and test a synthesizer mounted on my PCB?

A: Yes. However, it is important to note that the PC parallel port is a TTL (5 V) interface while the synthesizer has a 3 V interface. Therefore, a buffer/driver with level translation will be required. Device damage may occur if the synthesizer is connected directly to the parallel port.

Please note that a third party parallel port driver (DLPortIO) must be installed for the Silicon Laboratories synthesizer evaluation software to be functional. DLPortIO can be installed by running the port95nt.exe file, which is available for download along with the synthesizer evaluation board control software at www.silabs.com.
Q: **What is the pin mapping from the synthesizer evaluation board to the parallel port connector (DB25)?**

<table>
<thead>
<tr>
<th>Signal</th>
<th>DB25 pin #</th>
<th>JP1 pin # (Evaluation Board)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEN</td>
<td>2 (D0)</td>
<td>3</td>
</tr>
<tr>
<td>SDATA</td>
<td>3 (D1)</td>
<td>5</td>
</tr>
<tr>
<td>SCLK</td>
<td>4 (D2)</td>
<td>7</td>
</tr>
<tr>
<td>PWDN</td>
<td>6 (D4)</td>
<td>11</td>
</tr>
<tr>
<td>AUXOUT</td>
<td>11 (+Busy/S7-)</td>
<td>21</td>
</tr>
</tbody>
</table>

Q: **Are there specific requirements for the serial interface pins while the synthesizer is powering up?**

A: These pins should not be allowed to float or toggle during power up. As an example, toggling on the SEN pin can result in the synthesizer entering an unknown state.

Q: **Is it possible to read back the information stored in the tuning code registers of the synthesizer?**

A: The AUXOUT pin can be used to read the contents of the tuning code registers. This is especially useful if monitoring the frequency tuning margin on each unit in production is required. See the "Verifying Margin in Production" section in "AN31: Inductor Design for the Si41xx Synthesizer Family" for more details.
Phase Noise/Update Rate Effects

Q: What are the phase noise characteristics of the synthesizers?

A: The phase noise specifications for each synthesizer are contained in the respective device data sheets. For example, the typical phase noise of the Si4133 RF2 PLL operating at 1.2 GHz is ~134 dBc/Hz at a 1 MHz offset. The integrated phase error under the same conditions (from 10 Hz to 100 kHz) is 0.7 degrees rms.

Q: What are the factors that affect phase noise? Can phase noise be reduced?

A: The three main factors that affect phase noise are update rate, phase detector gain and the phase noise characteristic of the reference frequency. Other factors such as the temperature and supply voltage level have a minimal effect on phase noise.

Update Rate:
The update rate is the frequency at which the synthesizer phase detector is operating. Mathematically, it is represented as Update Rate = FREF/R, where FREF is the reference frequency. Generally, the higher the update rate, the lower the phase noise. Figure 1 below shows the phase noise characteristic for Si4133 (IF = 550 MHz) under typical conditions. The update rates used are 200 kHz and 1000 kHz.

![Si4133 IF Phase Noise Plots @ 550 MHz](image)

**Figure 1. Si4133 Phase Noise for Fphi = 200 kHz and 1000 kHz**

From figure 1 above, it is apparent that the 1000 kHz update rate results in lower phase noise. This is more noticeable at lower offset frequencies.

The update rate also affects the loop bandwidth. This effect can also be observed in figure 1. The loop bandwidth of the synthesizers is proportional to the update rate.

Phase Detector Gain:
The phase detector gain setting can also be used for optimizing phase noise performance. Figure 2 below shows the phase noise characteristics for various RF1 phase detector (KP1) settings.
For offset frequencies much less than the loop bandwidth, higher phase detector gains lead to lower phase noise. However, it is important to point out that a very large phase detector gain can also result in the loop being unstable. It is recommended that the phase detector gain be set according to the value programmed into the N register. This information is available in the synthesizer device data sheets.

**Frequency Reference:**
At offset frequencies much less than the loop bandwidth, the reference source largely determines the phase noise of the output. For this reason, it is recommended that a stable reference such as a temperature compensated crystal oscillator (TCXO) be used in applications requiring very good phase noise performance.

In general for synthesizers, the phase noise at a given offset frequency reduces as the offset frequency increases. For integrated phase noise therefore, the lower offset frequencies dominate the integration. As a result, the frequency reference plays a dominant role in the value of the integrated phase error.

**Q: What are the effects of changing the update rate?**

A: The parameters dependent on, or affected by, the update rate include loop bandwidth, settling time of the PLL, resolution of the channel spacing, and the location of reference related spurs on the phase noise characteristic. Additionally, the loop bandwidth determines the dominant source of phase noise at a given frequency offset.

**Loop Bandwidth:**
The update rate determines the loop bandwidth of the PLL. Specifically, the loop bandwidth is approximately one tenth of the update rate. Changing the update rate affects the overall phase noise characteristic.

For offset frequencies much less than the loop bandwidth, the overall phase noise is dominated by the reference source. On the other hand, the voltage-controlled oscillator (VCO) phase noise dominates the overall phase noise for offset frequencies much larger than the loop bandwidth.
Settling Time:
The settling time of the PLL is also dependent on the update rate. A higher update rate leads to a shorter settling time. Specific details about the relationship between update rate and settling time are contained in the synthesizer device data sheets. As an example, a 500 kHz update rate on the Si4133 corresponds to a settling time of 80 µs.

Channel Spacing Resolution:
Resolution of the channel spacing is determined by the update rate. The output frequency can be written as $F_{OUT} = \left( F_{REF}/R \right) \times N$, where $F_{REF}$ is the reference frequency. This can be re-written as $F_{OUT} = \left( \text{Update Rate} \right) \times N$. Therefore, the output frequency can be changed in steps equivalent to the update rate. This is achieved by simply incrementing or decrementing the value of the N register.

Channel spacing is an important consideration in applications where the synthesizer is used to generate different frequencies. A lower update rate is necessary for more closely spaced channels.

Reference Related Spurs:
Reference related spurs are present in the output frequency spectrum of the synthesizer and occur at integer intervals of the update rate. These spurs can be seen in figures 3 and 4 below. In figure 1, update rates of 200 kHz and 1000 kHz are used. In the case of the 200 kHz update rate, the spurs are located at 200 kHz, 400 kHz, 600 kHz and 1000 kHz. For the 1000 kHz update rate, the first spur is located at an offset of 1000 kHz.

Generally, the QFN packages offer better reference related spur performance than TSSOP packages.
Q: Are the terms "update rate", "comparison frequency" and "step size" equivalent?

A: For the Silicon Laboratories Si41xx synthesizer family, these terms refer to the same parameter and can be used interchangeably.
Si41xx FAQ

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