

Timing Simplified

Silicon Labs offers a broad portfolio of frequency flexible timing products that enable hardware designers to simplify clock generation, distribution, and jitter attenuation. The portfolio includes:

- Network synchronizers
- Jitter attenuating clocks
- Clock generators
- Clock buffers
- PCIe clocks and buffers
- Oscillators (XO/VCXO)

Silicon Labs clocks use proprietary DSPLL and MultiSynth technologies to generate any combination of frequencies with ultra-low jitter, enabling best-in-class clock tree integration. Clock buffers provide low-jitter, low-skew clock distribution with integrated format/voltage level translation. PCIe clocks/buffers combine Gen 1/2/3/4 compliance with on-chip series termination, simplifying design. XO/VCXOs are factory-customizable to any frequency, with samples available in one to two weeks.



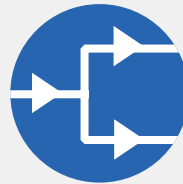
Oscillators

- Any frequency up to 1.5 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)



Clock Generators

- Any-frequency, any-output
- Ultra-low jitter: 90 fs RMS
- Clock tree on a chip replaces clocks and XOs



Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4 compliant



Jitter Attenuating Clocks/Network Sync

- Any frequency, any output
- Ultra-low jitter: 90 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs

Recommended Timing Solutions for Intel



Protocol	Intel (Altera)											Silicon Labs									
	Stratix			Arria				Cyclone				Jitter Band (MHz)	Refclk TJ rms max (fs)	XO/VCXO			Buffer	Clock Gen			Jitter Atten. Clock
	10 GX/SX	V GX/GS	V GT	10 GX/SX	10 GT	V GX	V GT/ST	V GZ	10 GX	V GX/SX	V GT/ST			Si51x	Si59x	Si54x	Si533xx	Si5338	Si5341	Si5332	Si534x/8x
SGMII/QSGMII	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	1-20	1400	✓	✓	✓	✓	✓	✓	✓	✓
QPI	✓	✓	✓	✓	✓			✓				Intel	200	✓		✓	✓	✓			✓
SAS/SATA 6G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	2.6-15	780	✓	✓	✓	✓	✓	✓	✓	✓
SAS/SATA 12G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	2.6-15	390	✓		✓	✓		✓	✓	✓
SerialLite II, III	✓	✓	✓	✓	✓			✓	✓			Intel	1600	✓	✓	✓	✓	✓	✓	✓	✓
SDI 6G, 12G	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	0.1-F/2	400		✓	✓	✓		✓	✓	✓
SFI-5.1	✓	✓	✓	✓	✓	✓	✓	✓				4-20	1300	✓	✓	✓	✓	✓	✓	✓	✓
SFI-5.2	✓	✓	✓	✓	✓			✓				4-20	380	✓		✓	✓		✓	✓	✓
RapidIO-1,2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	4-20	640	✓	✓	✓	✓	✓	✓	✓	✓
RapidIO-3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	4-20	410	✓		✓	✓	✓			✓
RapidIO-4	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	1.9-10	290			✓	✓		✓	✓	✓
SONET/SDH OC-48	✓	✓	✓	✓	✓	✓	✓	✓	✓			1-20	1000	✓	✓	✓	✓	✓			✓
SONET/SDH OC-192	✓	✓	✓	✓	✓	✓	✓	✓	✓			4-20	240			✓	✓		✓		✓
XAUI 10GBASE-X	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	0.6-20	430	✓		✓	✓	✓	✓	✓	✓
XLAUI (40GbE)	✓	✓	✓	✓	✓			✓				0.6-20	430	✓		✓	✓		✓	✓	✓

Intel FPGA Phase Noise Mask Requirements



Stratix 10 GX/SX Arria 10 GX/SX/GT Stratix V GX/GS/GT Arria V GX/SX		XO		VCXO	Clock Buffer	Clock Generator			Jitter Attenuating Clock	Network Synchronizers (SyncE/1588)
Offset	Phase Noise at 156.25 MHz (dBc/Hz)	Si540 (dBc/Hz)	Si570/Si53x (dBc/Hz)	Si55x (dBc/Hz)	Si5330x Universal Buffers (dBc/Hz)	Si5341 Si5340 (dBc/Hz)	Si5332 (dBc/Hz)	Si5338 Si5335 (dBc/Hz)	Si5347/6/5/4/2 (dBc/Hz)	Si5383/48 (dBc/Hz)
100 Hz	-82	-110	-113	-86	-117	-94	-100	-90	-92	-93
1 kHz	-102	-121	-121	-114	-132	-125	-118	-120	-124	-122
10 kHz	-112	-132	-129	-132	-140	-136	-125	-126	-136	-137
100 kHz	-122	-151	-134	-142	-150	-141	-132	-132	-141	-145

Intel FPGA Phase Noise Mask Requirements



Arria V GT/ST		XO		VCXO	Clock Buffer	Clock Generator			Jitter Attenuating Clock	Network Synchronizers (SyncE/1588)
Offset	Phase Noise at 156.25 MHz (dBc/Hz)	Si540 (dBc/Hz)	Si570/ Si53x (dBc/Hz)	Si55x (dBc/Hz)	Si5330x Universal Buffers (dBc/Hz)	Si5341 Si5340 (dBc/Hz)	Si5332 (dBc/Hz)	Si5338 Si5335 (dBc/Hz)	Si5347/6/5/4/2 (dBc/Hz)	Si5383/48 (dBc/Hz)
100 Hz	-80	-110	-113	-86	-117	-94	-100	-90	-92	-93
1 kHz	-110	-121	-121	-114	-132	-125	-118	-120	-124	-122
10 kHz	-120	-132	-129	-132	-140	-136	-125	-126	-136	-137
100 kHz	-120	-151	-134	-142	-150	-141	-132	-132	-141	-145
1 MHz	-130	-160	-145	-148	-154	-150	-145	-132	-154	-150