Process Change Notice #1003232

User Registration
Register today to create your account on Silabs.com. Your personalized profile allows you to receive technical document updates, new product announcements, "how-to" and design documents, product change notices (PCN) and other valuable content available only to registered users. http://www.silabs.com/profile

PCN Date: 23Mar10		**Effective Date:** 23Jun10
Title: C8051F5xx-Ix Datasheet Updates and Errata Elimination		
Originator: Dan Lunecki	**Phone:** +1.512.532.5227	**Dept:** Product Marketing
Customer Contact: Kathy Haggar	**Phone:** +1.512.532.5261	**Dept:** Sales / Customer Service

PCN Type:

☐ **Assembly** ☐ **Discontinuance** ☐ **Package** ☐ **Test**
☒ **Datasheet** ☐ **Fabrication** ☐ **Product Revision**
☐ **Packing** ☐ **Labeling** ☐ **Location** ☐ **Other**

Last Order Date: N/A

PCN Details

Description of Change:

Update C8051F5xx-Ix datasheets to incorporate Errata plus C8051F5xx-Ax automotive grade products. The datasheet change details are listed in Appendix A.

Reason for Change:

Eliminate the Errata and add automotive grade part numbers

Impact on Form, Fit, Function, Quality, Reliability:

The impact on form, fit, function, quality or reliability is identified in the datasheet change detail in Appendix A.

Product Identification:

Family	New Datasheet	Old → New Revision
C8051F50x/F51x	C8051F0x-F1x	1.0 → 1.1
C8051F52x/F53x	C8051F52x-F53x	1.1 → 1.2
C8051F4x	C8051F54x	0.1 → 1.0
C8051F55x/F56x/F57x	C8051F55x-F56x-F57x	0.5 → 1.0
C8051F58x/F59x	C8051F58x-F59x	1.1 → 1.2

Last Date of Unchanged Product: N/A

Qualification Samples: N/A

Qualification Data: N/A

APPENDIX A – Datasheet Change Details

C8051F0x-F51x Revision 1.0 to Revision 1.1

- Updated "Ordering Information" on page 20 and Table 2.1, "Product Selection Guide," on page 21 to include -A (Automotive) devices and automotive qualification information.
- Updated supply current related specifications throughout "5. Electrical Characteristics".
- Updated SFR Definition 8.1 to change VREF high setting to 2.20 V from 2.25 V.
- Updated Table 5.12 on page 51 and Figure 9.1 on page 75 to indicate that Comparators are powered from VIO and not VDDA.
- Updated Table 5.12 on page 51 to fix Comparator Supply Current Typical values for Modes 2 and 3.
- Updated the Gain Table in "6.3.1. Calculating the Gain Value" to fix the ADC0GNH Value in the last row.
- Updated Table 11.1 on page 89 with correct timing for all branch instructions, MOVC, and CPL A.
- Updated "15.1. Programming The Flash Memory" to clarify behavior of 8-bit MOVX instructions and when writing/erasing Flash.
- Updated SFR Definition 15.3 to include FLEWT bit definition. This bit must be set before writing or erasing Flash. Also updated Table 5.5 to reflect new Flash Write and Erase timing.
- Updated "17.7. Flash Error Reset" with an additional cause of a Flash Error reset.
- Updated "20.1.3. Interfacing Port I/O in a Multi-Voltage System" to remove note regarding interfacing to voltages above VIO.
- Updated "23. SMBus"to remove all hardware ACK features, including SMB0ADM and SMB0ADR SFRs.
- Updated "24.3.2. Data Reception" to clarify UART receive FIFO behavior.
- Updated SFR Definition 24.1 for SCON0 to correct SFR Page to 0x00 from All Pages.

Note: All items from the C8051F50x-F51x Errata dated July 1, 2009 are incorporated into this data sheet.

C8051F52x-F53x Revision 1.1 to 1.2

- Updated "Ordering Information" on page 14 and Table 1.1, "Product Selection Guide (Recommended
- for New Designs)," on page 14 to include -A (Automotive) devices and automotive qualification information.
- Updated Table 2.3, "ADC0 Electrical Characteristics," on page 29 to include Temperature Sensor tracking time requirement and update INL maximum specification.
- Updated Figure 3.1. 'DFN-10 Package Diagram' on page 39 with new Pin-1 detail drawing.
- Updated Table 8.1, "CIP-51 Instruction Set Summary," on page 83 with correct CJNE and CPL timing.
- Updated "Power-Fail Reset / VDD Monitor" on page 107 to clarify the recommendations for the VDD monitor.

Note: All items from the C8051F52xA-F53xA Errata dated August 26, 2009 are incorporated into this data sheet.

C8051F54x Revision 0.1 to Revision 1.0

- Updated "2. Ordering Information" to include -A (Automotive) devices and automotive qualification information.
- Updated Figure 3.9.
- Updated supply current related specifications throughout "4. Electrical Characteristics" .
- Updated SFR Definition 6.1 (REF0CN) to change VREF high setting to 2.20 V from 2.25 V.
- Updated Figure 7.1 to indicate that Comparators are powered from VIO and not VDDA.
- Updated the Gain Table in "5.3.1. Calculating the Gain Value" to fix the ADC0GNH Value in the last row.
- Updated Table 9.1 with correct timing for all branch instructions, MOVC, and CPL A.
- Updated Table 13.1 to indicate behavior when performing a Flash operation in reserved space.
- Updated "13.1. Programming The Flash Memory" to clarify behavior of 8-bit MOVX instructions and when writing/erasing Flash.
- Updated SFR Definition 13.3 (FLSCL) to include FLEWT bit definition. This bit must be set before writing or erasing Flash. Also updated Table 4.5 to reflect new Flash Write and Erase timing.
- Updated "15.7. Flash Error Reset" with an additional cause of a Flash Error reset.
- Updated "17.1.3. Interfacing Port I/O in a Multi-Voltage System" to remove note regarding interfacing to voltages above VIO.
- Updated "19. SMBus" to remove all hardware ACK features, including SMB0ADM and SMB0ADR SFRs.
- Updated SFR Definition 20.1(SCON0) to correct SFR Page to 0x00 from All Pages.
- Updated CP Register Definition 24.2 with proper Device ID.

Note: All items from the C8051F54x Errata dated November 5th, 2009 are incorporated into this data sheet.

C8051F55x-F56x-F57x Revision 0.5 to Revision 1.0

- Updated "2. Ordering Information" to include -A (Automotive) devices and automotive qualification information.
- Updated Figure 4.8 on page 35.
- Updated supply current related specifications throughout "5. Electrical Characteristics" .
- Updated SFR Definition 7.1 to change VREF high setting to 2.20 V from 2.25 V.
- Updated Figure 8.1 to indicate that Comparators are powered from VIO and not VDDA.
- Updated the Gain Table in "6.3.1. Calculating the Gain Value" to fix the ADC0GNH Value in the last row.
- Updated Table 10.1 with correct timing for all branch instructions, MOVC, and CPL A.
- Updated "14.2. Non-volatile Data Storage" to clarify behavior of 8-bit MOVX instructions and when writing/erasing Flash.
- Updated SFR Definition 14.3 (FLSCL) to include FLEWT bit definition. This bit must be set before writing or erasing Flash. Also updated Table 5.5 to reflect new Flash Write and Erase timing.
- Updated "16.7. Flash Error Reset" with an additional cause of a Flash Error reset.
- Updated "19.1.3. Interfacing Port I/O in a Multi-Voltage System" to remove note regarding interfacing to voltages above VIO.
- Updated "22. SMBus" to remove all hardware ACK features, including SMB0ADM and SMB0ADR SFRs.
- Updated SFR Definition 23.1 (SCON0) to correct SFR Page to 0x00 from All Pages.

Note: All items from the C8051F55x-F56x-57x Errata dated November 5th, 2009 are incorporated into this data sheet.

C8051F58x-F59x Revision 1.0 to Revision 1.1

- Updated “Ordering Information” on page 22 to include -A (Automotive) devices and automotive qualification information.
- Updated supply current related specifications throughout “5. Electrical Characteristics” .
- Updated SFR Definition 8.1 to change VREF high setting to 2.20 V from 2.25 V.
- Updated Table 5.12 on page 53 and Figure 9.1 on Page 77 to indicate that Comparators are powered from VIO and not VDDA.
- Updated the Gain Table in “Calculating the Gain Value” on page 60 to fix the ADC0GNH Value in the last row.
- Updated Table 11.1 on page 94 with correct timing for all branch instructions, MOVC, and CPL A.
- Updated “Programming The Flash Memory” on page 138 to clarify behavior of 8-bit MOVX instructions and when writing/erasing Flash.
- Updated SFR Definition 15.3 (FLSCL) to include FLEWT bit definition. This bit must be set before writing or erasing Flash. Also updated Table 5.5 on page 48 to reflect new Flash Write and Erase timing.
- Updated “17.7. Flash Error Reset” with an additional cause of a Flash Error reset.
- Updated “20.1. Port I/O Modes of Operation” to remove note regarding interfacing to voltages above VIO.
- Updated “23. SMBus” to remove all hardware ACK features, including SMB0ADM and SMB0ADR SFRs.
- Updated “24.3.2. Data Reception” to clarify UART receive FIFO behavior.
- Updated SFR Definition 24.1 (SCON0) to correct SFR Page to 0x00 from All Pages.
- Various formatting changes and corrections throughout the document.

Note: All items from the C8051F58x/59x Errata dated July 1, 2009 are incorporated into this data sheet.

