Process Change Notice #1101101

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PCN Date: 10Jan11		**Effective Date:** 10Apr11
Title: Si4010 Revision C		
Originator: Lawrence Der	**Phone:** 512-532-5830	**Dept:** Wireless Marketing - EMS
Customer Contact: Kathy Haggar	**Phone:** 512-532-5261	**Dept:** Inside Sales

PCN Type:

☐ **Assembly**	☐ **Discontinuance**	☐ **Package**	☐ **Test**
☐ **Datasheet**	☐ **Fabrication**	☒ **Product Revision**	
☐ **Packing**	☐ **Labeling**	☐ **Location**	☐ **Other**

Last Order Date: 10Apr11

PCN Details

Description of Change:

Silicon Laboratories, Inc. (Silicon Labs) is pleased to announce Revision C2 of Si4010 products.

Revision C2 allows an additional 50 bytes of RAM memory recovery with the Rev C silicon in FSK mode, should the customer decide to recompile the code per Rev C headers. The recompilation is optional, i.e., not required. The details are explained below:

Rev C ROM function has changed by correcting the vFcast_FskAdj() function.

Nothing will change in the compiled code when the chip is used in OOK mode, since this API function is never called. Therefore, compiled code is not linked to the user code from the si4010_fix_rom_keil.lib.

Moreover, the ROM change is transparent to the user if desired. Customers can continue to use the released headers for rev B, compile and link applications as usual and their application will work on both rev B and rev C devices. However, customers using rev C silicon with rev B headers, will have 50 Bytes of dead weight in the RAM in FSK mode. Customers desiring this space must make the following changes:

1. In the si4010_rom_keil.a51 file, change the following line:
   ; RomSymbol _VFCAST_FSKADJ, 080FCH .. fix_rom library needed
   To:
   RomSymbol _VFCAST_FSKADJ, 080FCH
   (only remove the ';' from the beginning of the line)
2. The si4010_fix_rom_keil.lib should be removed from the list of 'files to link' of their project
3. Re-compile and re-link the application to get those 50 bytes back

Note:

- The three steps above are not required
- The three steps do not have any effect in OOK mode [if call to vFcast_FskAdj() is not present in the project]
- Customers desiring re-compilation of the rev C code with the rev C headers, should be aware that the product will NO LONGER run on rev B silicon.

Customers using rev B silicon, must use rev B headers. However, the rev C silicon can use either the rev B or rev C headers. Customers using rev C headers with rev C silicon, can get an additional 50 bytes of RAM memory when using FSK mode.

Reason for Change:

The Si4010-C2-GS/R and Si4010-C2-GT/R correct the RESET errata and ROM bug associated with the Si4010-B1-GS/R and Si4010-B1-GT/R product.

Impact on Form, Fit, Function, Quality, Reliability:

There is no impact on form, fit, quality or reliability.

The function has been changed as described in the Description of Change above.

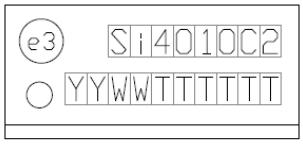
The Si4010-C2-GS is a pin-compatible, feature-compatible, drop-in replacement part for the Si4010-B1-GS. The Si4010-C2-GT is a pin-compatible, feature-compatible, drop-in replacement part with the Si4010-B1-GT.

Product Identification:

This PCN applies to devices ordered using the following ordering part numbers:

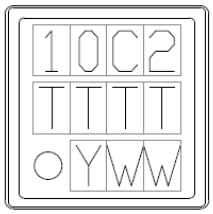
Existing OPN	Replacement OPN	Existing OPN	Replacement OPN
Si4010-B1-GS	Si4010-C2-GS	Si4010-B1-GT	Si4010-C2-GT
Si4010-B1-GSR	Si4010-C2-GSR	Si4010-B1-GTR	Si4010-C2-GTR

Si4010-C2-GS/R Device Top Mark



Mark Method:	Laser	
Pin 1 Mark:	Bottom-Left Justified	
Font Size:	0.71mm (2.0 Point) Right-Justified	
Line 1 Mark Format:	Circle 1.3mm Diameter Left Justified Silicon Labs Identifier Product ID	"e3" Pb-Free Symbol Si4010C2
Line 2 Mark Format:	YY = Year WW = Workweek TTTTTT = Trace Code	Assigned by the Assembly House. Corresponds to the year and work week of the mold date. Manufacturing code characters from the Markings section of the Assembly Purchase Order form.

Si4010-C2-GT/R Device Top Mark



Mark Method:	Laser	
Pin 1 Mark:	Circle = 0.40mm Diameter	
Font Size:	0.61mm (24 mils) Right-Justified	
Line 1 Mark Format:	Product ID	10C2
Line 2 Mark Format:	TTTT =Trace Code	Line 2 from the "Markings" section of the Assembly Purchase Order form.
Line 3 Mark Format:	Pin 1 Identifier YWW = Date Code	Lower-Left Assigned by the Assembly House. Y = Last Digit of Current Year (ex: 2008 = 8) WW = Current Work Week

Last Date of Unchanged Product: 10Apr11

Silicon Labs will discontinue the sale of the Si4010-B1-GS and Si4010-B1-GT products. Customers can order the Si4010-B1-GS and Si4010-B1-GT products until 10Apr11. Silicon Labs will not accept orders for the revision B1 devices after 10Apr11.

Qualification Samples:

Available upon request. Please contact your local Silicon Laboratories sales representative to order samples. A list of Silicon Laboratories sales representatives may be found at www.silabs.com.

Qualification Data:

See Appendix A for Qualification Report. The Si4010 Datasheet is available upon request. Please contact your local Silicon Laboratories sales representative to request the Datasheet.

Appendix A: Qualification Report

Si4010-C2-GS/GT Qualification Report

W7101F1 Product Qualification Plan and Report Rev. D

Part Rev C2, TSMC Fabrication,Unisem Assembly except as noted							
Test Name	**Test Condition**	**Qualification**	**Lot ID or Start**	**Fail/Pass or End**	**Notes**	**Summary**	**Status**
Test Group A - Accelerated Environment Stress Tests - Unisem 10MSOP							
HAST	JA110		Q29022	0/77	1		
	130°C, 85%RH	3 lots, N=>25	Q29019	0/79	1	3 lots	
	Vcc=3.6V, 96 hours		Q29163	0/78	1	0/234	Pass
Temp Cycle	JA104		Q29026	0/77	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q29023	0/81	1	3 lots	
			Q29162	0/78	1	0/236	Pass
HTSL	JA103		Q29024	0/33	1		
	150°C, 1000hr	3 lots, N=>25	Q29021	0/58	1	3 lots	
			Q29161	0/46	1	0/137	Pass
Test Group A - Accelerated Environment Stress Tests - Unisem 14SOIC							
HAST	JA110		Q28876	0/80	1		
	130°C, 85%RH	3 lots, N=>25	Q28885	1/79	1	3 lots	
	Vcc=3.6V, 96 hours		Q28851	0/80	1	1/239	Pass
Temp Cycle	JA104		Q28878	0/80	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q28883	0/80	1	3 lots	
	500 cycles		Q28853	0/80	1	0/240	Pass
HTSL	JA103		Q28879	0/50	1		
	150°C, 1000hr	3 lots, N=>25	Q28884	0/50	1	3 lots	
			Q28850	0/27	1	0/127	Pass
Test Group B - Accelerated Lifetime Simulation Tests							
HTOL	JA108		Q28629	0/80			
	125°C, Dynamic	3 lots, N=>77	Q28903	0/80			
	Vcc=3.6V, 1000 hours		Q28904	0/79		3 lots	
			Q29729	20-Dec		0/239	In Progress
LTOL	JA108		Q22643	0/80			
	-10°C, Dynamic	1 lot, N=>32				1 lots	
	Vcc=3.6V, 1000 hours					0/80	Pass
ELFR	JA108		Q29612	0/810			
	125°C, Dynamic	3 lots, N=>500	Q29173	0/1882		2 lots	
	Vcc=3.6V, 48 hours		Q28789	20-Dec		0/2692	In Progress

Appendix A: Qualification Report (cont)

Part Rev C2, TSMC Fabrication,Unisem Assembly except as noted							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group C - Package Assembly Integrity Tests - Unisem 10MSOP							
Wire Bond Shear	JB116	5 units, N=>30	454931.1 456820.1 458229.1	20-Dec 20-Dec 20-Dec		0 lots 0/0	In Progress
Wire Bond Pull	M2011	5 units, N=>30	454931.1 456820.1 458229.1	20-Dec 20-Dec 20-Dec		0 lots 0/0	In Progress
Physical Dimensions	JB100	3 lots, N=>10	454931.1 456820.1 458229.1	20-Dec 20-Dec 20-Dec		0 lots 0/0	In Progress
Solderability	JB102	3 lots, 15 leads	454931.1 456820.1 458229.1	20-Dec 20-Dec 20-Dec		0 lots 0/0	In Progress
Test Group C - Package Assembly Integrity Tests - Unisem 14SOIC							
Wire Bond Shear	AEC-Q100-001	5 units, N=>30	456821.1 454922.1 458228.1	20-Dec 20-Dec 20-Dec		0 lots 0/0	In Progress
Wire Bond Pull	M-STD-883 Performed post-TC	5 units, N=>30	456821.1 454922.1 458228.1	20-Dec 20-Dec 20-Dec		0 lots 0/0	In Progress
Physical Dimensions	JB100	3 lots, N=>10	456821.1 454922.1 458228.1	20-Dec 20-Dec 20-Dec		0 lots 0/0	In Progress
Solderability	JB102	1 lot, N=>15	456821.1 454922.1 458228.1	20-Dec 20-Dec 20-Dec		0 lots 0/0	In Progress
Test Group E - Electrical Verification							
ESD-HBM	JA114	1 lot, N=>3	Q29675	0/3		±2.5kV	Pass
ESD-MM	JA115	1 lot, N=>3	Q29676	0/3		±250V	Pass
ESD-CDM	JC101	1 lot, N=>3	Q29730 Q29674	0/3 0/3	10MSOP 14SOIC	±1.25kV ±1.25kV	Pass
Latch Up	JESD78 ±200mA Overvoltage = 5.4V	1 lot, N=>6	Q29116 Q29115	0/6 0/6	85°C 25°C	2 lots 0/12	Pass

Notes:
1. Preceded by MSL2@260C Preconditioning

