Process Change Notice # 1104121

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PCN Date: 12Apr11		**Effective Date: 12Jul11**
Title: C8051F5xx Datasheets and Errata Updates		
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PCN Type:

☐ **Assembly**	☐ **Discontinuance**	☐ **Package**	☐ **Test**
☒ **Datasheet**	☐ **Fabrication**	☐ **Product Revision**	
☐ **Packing**	☐ **Labeling**	☐ **Location**	☐ **Other**

Last Order Date: N/A

PCN Details

Description of Change:

Updated C8051F5xx datasheets and errata. The datasheet details are listed in Appendix A.

Reason for Change:

Keeps datasheets and errata consistent with revisions to the part.

Impact on Form, Fit, Function, Quality, Reliability:

No impact to product form, fit, quality or reliability. The details of datasheet functional changes are listed in Appendix A.

Product Identification:

Family Datasheet	Old ➔ New Revision
C8051F50x/ F51x	1.1 ➔ 1.2
C8051F52x/F52xA/F53x/F53xA	1.2 ➔ 1.3
C8051F55x/F56x/F57x	1.0 ➔ 1.1
C8051F54x	1.0 ➔ 1.1
C8051F58x/F59x	1.1 ➔ 1.2

Last Date of Unchanged Product: 12-Jul-11

Qualification Samples:

Samples available upon request. Please contact your local Silicon Laboratories sales representative to order samples. A list of Silicon Laboratories sales representatives may be found at www.silabs.com.

Qualification Data: N/A.

The revised datasheets and errata are available at www.silabs.com for registered users.

APPENDIX A – Datasheet Change Details

C8051F50x-F51x Revision 1.1 to Revision 1.2

- Updated “1. System Overview” with a voltage range specification for the internal oscillator.
- Updated Table 5.6 on page 47 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.
- Updated “5. Electrical Characteristics” to remove the internal oscillator curve across temperature diagram.
- Updated SFR Definition 10.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.
- Updated “21. Local Interconnect Network (LIN)” with a voltage range specification for the internal oscillator.
- Updated “22. Controller Area Network (CAN0)” with a voltage range specification for the internal oscillator.
- Updated SFR Definition 8.1 (REF0CN) with oscillator suspend requirement for ZTCEN.
- Updated "16.3 Suspend Mode" with note regarding ZTCEN.
- Updated Figure 6.4 with new timing diagram when using CNVSTR pin.
- Added Port 2 Event and Port 3 Events to wake-up sources in Section 19.2.1.
- Updated LIN Register Definitions 21.9 and 21.10 with correct reset values.
- Updated C2 Register Definitions 28.2 and 28.3 with correct C2 and SFR addresses.

C8051F52x/F52xA/F53x/F53xA Revision 1.2 to Revision 1.3

- Updated System Overview on page 13 with a voltage range specification for the internal oscillator.
- Updated Table 2.10 on page 34 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.
- Updated Section 2 to remove the internal oscillator curve across temperature diagram.
- Updated Figure 4.5 12-Bit ADC Burst Mode Example with Repeat Count Set to 4 on page 59 with new timing diagram when using CNVSTR pin.
- Updated SFR Definition 5.1 (REF0CN) with oscillator suspend requirement for ZTCEN.
- Updated SFR Definition 6.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.
- Updated Section 8.3.3. Suspend Mode on page 90 with note regarding ZTCEN.
- Updated Section 17. LIN (C8051F520/0A/3/3A/6/6A and C8051F530/0A/3/3A/6/6A) on page 163 with a voltage range specification for the internal oscillator.

C8051F54x Revision 1.0 to Revision 1.1

▫ Updated 1. System Overview with a voltage range specification for the internal oscillator.

▫ Updated Figure 5.4, 12-Bit ADC Burst Mode Example With Repeat Count Set to 4, on page 33 with new timing diagram when using CNVSTR pin.

▫ Updated Table 6.6, Internal High-Frequency Oscillator Electrical Characteristics, on page 53 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.

▫ Updated 6. Electrical Characteristics to remove the internal oscillator curve across temperature diagram.

▫ Updated SFR Definition 7.1 (REF0CN) with oscillator suspend requirement for ZTCEN.

▫ Fixed incorrect cross references in 8. Comparators.

▫ Updated SFR Definition 9.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.

▫ Updated Figure 11.2, Flash Program Memory Map, on page 86 with correct address for start of lock byte page from 0x3900 to 0x3A00.

▫ Updated 15.3. Suspend Mode with note regarding ZTCEN.

▫ Added Port 2 Event and Port 3 Event to wake-up sources in 17.2.1. Internal Oscillator Suspend Mode

▫ Updated 19. Local Interconnect Network (LIN) with a voltage range specification for the internal oscillator.

▫ Updated LIN Register Definitions for LIN0MUL and LIN0DIV to correct the reset value.

▫ Updated C2 Register Definitions 25.2 and 25.3 with correct C2 and SFR addresses.

C805155x/F56x/F57x Revision 1.0 to Revision 1.1

▫ Updated 1. System Overview with a voltage range specification for the internal oscillator.

▫ Updated Table 5.6, Internal High-Frequency Oscillator Electrical Characteristics, on page 42 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.

▫ Updated 5. Electrical Characteristics to remove the internal oscillator curve across temperature diagram.

▫ Updated Figure 6.4 on Page 51 with new timing diagram when using CNVSTR pin.

▫ Updated SFR Definition 7.1 (REF0CN) with oscillator suspend requirement for ZTCEN.

▫ Fixed incorrect cross references in 8. Comparators.

▫ Updated SFR Definition 9.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.

▫ Update 15.3. Suspend Mode with note regarding ZTCEN.

▫ Added Port 2 Event and Port 3 Events to wake-up sources in 18.2.1. Internal Oscillator Suspend Mode

▫ Updated 20. Local Interconnect Network (LIN0) with a voltage range specification for the internal oscillator.

▫ Updated LIN Register Definitions 20.9 and 20.10 with correct reset values.

▫ Updated 21. Controller Area Network (CAN0) with a voltage range specification for the internal oscillator.

▫ Updated C2 Register Definitions 27.2 and 27.3 with correct C2 and SFR Addresses.

C8051F58x/F59x Revision 1.1 to Revision 1.2

▫ Updated 1. System Overview with a voltage range specification for the internal oscillator.

▫ Updated Table 5.6, Internal High-Frequency Oscillator Electrical Characteristics, on page 49 with new conditions for the internal oscillator accuracy. The internal oscillator accuracy is dependent on the operating voltage range.

▫ Updated 5. Electrical Characteristics to remove the internal oscillator curve across temperature diagram.

▫ Updated Figure 6.4 with new timing diagram when using CNVSTR pin.

▫ Updated SFR Definition 8.1 (REF0CN) with oscillator suspend requirement for ZTCEN.

▫ Fixed incorrect cross references in 9. Comparators .

▫ Updated SFR Definition 10.1 (REG0CN) with a new definition for Bit 6. The bit 6 reset value is 1b and must be written to 1b.

▫ Updated SFR Definition 12.1 (PSBANK) with correct reset value.

▫ Updated 16.3. Suspend Mode with note regarding ZTCEN.

▫ Added Port 2 Event and Port 3 Events to wake-up sources in 19.2.1. Internal Oscillator Suspend Mode .

▫ Updated SFR Definition 20.3 with correct names for bits CP2AE and CP2E.

▫ Updated 21. Local Interconnect Network (LIN0) with a voltage range specification for the internal oscillator.

▫ Updated LIN Register Definitions 21.9 and 21.10 with correct reset values.

▫ Updated 22. Controller Area Network (CAN0) with a voltage range specification for the internal oscillator.

▫ Updated C2 Register Definitions 30.2 and 30.3 with correct C2 and SFR addresses.

