



17070795 C8051F99x Datasheet Update PCN

PCN Issue Date: 7/7/2017

Effective Date: 10/12/2017

PCN Type: Datasheet

Description of Change

Silicon Labs is pleased to announce the release of version 1.3 of the C8051F99x datasheet.

This change is to increase the robustness of the Brown Out Detector and includes a single specification change of the maximum Power-On Reset(POR) Monitor Threshold voltage level and other minor updates. The complete list of changes are as follows.

- Increased the maximum Power-On Reset(POR) Monitor Threshold voltage level in Table 4.4. "Reset Electrical Characteristics" from 1.3 V to 1.4 V.
- Removed incorrect mentions of two-cell mode.
- Added additional information to Section 20.2.3 "Using the Low Frequency Oscillator (LFO)" to clarify that altering BIASX2 and LOADCAP affects the LFO.
- Corrected the address of the RTC0CN register from 0x04 to 0x05 in Section 20.1.2" Using RTC0ADR and RTC0DAT to Access SmartClock Internal Registers".
- Corrected the value written to RTC0ADR in Section 20.1.3 "RTC0ADR Short Strobe Feature". The value written to RTC0ADR should be #015h instead of #095h.
- Added a recommendation for a 1ms delay to the start up procedure for Section 19.3.1. "External Crystal Mode".
- Updated the description in Section 19.4 "Special Function Registers for Selecting and Configuring the System Clock" to 14 MHz to be consistent with the FLSC register (SFR Definition 14.5).
- Updated the LFOEN bit in the RTC0XCN register to indicate the read and write access rather than only read.

Reason for Change

This family of devices contains 2 systems to protect itself from low Vdd voltages. After the Vdd monitor the POR monitor is the second defense system and mainly protects the device during sleep mode. The datasheet version 1.2 specification indicated that if, while in sleep, the Vdd level went below 1.3V that the device would reset. The new datasheet version 1.3 specification now indicates that the Vdd level must go below 1.4V before the device will reset. This means the device may reset slightly earlier than before if experiencing a falling Vdd. This change does not affect how the device operates as the minimum Vdd level is 1.8V. This change is made to ensure all systems are unaffected by a falling Vdd and no issues have been observed on devices due to this change. The other changes in the datasheet are minor and are part of Silicon Labs continual improvement process.

Impact on Form, Fit, Function, Quality, Reliability

This change does not impact form, fit, quality, or reliability and neither the old nor the new specification of the POR maximum voltage have not been found to cause any issues. For function impact, see change reason section.

Product Identification

C8051F990-C-GM
C8051F990-C-GMR
C8051F991-C-GM
C8051F991-C-GMR
C8051F996-C-GM
C8051F996-C-GMR
C8051F996-C-GU
C8051F996-C-GUR
C8051F997-C-GM
C8051F997-C-GMR
C8051F997-C-GU
C8051F997-C-GUR

Last Date of Unchanged Product: 10/12/2017

Qualification Samples

Samples available on request

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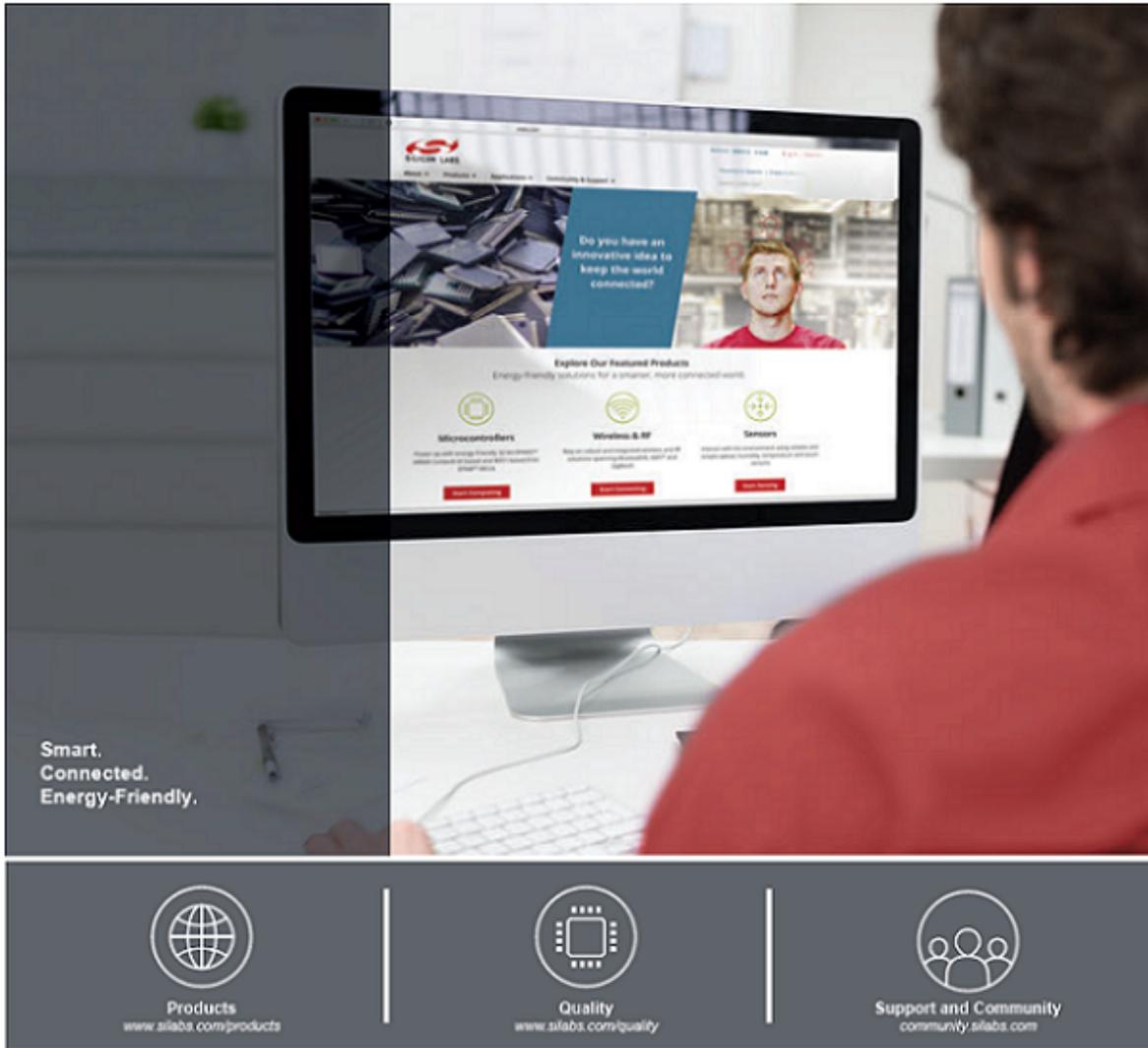
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Qualification Data

Qualification data available on request



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