



190222485 C8051F37x/39x Datasheet V1.2 Release

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Effective Date: 2/22/2019

Description of Change

Silicon Labs is pleased to announce the release of version 1.2 of the C8051F37x/39x datasheet. The changes are as follows.

- Updated the incorrectly documented SFR Definition 16.1. PFE0CN: Prefetch Engine Control by changing the PFEN bit of the PFE0CN register from a reset value of 1 to a reset value of 0. This indicates that the prefetch engine is disabled after a reset and must be turned back on if the device is running above 25MHz.
- Updated Section 16. Prefetch Engine to add details stating that when running system clock above 25MHz the prefetch engine must be enabled and pointing to the 2 bits that need to be set to do this.
- Updated Table 2.1. Product Selection Guide to indicate that the C8051F37x devices are now Not Recommended For New Design (NRND).

Reason for Change

Correcting the incorrectly documented default state of the flash prefetch engine and tagging the C8051F37x devices as NRND.

Product Identification

C8051F370-A-GM
C8051F371-A-GM
C8051F374-A-GM
C8051F375-A-GM
C8051F390-A-GM
C8051F391-A-GM
C8051F392-A-GM
C8051F393-A-GM
C8051F394-A-GM
C8051F395-A-GM
C8051F396-A-GM
C8051F397-A-GM
C8051F398-A-GM
C8051F399-A-GM

This change is considered a minor change which does not affect form, fit, function, quality, or reliability. The information is being provided as a customer courtesy.

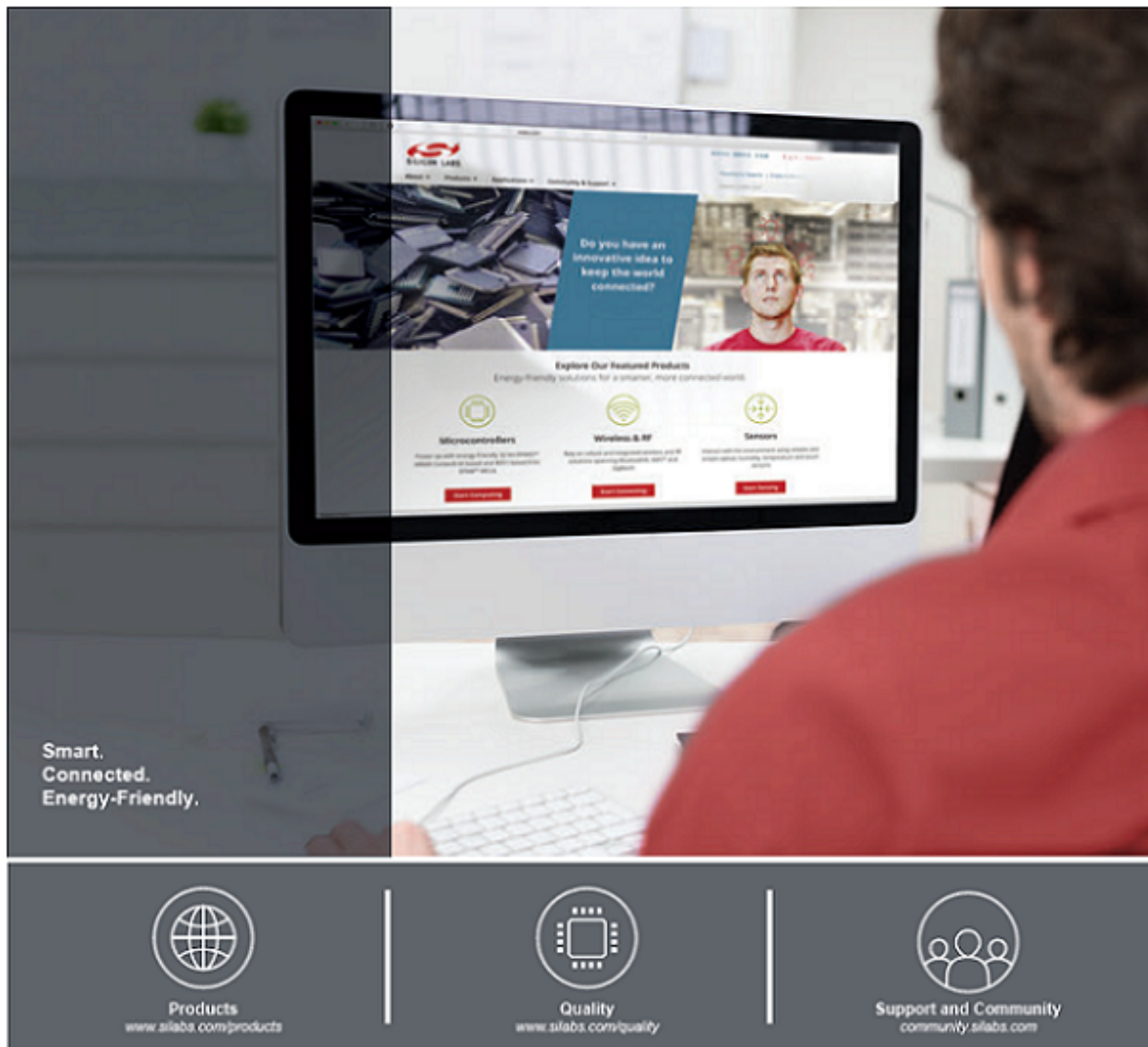
Please contact your local Silicon Labs sales representative with any questions about this notification. A list of Silicon Labs sales representatives may be found at <http://www.silabs.com>.

Customer Actions Needed:

Review datasheet changes and contact your local Silicon Labs representative with questions.

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