2412061606 SiWx917 Module Datasheet v0.7, Errata v0.1 and Marking Update

PCN Issue Date: Dec 06, 2024 **Effective Date:** Mar 12, 2025

PCN Type: Assembly; Datasheet; Errata

Description of Change

Silicon Labs is pleased to announce the release of datasheet version 0.7 for SiWG917 Wireless (SoC) Module and SiWN917 Network Co-Processor Connectivity (NCP) Module (jointly referred to as the SiWx917 Modules).

Links to datasheets:
• https://www.silabs.com/documents/public/data-sheets/siwg917y-datasheet.pdf
• https://www.silabs.com/documents/public/data-sheets/siwn917y-datasheet.pdf

Silicon Labs also announces marking update for the SiWx917 modules to add the RCM Compliance Mark, denoting the conformity with ACMA (Australia) and RSM (New Zealand) regulations.

Finally, Silicon Labs also announces the release of SiWG917 SoC Module Errata v0.1 that adds:
• OSC_32kHz_E401 (Recommendation for an External Oscillator as Mandatory Requirement)
• OSC_32kHz_E402 (Device Hangs on Application Reset and after FW Upgrade by Commander)
• OSC_32kHz_E403 (ULP MCU Calendar Peripheral is Inaccurate)

SiWN917 NCP Module Errata v0.1 is released with the following added:
• OSC_32kHz_E421 (Recommendation for External Oscillator as Mandatory Requirement)

Please review the errata documents for detailed description, affected conditions/impacts, workaround (if available) and resolution (if available).

Links to errata:
• https://www.silabs.com/documents/public/errata/siwg917-soc-module-errata.pdf
• https://www.silabs.com/documents/public/errata/siwn917-ncp-module-errata.pdf

Reason for Change

Notable changes for SiWG917 Wireless (SoC) Module v0.7 Datasheet are:
• Replaced references to "ThreadArch" with "Network Wireless Processor" and / or "NWP"
• Changed AI/ML mentions to more directly refer to the MVP block capabilities
• Updated typical electrical characteristics with characterization results
• Updated peripheral and signal names for consistency with software libraries
• Removed unsupported features: SIO, IrDA, RO temperature sensor, SCT input 1-3, SCT output 2-7
• 5.6.1.18 SPI Flash Controllers: Updated section to clarify QSPI operation and note that QSPI only available as flash interface
• Figure 5.1 NWP and M4 shared SRAM memory architecture on page 17 Corrected 192 KB SRAM bank memory multiplexing
• Updated section 5.6.1.20 with simplified options for PSRAM and Flash and added list of supported external PSRAM/Flash options. Detailed Supply configurations moved to AN1494
• 7.1 Absolute Maximum Ratings: Added absolute maximum voltage and current ratings for I/O pins
• 7.3.2 Power On Control (POC) and Reset Clarified POC and Reset functionality
• Minor corrections in the 7.4.1 clock specifications
• 32KHz crystal details and description changed, note added
• 7.6 RF Characteristics Added supported WLAN channels for different regions
• 8. Reference Schematics, BOM and Layout Guidelines
  - Split schematics into separate figures with in-text notes for legibility
  - Updated component recommendations per final design guidelines
• Updated WLAN & BLE Transmitter and Receiver typical data
• Updated current consumption typical data
• Updated Secure Debug to Debug Lock to match current functionality
• Presentation and formatting changes throughout document, including figure and table title assignments, units, cross-references, specification table formats, GPIO mux table formats, etc.

Notable changes for SiWN917 NCP Module v0.7 Datasheet are:
• Replaced references to "ThreadArch" with "Network Wireless Processor" and / or "NWP"
• Changed AI/ML mentions to more directly refer to the MVP block capabilities
• Updated typical electrical characteristics with characterization results
• Normalized pin names for SPI Secondary to HSPI Secondary to match documentation and software
• Removed non-implemented peripherals from block diagrams and text
• 7.1 Absolute Maximum Ratings: Added absolute maximum voltage and current ratings for I/O pins
• 7.3.2 Power On Control (POC) and Reset Clarified POC and Reset functionality
• Minor corrections in the 7.4.1 clock specifications
• 32KHz crystal details and description changed, note added
• 7.5 RF Characteristics Added supported WLAN channels for different regions
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Impact on Form, Fit, Function, Quality, Reliability

• Form – No change
• Fit – No change
• Quality – No change
• Reliability – No Change
• Function: There has been a change in RF performance for WLAN and BLE. Also, there are some changes in the WLAN current consumption & MCU power consumption data. Please refer to the sections mentioned below in the datasheets for more details.

SiWG917 Wireless (SoC) Module v0.7 Datasheet
• Sections and sub-sections of 7.6 (7.6.1.1, 7.6.2, 7.6.3) for updated WLAN and BLE Tx/Rx (7.6.4, 7.6.7, 7.6.8, 7.6.9) typical Data
• Section 7.7.1 for updated WLAN 2.4GHz current consumption Data and 7.7.3 for MCU Power consumption data

SiWN917 NCP Module v0.7 Datasheet
• Sections and sub-sections of 7.5 (7.5.1.1, 7.5.2, 7.5.3) for updated WLAN Tx/Rx and BLE Tx/Rx (7.5.4, 7.5.7, 7.5.8, 7.5.9) Tx/Rx typical Data
• Section 7.6.1 for updated WLAN 2.4GHz current consumption Data

Product Identification

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Existing Part #
SIWG917Y110LGABA
SIWG917Y110LGABAR
SIWG917Y110LGNBA
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SIWG917Y110LGNBAR
SIWG917Y111MGABA
SIWG917Y111MGABAR
SIWG917Y111MGNBA
SIWG917Y111MGNBAR
SIWG917Y121MGABA
SIWG917Y121MGABAR
SIWG917Y121MGNBA
SIWG917Y121MGNBAR
SIWN917Y100LGABA
SIWN917Y100LGABAR
SIWN917Y100LGNBA
SIWN917Y100LGNBAR
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Last Date of Unchanged Product: Mar 12, 2025

Qualification Samples

N/A

Customer Response

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change, Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.

Customers may approve early PCN acceptance by emailing approval, along with PCN # to PCN@silabs.com

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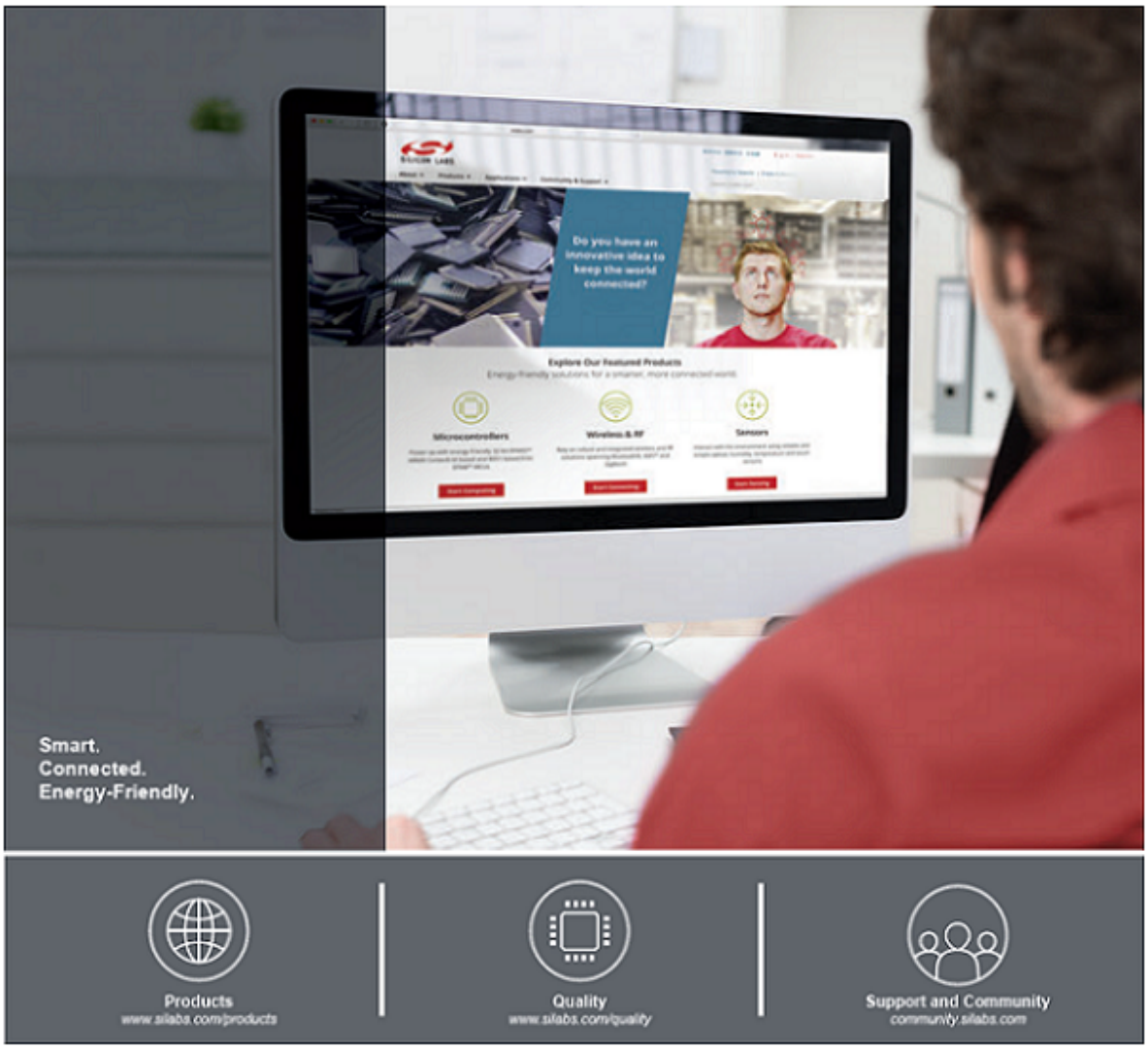
Qualification Data

N/A



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