Bulletin #1512071

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Bulletin Date: 12/7/2015	**Bulletin Effective Date:** 12/7/2015	
Title: C8051F58x C8051F59x Rev1.3 Data Sheet		
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Bulletin Details

Description:
Silicon Labs is pleased to announce that version 1.3 of the C8051F58x/59x data sheet is now available. All items below have been included in this revision of the data sheet. The revision includes:

Power-On Reset may fail for devices shipped prior to date code 1124

- Added a note regarding an issue with /RST low time on some older devices to section 17.1 Power-On Reset on page 153.

This issue was previously documented in the errata and has now been moved to the data sheet section 17.1 Power-On Reset on page 153. It has been removed from the errata.

Note: For devices with a date code before year 2011, work week 24 (1124), if the /RST pin is held low for more than 1 second while power is applied to the device, and then /RST is released, a percentage of devices may lock up and fail to execute code. Toggling the /RST pin does not clear the condition. The condition is cleared by cycling power. Most devices that are affected will show the lock up behavior only within a narrow range of temperatures (a 5 to 10 degrees C window). Parts with a date code of year 2011, work week 24 (1124) or later do not have any restrictions on /RST low time. The date code of a device is a four-digit number on the bottom-most line of each device with the format YYWW, where YY is the two-digit calendar year and WW is the two digit work week.

Use VDD Monitor low threshold setting during normal operation

– Added the note regarding the voltage regulator and VDD monitor in the high setting from section 17.2 Power-Fail Reset/VDD Monitor on page 154 to section 10 Voltage Regulator (REG0) on page 89 and section 15.4.1 VDD Maintenance and the VDD monitor on page 143.

This note already existed in section 17 Reset Sources on page 152, and has been added to additional locations to make it more prominent.

Note: The output of the internal voltage regulator is calibrated by the MCU immediately after any reset event. The output of the un-calibrated internal regulator could be below the high threshold setting of the VDD Monitor. If this is the case and the VDD Monitor is set to the high threshold setting and if the MCU receives a non-power on reset (POR), the MCU will remain in reset until a POR occurs (i.e., VDD Monitor will keep the device in reset). A POR will force the VDD Monitor to the low threshold setting which is guaranteed to be below the un-calibrated output of the internal regulator. The device will then exit reset and resume normal operation. It is for this reason Silicon Labs strongly recommends that the VDD Monitor is always left in the low threshold setting (i.e. default value upon POR).

Use VDD Monitor high setting only when writing Flash

– Updated step 4 in section 15.4.1 VDD Maintenance and the VDD monitor on page 143 to mention using the VDD monitor in the high setting during flash write/erase operations. To ensure the highest system reliability, firmware can change the VDD Monitor high threshold, and the system must use an external supply monitor.

This step previously mentioned using the VDD monitor, but did not specify that the VDD monitor must be in the high setting in order to write to flash.

Note: The output of the internal voltage regulator is calibrated by the MCU immediately after any reset event. The output of the un-calibrated internal regulator could be below the high threshold setting of the VDD Monitor. If this is the case, and the MCU receives a non-power on reset (POR) when the VDD Monitor is set to the high threshold setting, the MCU will remain in reset until a POR occurs (i.e., VDD Monitor will keep the device in reset). A POR will force the VDD Monitor to the low threshold setting, which is guaranteed to be below the un-calibrated output of the internal regulator. The device will then exit reset and resume normal operation. It is for this reason Silicon Labs strongly recommends that the VDD Monitor is always left in the low threshold setting (i.e. default value upon POR). When programming the Flash in-system, the VDD Monitor must be set to the high threshold setting. To prevent this issue from happening and ensure the highest system reliability, firmware can change the VDD Monitor high threshold, and the system must use an external supply monitor. For instructions on how to do this, see “Reprogramming the VDD Monitor High Threshold” on page 138.

Set ZTCEN before entering oscillator suspend

– Updated the SUSPEND bit description in SFR Definition 19.2 OSCICN register on page 179 to mention that firmware must set the ZTCEN bit in SFR Definition 8.1 REF0CN on page 76 before entering suspend.

This information was already present as a note in data sheet section 16.3 Suspend Mode on page 150, and has been added to the bit description to make it more prominent.

> Internal Oscillator Suspend Enable Bit
> Before entering suspend mode, firmware must set the ZTCEN bit in REF0CN

IFRDY flag does not accurately reflect the state of the oscillator

– Added a note to the IFRDY flag in the SFR Definition 19.2 OSCICN register on page 179 that the flag may not accurately reflect the state of the oscillator.

> IFRDY Internal Oscillator Frequency Ready Flag.
> Note: This flag may not accurately reflect the state of the oscillator. Firmware should not use this flag to determine if the oscillator is running.

VDD ramp time max 1 ms for power on specification

– Added VDD Ramp Time max 1 ms for Power On spec to Table 5.4 Reset Electrical Characteristics on page 48.

This specification was previously mentioned in section 15.4.1 V_{DD} Maintenance and the V_{DD} monitor on page 143. It is now added to the electrical specifications to make it more prominent.

Limited cold programming temperature range for industrial grade (-I) devices

– Added a note regarding programming at cold temperatures on –I devices to section 15.1 Programming The Flash Memory on page 138 and added Temperature during Programming Operations specification to Table 5.5 Flash Electrical Characteristics on page 48.

This specification was previously documented in the errata and has now been moved to the data sheet. It has been removed from the errata.
For –I (Industrial Grade) parts, parts programmed at a cold temperature below 0 °C may exhibit weakly programmed flash memory bits. If programmed at 0 °C or higher, there is no problem reading Flash across the entire temperature range of -40 °C to 125 °C. This temperature restriction does not apply to –A (Automotive Grade) devices.

VREF pin cannot operate as open-drain when VDD selected as reference source

– Added a note regarding P0.0/VREF when VDD is used as the reference to Table 20.1 Port I/O Assignment for Analog Functions on page 191 and to the description of the REFSL bit in SFR Definition 8.1 REF0CN register on page 76.

This issue was previously documented in the errata and has now been moved to the data sheet. It has been removed from the errata.

> If VDD is selected as the voltage reference in the REF0CN register and the ADC is enabled in the ADC0CN register, the P0.0/VREF pin cannot operate as a general purpose I/O pin in open-drain mode. With the above settings, this pin can operate in push-pull output mode or as an analog input.

GPIO may have indeterminate state for fast VIO ramp

– Added a note regarding a potential unknown state on GPIO during power up if VIO ramps significantly before VDD to section 20 Port Input/Output on page 188 and section 17 Reset Sources on page 152.

Note: When VIO rises faster than VDD, which can happen when VREGIN and VIO are tied together, a delay created between GPIO power (VIO) and the logic controlling GPIO (VDD) results in a temporary unknown state at the GPIO pins. Cross coupling VIO and VDD with a 4.7 µF capacitor mitigates the root cause of the problem by allowing VIO and VDD to rise at the same rate.

Set FLEWT bit before writing or erasing flash

– Added steps to set the FLEWT bit in the SFR Definition 15.3 FLSCL register on page 147 in section 15.1.3 Flash Erase Procedure on page 139, section 15.1.4 Flash Write Procedure on page 139, and section 15.1.5 Flash Write Optimization on page 140.

This requirement was previously documented in the bit description for the FLEWT bit, and it's been added to the procedures to make it more prominent.

> FLEWT Flash Erase Write Time Control.
> This bit should be set to 1b before Writing or Erasing Flash.
> 0: Short Flash Erase / Write Timing.
> 1: Extended Flash Erase / Write Timing.

Change VDD monitor to high threshold and use external supply monitor for systems that require programming flash in-system

- Added a section regarding steps to reprogram the VDD monitor high threshold in section 15.1.1 Reprogramming the VDD Monitor High Threshold on page 138.
- Recommendation is to add external supply monitor for systems that require programming flash in-system on section 15.1.1 Reprogramming the VDD Monitor High Threshold on page 138.

The output of the internal voltage regulator is calibrated by the MCU immediately after any reset event. The output of the un-calibrated internal regulator could be below the high threshold setting of the VDD Monitor.
If this is the case and the VDD Monitor is set to the high threshold setting and if the MCU receives a non-power on reset (POR), the MCU will remain in reset until a POR occurs (i.e., VDD Monitor will keep the device in reset). A POR will force the VDD Monitor to the low threshold setting which is guaranteed to be below the un-calibrated output of the internal regulator. The device will then exit reset and resume normal operation. It is for this reason Silicon Labs strongly recommends that the VDD Monitor is always left in the low threshold setting (i.e. default value upon POR). When programming the Flash in-system, the VDD Monitor must be set to the high threshold setting.

To prevent this issue from happening and ensure the highest system reliability, firmware can change the VDD
Monitor high threshold and use an external supply monitor that meets the Flash VDD requirement listed in Table 5.5 on page 48. To change the VDD Monitor high threshold, perform the following steps:
1. Disable interrupts.
2. Write 0x01 to the SFRPAGE register.
3. Copy the value from SFR address 0x93 to SFR address 0x94.
4. Return the SFRPAGE register to its previous value.

VDD monitor may trigger on fast VDD changes

– Added a note regarding fast changes on VDD causing the VDD Monitor to trigger to section 17.2 Power-Fail Reset/V_{DD} Monitor on page 154.

Note: The VDD Monitor may trigger on fast changes in voltage on the VDD pin, regardless of whether the voltage increased or decreased.

UART TX THRE0 bit may return incorrect status

– Added notes regarding UART TX and RX behavior in section 24.3.1 Data Transmission on page 259, section 24.3.2 Data Reception on page 259.

Note: THRE0 can have a momentary glitch high when the UART Transmit Holding Register is not empty. The glitch will occur sometime after SBUF0 was written with the previous byte and does not occur if THRE0 is checked in the instruction(s) immediately following the write to SBUF0. When firmware writes SBUF0 and SBUF0 is not empty, TX0 will be stuck low until the next device reset. Firmware should use or poll on TI0 rather than THRE0 for asynchronous UART writes that may have a random delay in between transactions.

UART RX may overrun on simultaneous FIFO read/write

– Added notes regarding UART RX behavior in section 24.3.2 Data Reception on page 260.

Note: The UART Receive FIFO pointer can be corrupted if the UART receives a byte and firmware reads a byte from the FIFO at the same time. When this occurs, firmware will lose the received byte and the FIFO receive overrun flag (OVR0) will also be set to 1. Systems using the UART Receive FIFO should ensure that the FIFO isn't accessed by hardware and firmware at the same time. In other words, firmware should ensure to read the FIFO before the next byte is received.

Included crystal oscillator electrical characteristics

– Added Table 5.8 Crystal Oscillator Electrical Characteristics on page 50. The table includes crystal frequency and crystal drive current specifications.

This information was not documented in the data sheet before.

Use software-controlled startup sequence to reliably start crystal oscillator

– Added a note regarding surface mount crystals and drive current in section 19.4.1 External Crystal Example on page 185

Note: Small surface mount crystals can have maximum drive level specifications that are exceeded by the above XFCN recommendations. In these cases, a software-controlled startup sequence may be used to reliably start the crystal using a higher XFCN setting, and then lowering the XFCN setting once the oscillator has started to reduce the drive level and prevent damage or premature aging of the crystal. In all cases, the drive level should be measured to ensure that the crystal is being driven within its operational guidelines as part of robust oscillator system design. Contact technical support for additional details and recommendations if using surface mount crystals with these devices.

No delay requirement after enabling VDD monitor and before enabling it as reset source

– Removed recommendations to introduce a delay after enabling the VDD Monitor before enabling it as a reset source in 17.2 Power-Fail Reset/V_{DD} Monitor on page 154.

The step "If necessary, wait for VDD monitor to stabilize" in the previous data sheet was removed.

Reason:
Clarification of device behavior and inclusion of data sheet version 1.2 errata.

Product Identification:

C8051F580-IQ	C8051F580-IQR	C8051F580-AQ	C8051F580-AQR
C8051F580-IM	C8051F580-IMR	C8051F580-AM	C8051F580-AMR
C8051F581-IQ	C8051F581-IQR	C8051F581-AQ	C8051F581-AQR
C8051F581-IM	C8051F581-IMR	C8051F581-AM	C8051F581-AMR
C8051F582-IQ	C8051F582-IQR	C8051F582-AQ	C8051F582-AQR
C8051F582-IM	C8051F582-IMR	C8051F582-AM	C8051F582-AMR
C8051F583-IQ	C8051F583-IQR	C8051F583-AQ	C8051F583-AQR
C8051F583-IM	C8051F583-IMR	C8051F583-AM	C8051F583-AMR
C8051F584-IQ	C8051F584-IQR	C8051F584-AQ	C8051F584-AQR
C8051F584-IM	C8051F584-IMR	C8051F584-AM	C8051F584-AMR
C8051F585-IQ	C8051F585-IQR	C8051F585-AQ	C8051F585-AQR
C8051F585-IM	C8051F585-IMR	C8051F585-AM	C8051F585-AMR
C8051F586-IQ	C8051F586-IQR	C8051F586-AQ	C8051F586-AQR
C8051F586-IM	C8051F586-IMR	C8051F586-AM	C8051F586-AMR
C8051F587-IQ	C8051F587-IQR	C8051F587-AQ	C8051F587-AQR
C8051F587-IM	C8051F587-IMR	C8051F587-AM	C8051F587-AMR
C8051F588-IM	C8051F588-IMR	C8051F588-AM	C8051F588-AMR
C8051F589-IM	C8051F589-IMR	C8051F589-AM	C8051F589-AMR
C8051F590-IM	C8051F590-IMR	C8051F590-AM	C8051F590-AMR
C8051F591-IM	C8051F591-IMR	C8051F591-AM	C8051F591-AMR

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