Bulletin #1607081

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Bulletin Date: 7/8/2016	**Bulletin Effective Date:** 7/8/2016
Title: EFM32PG1 Pearl Gecko and EFM32JG1 Jade Gecko Revision C0	

Bulletin Details

Description:
Silicon Labs is pleased to announce product revision C of the EFM32PG1 Pearl Gecko and EFM32JG1 Jade Gecko 32-bit MCU families. After the effective date of this PCN, Silicon Labs plans to deliver Revision C for customers ordering Revision B. Datasheets, reference manuals, and errata have been updated for these products. The new revision is a pin-compatible replacement for the previous revision devices. In addition, Revision C introduces new extended temperature grade OPNs.

Please see attached Qualification Report in the Appendix.

The datasheets are updated to version 0.95 and the reference manuals are updated to version 0.6. The Revision C errata documents and updated Errata History documents are also available. Revision C eliminates the following errata in revision B:

Errata #	Designator	Title/Problem	Workaround Exists	Affected Revision	Fixed Revision
1	CUR_E201	EM2 and EM3 Current Consumption	No	B	Specifications updated in revision 0.95 of the Data Sheet to match the measured values.
2	CUR_E202	EM2/3 Current Consumption at Cold Temperatures	No	B	B, date code 1547 (November 16, 2015)
3	GPIO_E201	GPIO Default Slew Rate	Yes	B	B, date code 1603 (January 18, 2016)
4	DCDC_E201	DCDC Stops Regulating During a Fast EM0/1 to EM2/3/4H Transition	Yes	B	C

Reason:
Revision C is the full production (FP) version of all OPNs in the EFM32PG1 and EFM32JG1 families.

Product Identification:

Affected Revision B0 OPN	New Revision C0 OPN
EFM32PG1B200F256GM48-B0	EFM32PG1B200F256GM48-C0
EFM32PG1B200F128GM48-B0	EFM32PG1B200F128GM48-C0
EFM32PG1B200F256GM32-B0	EFM32PG1B200F256GM32-C0
EFM32PG1B200F128GM32-B0	EFM32PG1B200F128GM32-C0

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EFM32PG1B100F256GM32-B0	EFM32PG1B100F256GM32-C0
EFM32PG1B100F128GM32-B0	EFM32PG1B100F128GM32-C0
EFM32JG1B200F256GM48-B0	EFM32JG1B200F256GM48-C0
EFM32JG1B200F128GM48-B0	EFM32JG1B200F128GM48-C0
EFM32JG1B200F256GM32-B0	EFM32JG1B200F256GM32-C0
EFM32JG1B200F128GM32-B0	EFM32JG1B200F128GM32-C0
EFM32JG1B100F256GM32-B0	EFM32JG1B100F256GM32-C0
EFM32JG1B100F128GM32-B0	EFM32JG1B100F128GM32-C0
EFM32PG1B200F256GM48-B0R	EFM32PG1B200F256GM48-C0R
EFM32PG1B200F128GM48-B0R	EFM32PG1B200F128GM48-C0R
EFM32PG1B200F256GM32-B0R	EFM32PG1B200F256GM32-C0R
EFM32PG1B200F128GM32-B0R	EFM32PG1B200F128GM32-C0R
EFM32PG1B100F256GM32-B0R	EFM32PG1B100F256GM32-C0R
EFM32PG1B100F128GM32-B0R	EFM32PG1B100F128GM32-C0R
EFM32JG1B200F256GM48-B0R	EFM32JG1B200F256GM48-C0R
EFM32JG1B200F128GM48-B0R	EFM32JG1B200F128GM48-C0R
EFM32JG1B200F256GM32-B0R	EFM32JG1B200F256GM32-C0R
EFM32JG1B200F128GM32-B0R	EFM32JG1B200F128GM32-C0R
EFM32JG1B100F256GM32-B0R	EFM32JG1B100F256GM32-C0R
EFM32JG1B100F128GM32-B0R	EFM32JG1B100F128GM32-C0R

This change is considered a minor change which does not affect form, fit, function, quality, or reliability. The information is being provided as a customer courtesy.

Please contact your local Silicon Labs sales representative with any questions about this notification. A list of Silicon Labs sales representatives may be found at www.silabs.com

Customer Actions Needed:
Please qualify and use Rev C0 for any future needs. Revision B0 OPNs listed above are engineering samples and should not be used for Production.

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EFM32PG1BXXX and EFM32JG1BXXX Rev C0
Qualification Report

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Part Rev C0, TSMC Fabrication, SPIL Assembly

Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group A – Accelerated Environment Stress Tests - 7x7 QFN							
HAST	JA110		Q038584	0/43	1		
	130°C, 85%RH	3 lots, N=>25	Q038040	0/28	1	3 lots	Pass
	Vcc=3.8V, 96 hours		Q037588	0/25	1	0/96	
UHAST	JA110		Q038123	0/28	1		
	130°C, 85%RH	3 lots, N=>25	Q038039	0/28	1	3 lots	Pass
	Vcc=3.8V, 96 hours		Q037724	0/27	1	0/83	
Temp Cycle	JA104		Q037586	0/25	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q038041	0/28	1	3 lots	Pass
	500 cycles		Q038121	0/27	1	0/80	
HTSL	JA103		Q038038	0/28	1		
	150°C, 1000hr	3 lots, N=>25	Q038124	0/28	1	3 lots	Pass
			Q037590	0/25	1	0/81	
Test Group A – Accelerated Environment Stress Tests - 5x5 QFN							
HAST	JA110		Q038584	0/43	1		
	130°C, 85%RH	3 lots, N=>25	Q038040	0/28	1	3 lots	Pass
	Vcc=3.8V, 96 hours		Q037588	0/25	1	0/96	
UHAST	JA110		Q038014	0/35	1		
	130°C, 85%RH	3 lots, N=>25	Q038013	0/35	1	3 lots	Pass
	Vcc=3.8V, 96 hours		Q037772	0/27	1	0/97	
Temp Cycle	JA104		Q037776	0/27	1		
	Cond C: -65°C to 150°C	3 lots, N=>25	Q038010	0/35	1	3 lots	Pass
	500 cycles		Q038009	0/35	1	0/97	
HTSL	JA103		Q038012	0/35	1		
	150°C, 1000hr	3 lots, N=>25	Q038011	0/35	1	3 lots	Pass
			Q037774	0/27	1	0/97	
Test Group B – Accelerated Lifetime Simulation Tests							
HTOL			Q038136	0/80			
	JA108		Q038102	0/53			
	$T_J \geq 125°C$, Dynamic	3 lots, N=>77	Q037998	0/78		4 lots	Pass
	Vcc=3.8V, 1000 hours		Q037622	0/79		0/290	
LTOL	JA108						
	T_A = -10°C, Dynamic	1 lot, N=>32	Q037624	0/40		1 lots	Pass
	Vcc=3.8V, 1000 hours					0/40	
ELFR			Q038755	0/501			
	JA108		Q037570	0/508			
	$T_J \geq 125°C$, Dynamic	3 lots, N=>500	Q037999	0/507		4 lots	Pass
	Vcc=3.8V, 48 hours		Q038137	0/505		0/2021	

Approved by: K. Torres 1 of 2 Prepared on: 8 June 2016

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EFM32PG1BXXX and EFM32JG1BXXX Rev C0
Qualification Report

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Part Rev C0, TSMC Fabrication, SPIL Assembly							
Test Name	**Test Condition**	**Qualification**	**Lot ID or Start**	**Fail/Pass or End**	**Notes**	**Summary**	**Status**
NVM Endurance, Retention and Operating Life	JESD22-A117		Q038148	0/40	2		
	25°C	3 lots, N=>39	Q038147	0/40	2	3 lots	
	500 hours		Q037725	0/40	2	0/120	Pass
NVM Endurance, Retention and Operating Life			Q038066	0/40	3		
	JESD22-A117		Q038028	0/40	3		
	125°C	3 lots, N=>39	Q038024	1/39	3, 4	4 lots	
	1000 hours		Q037652	0/40	3	1/159	Pass
Test Group E – Electrical Verification							
ESD-HBM	JA114	1 lot, N=>3	Q038744				Class 2
ESD-CDM	JC101	1 lot, N=>3	Q039297		5		Class C3
			Q039296		6		Class C3
Latch Up	JESD78	1 lot, N=>3	Q039298	25 °C	5		Pass
	±100mA		Q039300	25 °C	6		
Latch Up	JESD78	1 lot, N=>3	Q039299	125 °C	5		Pass
	±100mA		Q039301	125 °C	6		

Notes:
1. Parts are Pre-conditioned at MSL2/260°C
2. Preconditioned with 10K write/erase cycles at 25°C
3. Preconditioned with 10K write/erase cycles at 125°C
4. Failure analysis on the failure was inconclusive. An additional 40 units were stressed from the same wafer lot (Q038028) to reduce the LTPD% below the requirment. LTPD% = 5.76 at 90% confidence with 0 fails and a sample size =40. LTPD% = 4.80 at 90% confidence with 1 failure and a sample size = 80.
5. Results for the 7x7 QFN Package
6. Results for the 5x5 package

This report applies to the following part numbers:		
EFM32PG1B100F128GM32-C0	EFM32PG1B200F256GM48-C0	EFM32JG1B200F128GM32-C0
EFM32PG1B100F256GM32-C0	EFM32PG1B200F256IM32-C0	EFM32JG1B200F128GM48-C0
EFM32PG1B100F256IM32-C0	EFM32PG1B200F256IM48-C0	EFM32JG1B200F256GM32-C0
EFM32PG1B200F128GM32-C0	EFM32JG1B100F128GM32-C0	EFM32JG1B200F256GM48-C0
EFM32PG1B200F128GM48-C0	EFM32JG1B100F256GM32-C0	EFM32JG1B200F256IM32-C0
EFM32PG1B200F256GM32-C0	EFM32JG1B100F256IM32-C0	EFM32JG1B200F256IM48-C0

Approved by: K. Torres | 2 of 2 | Prepared on: 8 June 2016

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