Bulletin #1701251

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Bulletin Date: 1/25/2017	**Bulletin Effective Date:** 1/25/2017
Title: C8051F97x Datasheet Update Version 1.1 PB	

Bulletin Details

Description:
Silicon Labs is pleased to announce version 1.1 of the C8051F97x datasheet. This is part of Silicon Labs’ continual improvement process.

The changes in version 1.1 of the datasheet are as follows.

- Updated the QFN-48 and QFN-32 package specifications to higher resolution images and to the latest and more accurate package measurements.
- Added a note in Section "24.3.2. External RC Mode" on page 243 and Section "24.3.3. External Capacitor Mode" on page 245 to further clarify that to calculate the frequency control value when using an external oscillator there is an internal divide-by-2 stage that further reduces the frequency to ensure a properly conditioned system clock.
- Removed a statement in Section "26.3. Priority Crossbar Decoder" on page 281 that stated that the UART0 is the top priority.
- Removed all mention of the ADC0MX channels other than ADC0.0. This is due to the pin selection of the ADC channels (ADC0.n) being made by AMUX0.
- Updated the QFN-32 and QFN-24 pin definition with the correct pin numbering.
- Added RTC Oscillator Output functionality to P0.2 on Table 3.1 “Pin Definitions for C8051F970/3-A-GM (QFN-48)”.
- Added Wake-up Request functionality to P0.3 on Table 3.1 “Pin Definitions for C8051F970/3-A-GM (QFN-48)”.
- Added a note in Register 16.4 “PMU0MD: Power Management Unit Mode” on page 103 that the RTC Oscillator Output and Wake-up Request functionality are not available on the QFN-32 and QFN-24 packages.
- Removed a mention of UART0 routing to pins P0.4 and P0.5 in Register 26.1 “XBR0: Port I/O Crossbar 0” on page 285.
- Updated Figure 22.4 “DMA Mode Operation Flow Chart,” on page 206 to remove a mention of clearing and checking that ACCMD is 0.
- Added a note in Section "22.6. DMA Mode Operation" on page 205 to clarify what is needed to generate the MAC output for two arrays.
- Changed all references and mentions of QFN-28 to QFN-24.
- Added a note to Section "16.5. Sleep Mode" on page 97 that entering sleep mode may cause a device to disconnect while debugging.
- Swapped values 6 and 7 in the PERIPH field in Register 21.6, “DMA0NCF: DMA0 Channel Configuration” on page 195.
- Updated references to MSTEN to refer to SPI0CFG instead of SPI0CN in Section "28. Serial Peripheral Interface (SPI0)" on page 328.
- Updated the example in Section "22.11.3. Initializing Memory Block Using DMA0 and MAC0" on page 212 to refer to the MAC0ITER register instead of MAC0ICT.
- Removed Section 24.4.2 “SMBus Pin Swap” and 29.4.3 “SMBus Timing Control” because these features are not available on this device family.

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Reason:
Version 1.1 C8051F97x Datasheet release

Product Identification:
C8051F970-A-GM
C8051F970-A-GMR
C8051F971-A-GM
C8051F971-A-GMR
C8051F972-A-GM
C8051F972-A-GMR
C8051F973-A-GM
C8051F973-A-GMR
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C8051F974-A-GMR
C8051F975-A-GM
C8051F975-A-GMR

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