



Revision Change Notice #1605201

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PCN Issue Date: 5/20/2016	Effective Date: 6/20/2016
Title: EFM8BB3x Revision B	
PCN Type: ☒ Datasheet ☒ Product Revision	
PCN Details	

Description of Change:

Silicon Labs is pleased to announce revision B of the EFM8BB3x devices, revision 0.3 of the corresponding datasheet, revision 0.3 of the corresponding Reference Manual, revision 0.4 of the corresponding errata, and revision 0.1 of the corresponding errata history for these products.

Revision B ChangesCrystal Mode in External Oscillator is available in revision B

In revision A, crystal mode in the external oscillator option is not available. It is available in revision B.

VREF/P0.0 output can be retained in revision B

VREF/P0.0 output on revision A devices is not retained if the PINRETAIN bit in PCON1 is set (in addition to the RSTMD bit in the DAC) and drops from its level to 0 V on any non-POR reset. This problem has been fixed in revision B.

Timer 3/4 chaining mode in suspend works in all system clock divider settings in revision B

The Timer 3/4 32-bit counter on revision A devices does not switch to the low frequency oscillator (LFOSC0) after entering suspend mode if the system clock divider is set to a value of divide-by-4 or greater. This problem has been fixed in revision B. Timer 3/4 chaining mode in suspend mode works in all system clock divider values.

CLU wake-up sources are edge triggered in revision B

CLU interrupt-enabled Suspend or Snooze wake-up sources are level triggered on revision A devices. On revision B devices these wake sources are edge triggered as described in device reference manual.

I2CSLAVE0 can distinguish between multiple addresses in revision B

I2CSLAVE0 can respond to multiple slave addresses and distinguish between these addresses using the receive FIFO when the ADDRCHK bit in I2C0CN0 is set to 1 in revision B. The ADDRCHK bit is not available on revision A devices.

REVID SFR will read 0x01 in revision B

The reset value of REVID SFR will read 0x01 in revision B instead of 0x00 in revision A

Revision 0.3 Data Sheet ChangesDebug section

Added figure 5.2 in section 5.2 to describe the debug connections that are required.

UART bootloader information

Added information about the UART bootloader in Section 3.10 Bootloader

Bootloader User Guide reference

Added a reference to AN945: EFM8 Factory Bootloader User Guide in Section 3.10 Bootloader

Pre-programmed UART bootloader

Added pre-programmed UART bootloader in Section 1 Feature List

Revision B part numbers



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Updated all orderable part numbers to revision B part numbers in Table 2.1 Product Selection Guide (note: added one part number that was not in Rev A EFM8BB31F16G-B-QFN24)

Crystal mode in external oscillator

Specified external crystal/RC oscillator feature in Section 1 Feature List and Section 3.4 Clocking

QFN32 PCB land pattern

Adjusted C1, C2 X2, Y2, and Y1 maximum dimensions in Section 7.2 QFN32 PCB Land Pattern

QFN32 and QSOP24 package markings

Adjusted package markings for QFN32 package in Section 7.3 QFN32 Package Marking and QSOP24 package in Section 10.3 QSOP24 Package Marking

DAC differential nonlinearity min/max

Changed DAC differential nonlinearity minimum from TBD to -1 and maximum from TBD to 1 in Table 4.12 DACs

Revision 0.4 Errata Changes

Revision 0.3 errata #1 XOSC_E101 – Crystal Mode in External Oscillator Not Available has been removed in revision 0.6 errata. The problem has been corrected in revision B of the device.

Revision 0.3 errata #2 RST_E101 – VREF/P0.0 Not Retained through Power-On Reset has been removed in revision 0.4 errata. The problem has been corrected in revision B of the device.

Revision 0.3 errata #3 TIMER_E101 – Timer 3/4 Chaining Mode in Suspend has been removed in revision 0.4 errata. The problem has been corrected in revision B of the device.

Revision 0.3 errata #4 CLU_E101 – CLU Wake-Up Sources are Level Triggered has been removed in revision 0.4 errata. The problem has been corrected in revision B of the device.

Revision 0.3 errata #5 I2CSLAVE_E101 – I2CSLAVE0 Cannot Distinguish Between Multiple Addresses has been removed in revision 0.4 errata. The problem has been corrected in revision B of the device.

Revision 0.3 errata #6 PKG_E101 – Top Marking Right Justified has been removed in revision 0.4 errata. The package marking issue only affects revision A QFP32 devices with a date code of 1531. No revision B devices have been affected.

Revision 0.3 errata #7 PKG_E102 – Devices Marked as G Grade has been removed in revision 0.4 errata. The package marking issue only affects revision A QFP32 devices with a date code of 1540 or 1602. No revision B devices have been affected.

Revision 0.3 errata #8 TEST_E101 – Devices Tested to 85 °C has been removed in revision 0.4 errata. This issue only affects revision A devices with a date codes of 1530, 1531, or 1532. No revision B devices have been affected.

After the effective date of this PCN, Silicon Labs reserves the right to deliver revision B for customers ordering revision A.

Reason for Change:

EFM8BB3x Revision B release
 EFM8BB3x Data sheet Revision 0.3 release
 EFM8BB3x Reference Manual Revision 0.3 release
 EFM8BB3x Errata Revision 0.3 release
 EFM8BB3x Errata History 0.1 release

Impact on Form, Fit, Function, Quality, Reliability:

There is no impact to form, fit, quality or reliability.

The following functions are impacted:

- Crystal Mode in External Oscillator is available in revision B
- VREF/P0.0 output can be retained in revision B
- Timer 3/4 chaining mode in suspend works in all system clock divider settings in revision B
- CLU wake-up sources are edge triggered in revision B
- I2CSLAVE0 can distinguish between multiple addresses in revision B
- The reset value of REVID SFR will read 0x01 in revision B

Product Identification:

Existing Part Number	Replacement Part Number	Drop in Compatible Indicator
EFM8BB31F16G-A-QFN32	EFM8BB31F16G-B-QFN32	Yes
EFM8BB31F16G-A-QFN32R	EFM8BB31F16G-B-QFN32R	Yes
EFM8BB31F16G-A-QFP32	EFM8BB31F16G-B-QFP32	Yes
EFM8BB31F16G-A-QFP32R	EFM8BB31F16G-B-QFP32R	Yes
EFM8BB31F16G-A-QSOP24	EFM8BB31F16G-B-QSOP24	Yes
EFM8BB31F16G-A-QSOP24R	EFM8BB31F16G-B-QSOP24R	Yes
EFM8BB31F32G-A-QFN24	EFM8BB31F32G-B-QFN24	Yes
EFM8BB31F32G-A-QFN24R	EFM8BB31F32G-B-QFN24R	Yes
EFM8BB31F32G-A-QFN32	EFM8BB31F32G-B-QFN32	Yes
EFM8BB31F32G-A-QFN32R	EFM8BB31F32G-B-QFN32R	Yes
EFM8BB31F32G-A-QFP32	EFM8BB31F32G-B-QFP32	Yes
EFM8BB31F32G-A-QFP32R	EFM8BB31F32G-B-QFP32R	Yes
EFM8BB31F32G-A-QSOP24	EFM8BB31F32G-B-QSOP24	Yes
EFM8BB31F32G-A-QSOP24R	EFM8BB31F32G-B-QSOP24R	Yes
EFM8BB31F64G-A-QFN24	EFM8BB31F64G-B-QFN24	Yes
EFM8BB31F64G-A-QFN24R	EFM8BB31F64G-B-QFN24R	Yes
EFM8BB31F64G-A-QFN32	EFM8BB31F64G-B-QFN32	Yes
EFM8BB31F64G-A-QFN32R	EFM8BB31F64G-B-QFN32R	Yes
EFM8BB31F64G-A-QFP32	EFM8BB31F64G-B-QFP32	Yes
EFM8BB31F64G-A-QFP32R	EFM8BB31F64G-B-QFP32R	Yes
EFM8BB31F64G-A-QSOP24	EFM8BB31F64G-B-QSOP24	Yes
EFM8BB31F64G-A-QSOP24R	EFM8BB31F64G-B-QSOP24R	Yes

Note: The part numbers above include tape and reel variants which are denoted with an "R" at the end of the orderable part number.

Last Date of Unchanged Product: 6/20/2016



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Qualification Samples:

Samples are available now. Please contact your Silicon Labs sales representative to order samples. A list of Silicon Labs sales representatives is available at www.silabs.com.

Specific conditions of acceptance of this change will be considered on a case by case basis if written notice is submitted within 30 days of this notice. To request further data or inquire about this notification, please contact your local Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at www.silabs.com.

In some cases rejection of a change notice may impact Silicon Labs product pricing, delivery, quality, or reliability.

Customer Early Acceptance Sign Off:

Customers may approve early PCN acceptance by completing the information below:

Early Acceptance: Date: _____

 Name: _____

 Company: _____

Email your early Acceptance approval to: katherine.haggard@silabs.com

Qualification Data:

Please see report below.

EFM8BB3* AEC-Q100 Qualification Report

W7101F1 - Product Qualification Report Record
Rev. H

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Part Rev B, GSCM Fabrication							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group A – Accelerated Environment Stress Tests - 32-TQFP - ASECL assembly							
HAST	JA110	3 lots, N=>77	Q038332	0/82	1	3 lots 0/246	Pass
	130°C, 85%RH		Q038502	0/82	1		
	Vcc=3.6V, 96 hours		Q038506	0/82	1		
UHAST	JA110	3 lots, N=>77	Q038334	0/82	1	3 lots 0/244	Pass
	130°C, 85%RH		Q038504	0/82	1		
	Vcc=3.6V, 96 hours		Q038508	0/80	1		
Temp Cycle	JA104	3 lots, N=>77	Q038333	0/86	1	3 lots 0/248	Pass
	Cond C: -65°C to 150°C		Q038501	0/81	1		
	500 cycles		Q038505	0/81	1		
HTSL	JA103	1 lot, N=>45	Q038315	0/46	1	3 lots 0/146	Pass
	150°C, 1000hr		Q038503	0/50	1		
			Q038507	0/50	1		
Test Group A – Accelerated Environment Stress Tests - 24-QSOP - UTACTH assembly							
HAST	JA110	3 lots, N=>77	Q038411	0/78	1	3 lots 0/238	Pass
	130°C, 85%RH		Q036513	0/80	1		
	Vcc=3.6V, 96 hours		Q036515	0/80	1		
UHAST	JA110	3 lots, N=>77	Q038412	0/78	1	3 lots 0/238	Pass
	130°C, 85%RH		Q036526	0/80	1		
	Vcc=3.6V, 96 hours		Q036527	0/80	1		
Temp Cycle	JA104	3 lots, N=>77	Q038413	0/79	1	3 lots 0/239	Pass
	Cond C: -65°C to 150°C		Q036523	0/80	1		
	500 cycles		Q036524	0/80	1		
HTSL	JA103	1 lot, N=>45	Q038366	0/50	1	3 lots 0/106	Pass
	150°C, 1000hr		Q036520	0/28	1		
			Q036521	0/28	1		
Test Group A – Accelerated Environment Stress Tests - 24-QFN - ASECL assembly							
HAST	JA110	3 lots, N=>77	Q038217	0/80	1	3 lots 0/240	Pass
	130°C, 85%RH		Q038218	0/80	1		
	Vcc=3.6V, 96 hours		Q038219	0/80	1		
UHAST	JA110	3 lots, N=>77	Q038223	0/80	1	3 lots 0/240	Pass
	130°C, 85%RH		Q038224	0/80	1		
	Vcc=3.6V, 96 hours		Q038225	0/80	1		
Temp Cycle	JA104	3 lots, N=>77	Q038220	0/80	1	3 lots 0/240	Pass
	Cond C: -65°C to 150°C		Q038221	0/80	1		
	500 cycles		Q038222	0/80	1		
HTSL	JA103	1 lot, N=>45	Q038181	0/48	1	3 lots 0/144	Pass
	150°C, 1000hr		Q038182	0/48	1		
			Q038183	0/48	1		

EFM8BB3* AEC-Q100 Qualification Report


W7101F1 - Product Qualification Report Record
Rev. H

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Part Rev B, GSMC Fabrication							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group A – Accelerated Environment Stress Tests - 32L-UQFN - UTACTH assembly							
HAST	JA110 130°C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>77	Q038160	0/84	1		Pass
			Q038359	0/84	1		
			Q038363	0/85	1	4 lots	
			Q039097	0/87	1	0/340	
UHAST	JA110 130°C, 85%RH Vcc=3.6V, 96 hours	3 lots, N=>77	Q038161	0/85	1		Pass
			Q038360	0/85	1		
			Q038364	0/80	1	4 lots	
			Q039095	0/87	1	0/337	
Temp Cycle	JA104 Cond C: -65°C to 150°C 500 cycles	3 lots, N=>77	Q038158	0/85	1		Pass
			Q038357	0/85	1		
			Q038361	0/85	1	4 lots	
			Q039098	0/98	1	0/353	
HTSL	JA103 150°C, 1000hr	1 lot, N=>45	Q038159	0/50	1		TBD
			Q038358	0/49	1	3 lots	
			Q039096	0/?	1	0/99	
Test Group B – Accelerated Lifetime Simulation Tests							
HTOL	JA108 T _J ≥ 125°C, Dynamic Vcc=3.6V, 1000 hours	3 lots, N=>77	Q038228	0/84			Pass
			Q038640	0/84		3 lots	
			Q038861	0/90		0/258	
LTOL	JA108 -40°C, Dynamic Vcc=3.6V, 1000 hours	1 lot, N=>77	Q036550	0/35		1 lots	Pass
						0/35	
ELFR	AEC-Q100-008 T _J ≥ 125°C, Dynamic Vcc=3.6V, 48 hours	3 lots, N=>800	Q038355	0/842			Pass
			Q038547	0/850		3 lots	
			Q038785	0/840		0/2532	
Data Retention High Temp	AEC-Q100-005 150°C, 1000 hours	3 lots, N=> 39	Q038230	0/44			Pass
			Q038627	0/45		3 lots	
			Q038848	0/49		0/138	
Data Retention Low Temp	AEC-Q100-005 25°C, 1000 hours	3 lots, N=> 38	Q038314	0/39			Pass
			Q038622	0/40		3 lots	
			Q038846	0/45		0/124	
NVM P/E Cycling High Temp	AEC-Q100-005 85°C, 1000 hours	3 lots, N=> 77	Q038193	0/140			Pass
			Q038588	0/140		3 lots	
			Q038790	0/136		0/416	
NVM P/E Cycling Low Temp	AEC-Q100-005 25°C, 1000 hours	3 lots, N=> 77	Q038194	0/40			Pass
			Q038589	0/40		3 lots	
			Q038788	0/45		0/125	

EFM8BB3* AEC-Q100 Qualification Report


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Part Rev B, GSMC Fabrication							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Test Group C – Package Assembly Integrity Tests							
Wire Bond Pull	M-STD-883 Performed post-TC	5 units, N=>30	Q038389	0/5	2	1 lot 0/5	Pass
Wire Bond Pull	M-STD-883 Performed post-TC	5 units, N=>30	Q038470	0/5	3	1 lot 0/5	Pass
Wire Bond Pull	M-STD-883 Performed post-TC	5 units, N=>30	Q038480	0/5	4	1 lot 0/5	Pass
Wire Bond Pull	M-STD-883 Performed post-TC	5 units, N=>30	Q038388	0/5	5	1 lot 0/5	Pass
Test Group E – Electrical Verification							
ESD-HBM	AEC-Q100-002	1 lot, N=>3	Q038341		2		Class 3A
ESD-CDM	AEC-Q100-011	1 lot, N=>3	Q038156		2		Class C6
			Q038118		3		Class C6
			Q038085		4		Class C6
			Q038125		5		Class C6
Latch Up	AEC-Q100-004 ±200mA Overvoltage = 5.4V	1 lot, N=>6	Q038353	25 °C			Pass
			Q038354	105 °C			Pass

Notes:

1. Parts are Pre-conditioned at MSL2/260°C
2. 32-TQFP
3. 24-QSOP
4. 24-QFN
5. 32L-JQFN

This report applies to the following part numbers:	
EFM8BB31F*G-B-QFN24	EFM8BB31F*I-B-QFN24
EFM8BB31F*G-B-QFN32	EFM8BB31F*I-B-QFN32
EFM8BB31F*G-B-QFP 32	EFM8BB31F*I-B-QFP 32
EFM8BB31F*G-B-QSOP 24	EFM8BB31F*I-B-QSOP 24