Clocks for 4.5G Radio Access Networks

SEPTEMBER 2017

Complete Timing Portfolio

- Leader in high performance clocks and oscillators
- Frequency flexibility + ultra-low jitter
- Best-in-class integration → single IC clock trees
- Highly programmable with quick-turn samples

XO/VCXO

Clock Generators

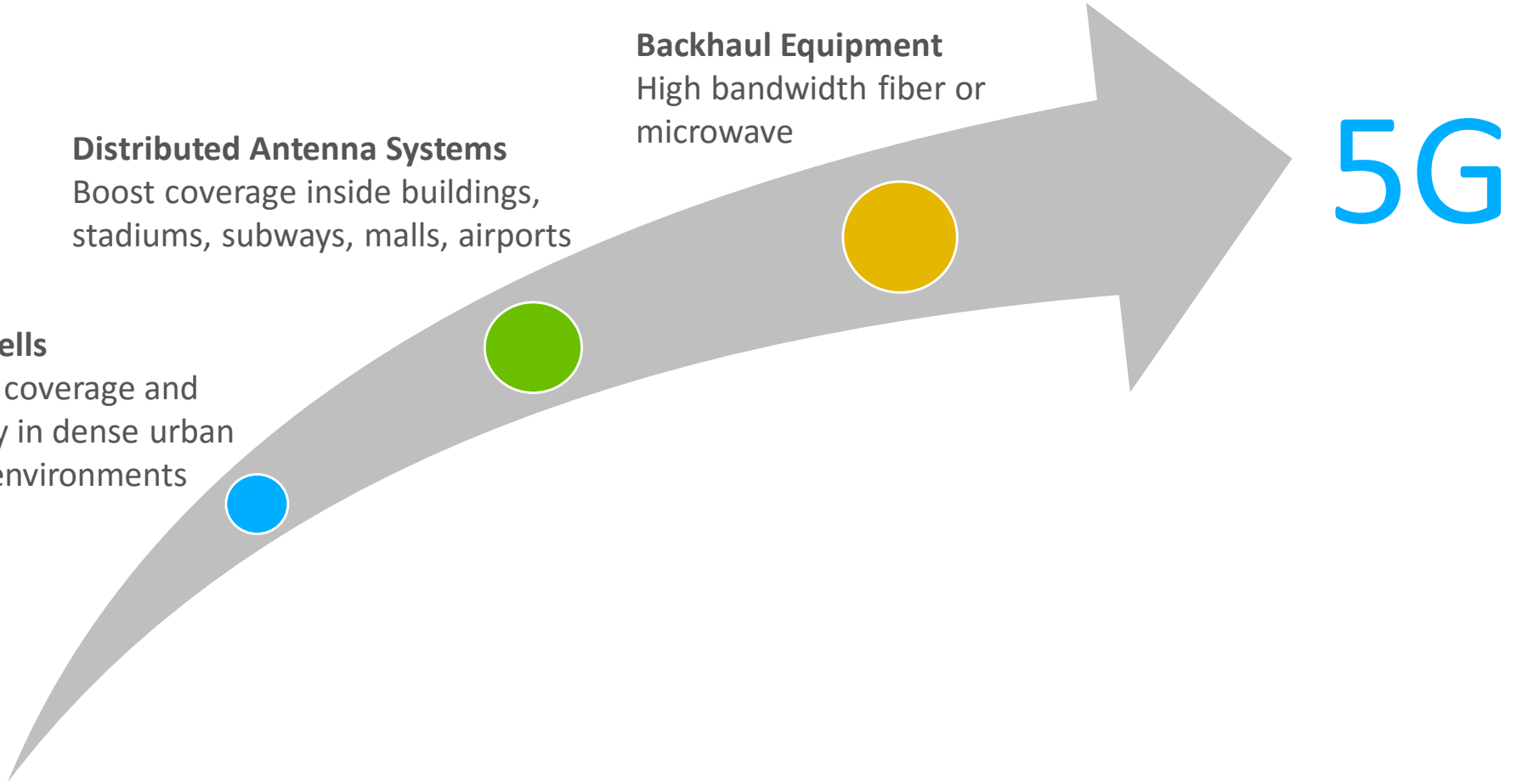
Clock Buffers

Synchronization

Jitter Attenuating Clocks

Wireless Clocks

Road to 5G Starts Now



Timing Focus Markets

	Core / Metro	Data Center	Wireless
Trends	10G → 100G / 400G	40G → 100G Mobile Edge Computing	LTE-Advanced, 4.5G, 5G Massive MIMO, IEEE 1588
Applications	 Core Router  Packet-Optical Transport  Data Center Interconnect	 Servers  Switches  Storage	  Small Cells MDAS   RRH BBU   Fronthaul / Backhaul

SILICON LABS

Delivering optimized timing solutions combining highest performance and integration

History of Innovation

2002 — **Industry's first** jitter attenuating CLK IC

2005 — **Industry's first** quad frequency XO/VCXOs

2007 — **Industry's first** any-rate jitter attenuating CLK

2008 — **Industry's first** any-rate CLK generator

2012 — **Industry's first** multi-format low jitter buffer

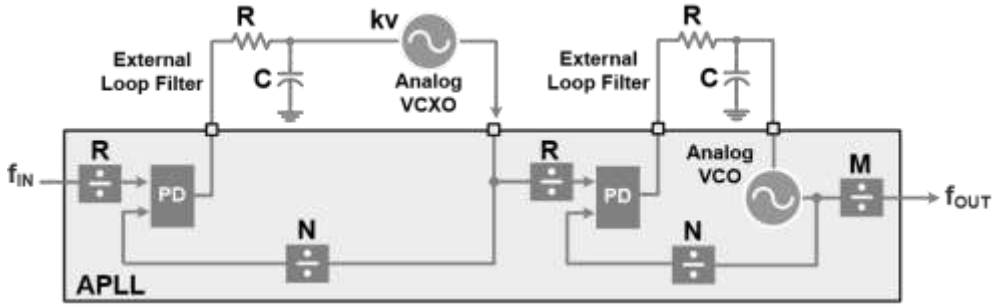
2014 — **Industry's first** 100 fs any-rate jitter attenuating CLK

2016 — **Industry's first** Coherent optical CLK

2017 — **Industry's first** <100 fs any-rate XOs

Available Now! Industry's first LTE + Ethernet CLKs

DSPLL Simplifies Low Jitter Clock Generation



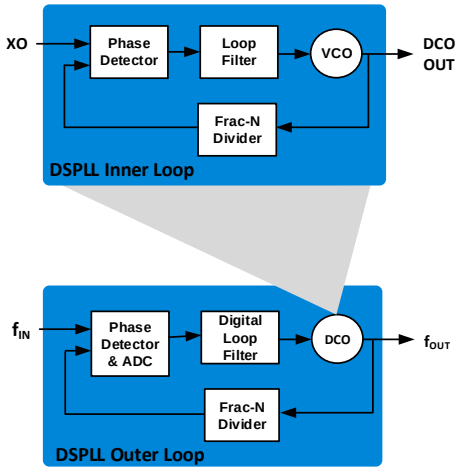
Two-Stage Cascaded PLL:

- 1st stage: jitter cleaning, 2nd stage: clock generation
- Requires discrete VCXO, loop filters, LDOs
- Susceptible to board-level noise coupling
- High power, BiCMOS technology

>100 U.S. and international patents issued or filed for Silicon Labs timing technology

Low Phase Noise Clock Generation

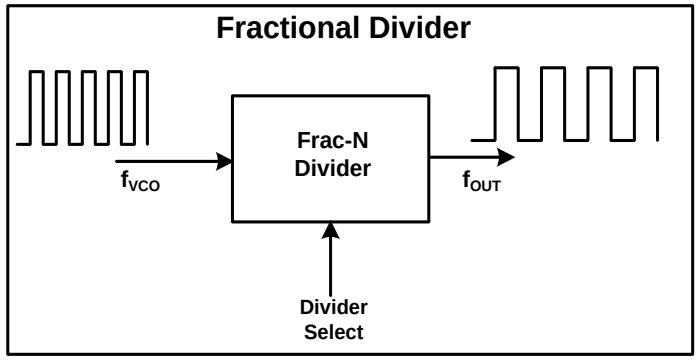
Jitter Cleaning

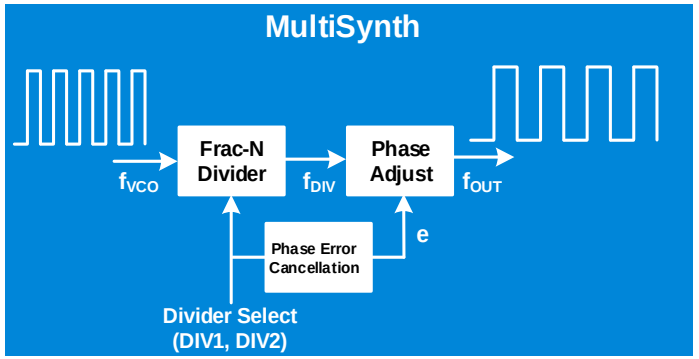


Two-Stage Nested DSPLL:

- Provides jitter cleaning and clock generation
- No external VCXO, loop filters; eliminates VCXO LDO
- Highly immune to board-level noise
- >50% lower power, 55 nm CMOS technology

MultiSynth Technology = Any Frequency Flexibility





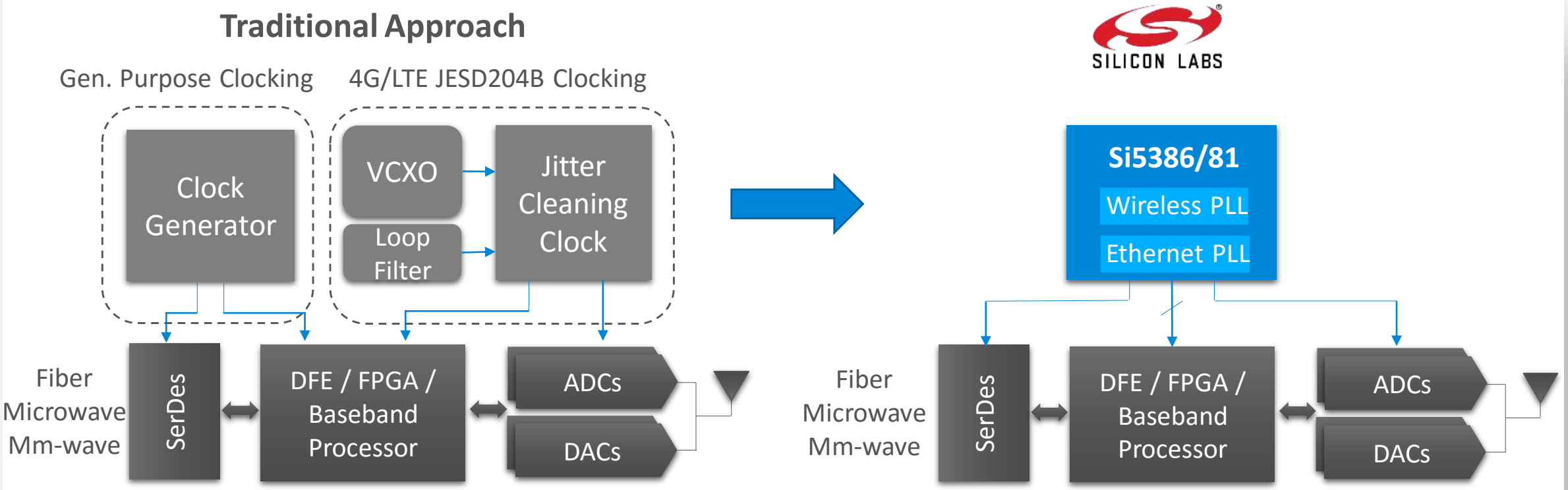
Conventional approach

- Configuration-dependent jitter
- No phase error cancellation
- Highly variable jitter generation
- Non-zero ppm frequency synthesis error

Silicon Labs approach

- Dynamic phase error cancellation minimizes jitter
- Consistent, low jitter operation
- Zero ppm frequency synthesis error
- Any frequency with <100 fs rms jitter

Simplifying Timing For Small Cells, DAS and Backhaul

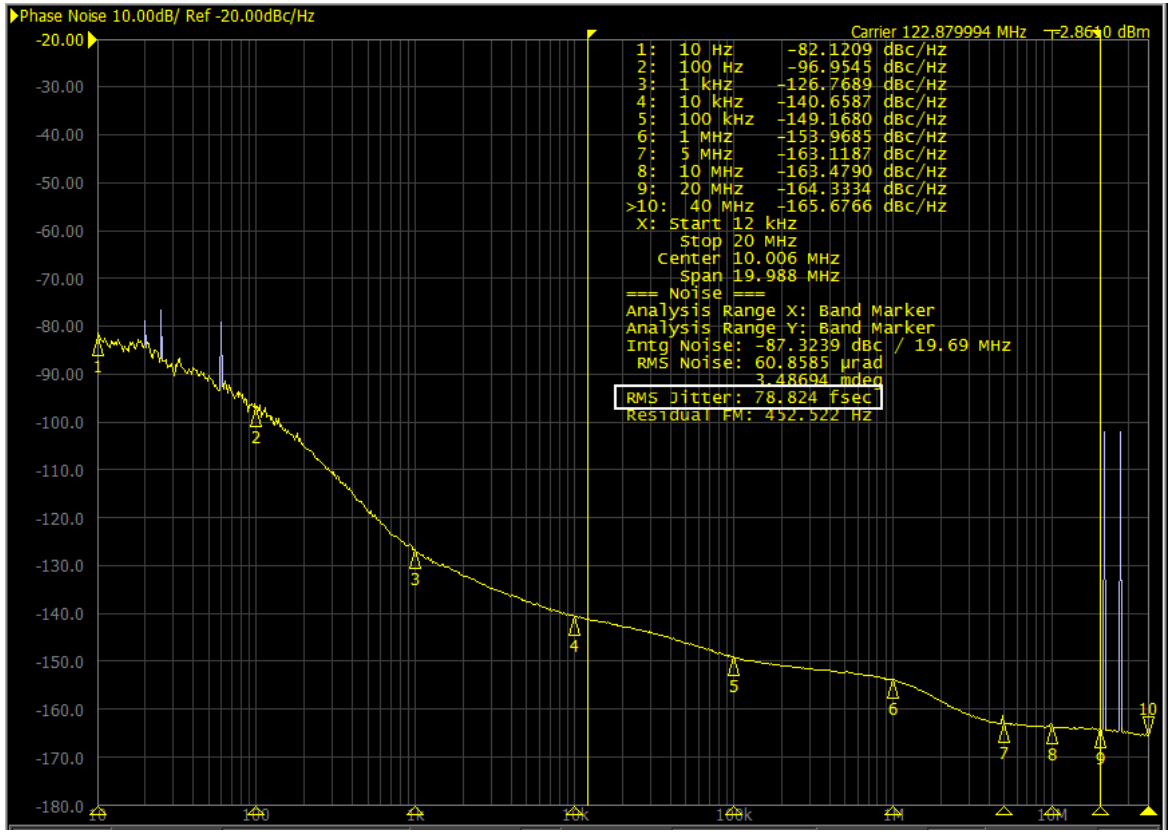


- Requires 2 clock IC's and VCXO
- Not optimized for size, power, cost
- 339 mm^2 PCB area
- 2.4 W power consumption

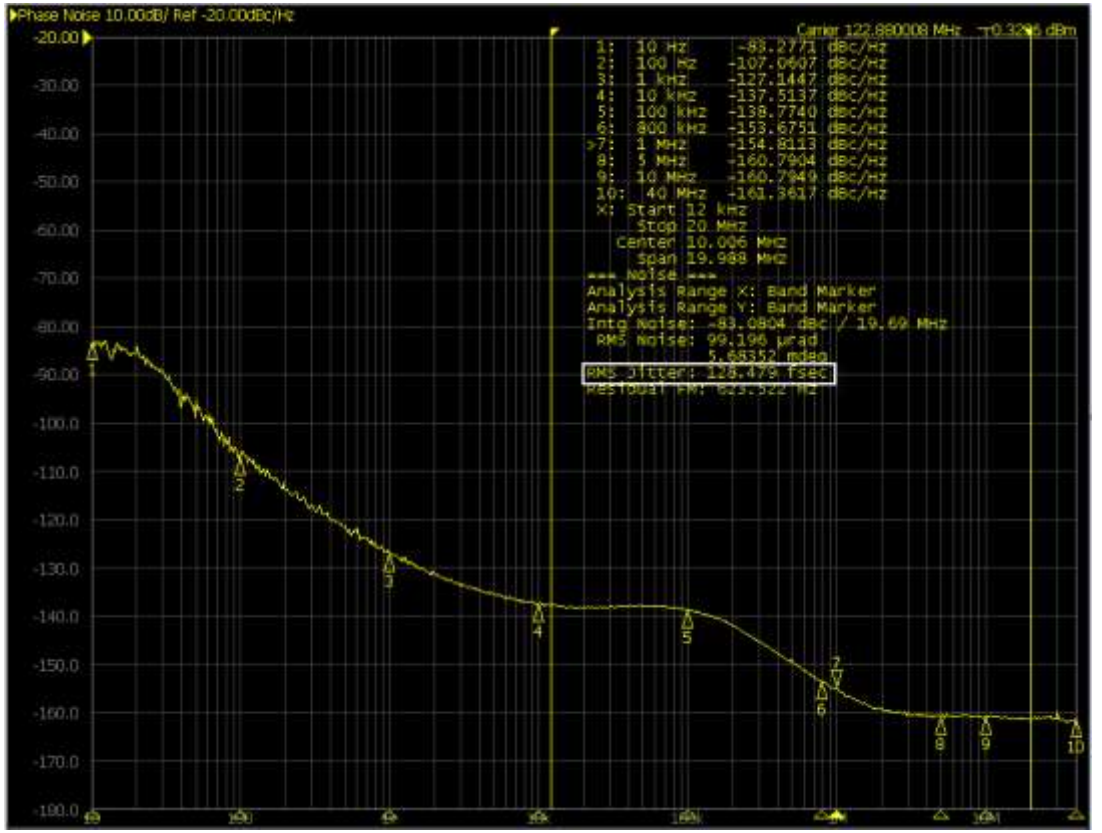
- Single IC → highest integration
- Optimized LTE + Ethernet clocking
- 94 mm^2 PCB area
- 1.1 W power consumption

Low Phase Noise – DSPLL Replaces 30.72 MHz VCXO-Based PLLs

Si538x with no VCXO at 122.88MHz



LMK04828 with 30.72 MHz VCXO at 122.88MHz



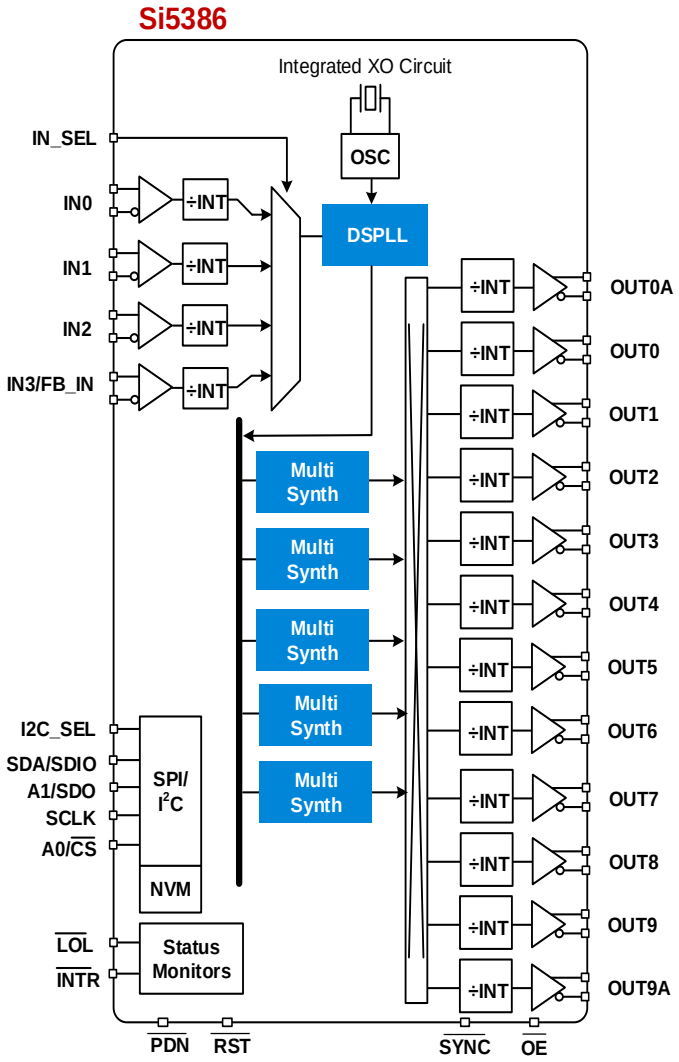
Better performance without the cost and PCB area of a VCXO

The Si538x Integration Advantage is Clear

BOM Components	Cascaded PLL	Si5381/82/86 DSPLL
DUT area	81	81
VCXO area	151	8
Loop filter area	9	0
Power supply filtering	31	4
Fractional Clock IC area	49	0
Other PCB area	18	2
Total PCB footprint	**339 mm^2**	**95 mm^2**
Power Consumption	**2.4 W**	**1.0 – 1.5 W**

70% smaller and 55% lower power than competing devices

Si5386 1-DSPLL Wireless Clock



Part Number	No. of Clock Domains	Clock Inputs/ Outputs	Input Frequency	Output Frequency	Phase Jitter (fs RMS)	PLL Bandwidth	Package
Si5386	5	4/12	7.68 MHz to 750 MHz	100 Hz to 2.94912 GHz	80	10 Hz to 4 kHz	64 LGA 9x9 mm

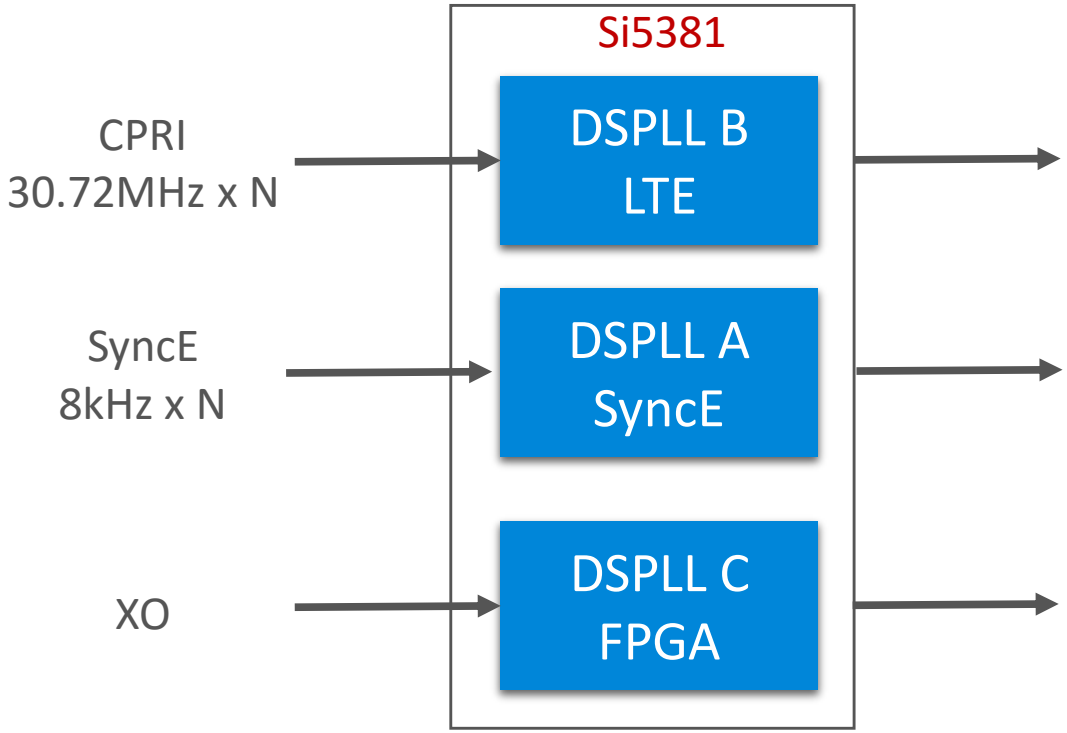
APPLICATIONS

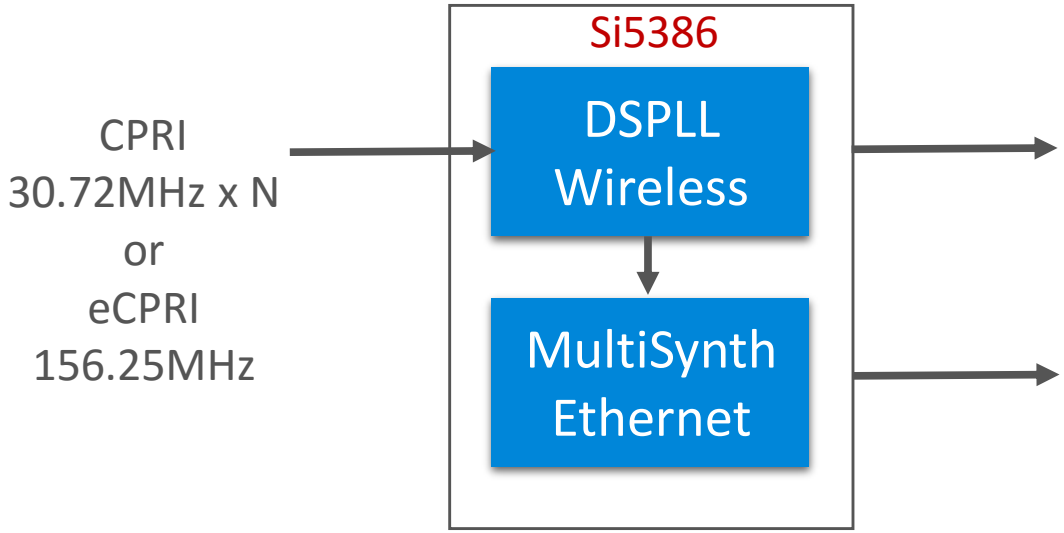
- Small cells
- Pico cells, femto cells
- Fixed wireless
- Distributed Antenna Systems

FEATURES

- 5 independent frequency domains
  - RF transceivers
  - Data converter clocks
  - CPRI, Ethernet, CPU clocks
- No external VCXO, crystal, loop filters
- Hitless switching, holdover
- Optional zero delay mode
- Low phase noise, spurious & jitter
  - Noise floor: -165 dBc/Hz
  - Spur: -103 dBc @ 122.88 MHz
  - 80 fs RMS jitter
- Configurable swing: 200-3200 mVpp

New Solutions for Wireless

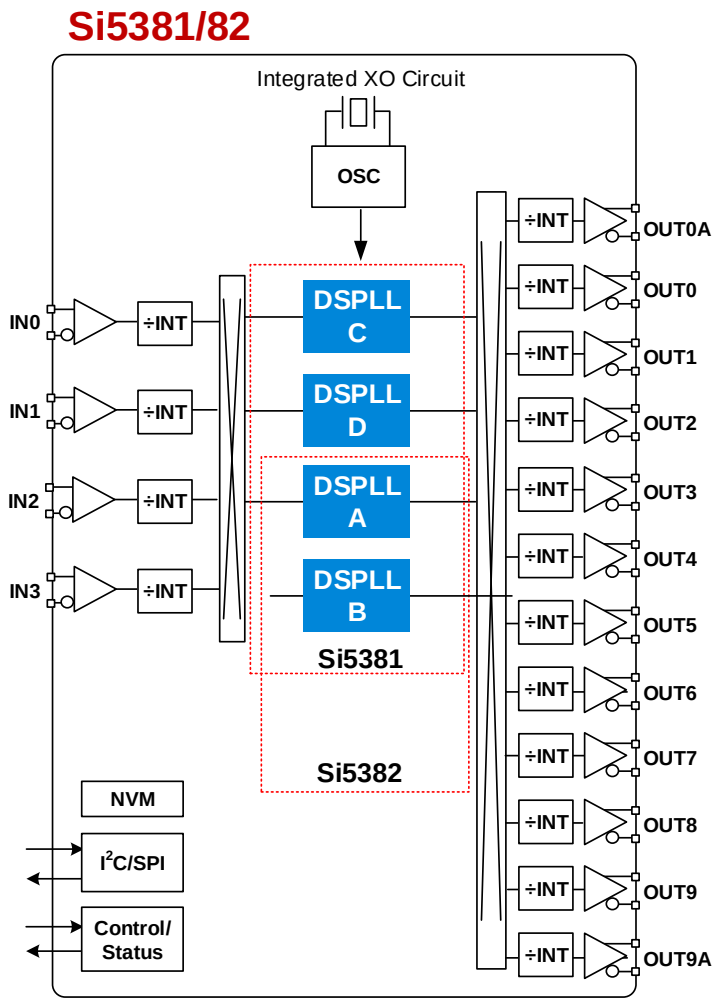




- Base Band Unit
  - DSPLL for 4G/LTE Clocks to ADC/DAC
  - DSPLL for SyncE
  - DSPLL for FPGA clocking

- Small Cells / Distributed Antenna Systems
  - DSPLL for RF transceiver
  - MultiSynth channel generates Ethernet frequencies

Si5381/82 Multi-DSPLL Wireless Clock



Part Number	# PLLs	Clock Inputs/ Outputs	Input Frequency	Output Frequency	Phase Jitter (fs rms)	PLL Bandwidth	Package
Si5381	4	4/12	8 kHz to 750 MHz	100 Hz to 2.94912 GHz	80	10 Hz to 4 kHz	64 QFN 9x9 mm
Si5382	2						

APPLICATIONS

- Mobile backhaul
- LTE-Advanced, 4.5G
- Fixed wireless
- Base band units, micro-BTS

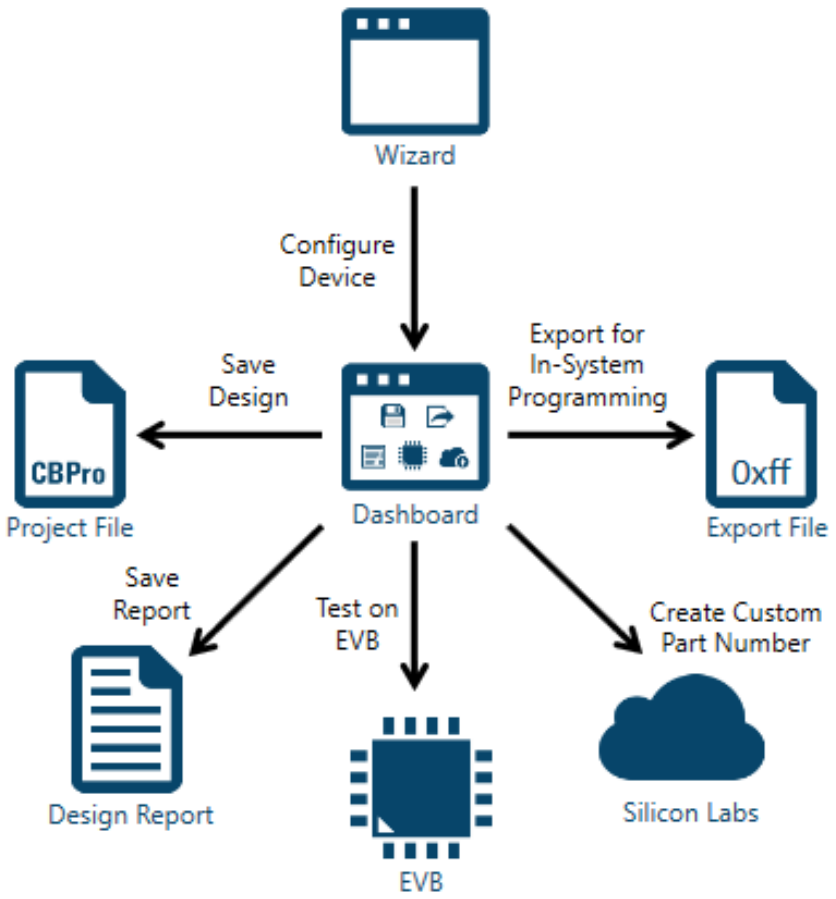
FEATURES

- 2 or 4 independent timing paths
- ANY in to ANY out frequency per DSPLL
- No external VCXO, crystal, loop filters
- Hitless switching, holdover
- Optional zero delay mode
- DSPLL B optimized for wireless
  - Noise floor: -165 dBc/Hz
  - Spur: -103 dBc @ 122.88 MHz
  - 80 fs RMS jitter
- DSPLL A/C/D for reference & data
  - FPGA, CPU, SyncE

Product Comparison Table

Feature	Si5381/Si5382	Si5386
No. Of Clock Inputs/Outputs	4/12 (differential)	4/12 (differential)
No. of DSPLLs	4/2	1
No. of Frequency Domains	Four independent DSPLLs	Five MultiSynths
Integrated VCXO and Loop Filter	Yes	Yes
Integrated Reference	Yes: no external xtals or oscillators	Yes: no external xtals or oscillators
Zero Delay Mode	Yes	Yes
Package	9x9 mm 64-LGA	9X9 mm 64-LGA
Power Consumption	1.4W/1.1W	1.0W

Si538x Development Tools



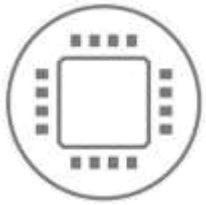
CBPro

Start Here

- Find the right clock and customize it for your application
- Test on an Evaluation Board
- Create custom part number
- Contact Sales or Distributor and place sample order
- Receive pre-programmed samples in 2 weeks

- Click here to download ClockBuilder Pro
- Si538x development kits:
  - Si5381E-E-EVB, Si5382E-E-EVB, Si5386E-E-EVB

Summary: Si538x Simplify Wireless Clock Trees



Best-in-class integration

- Highest level of integration
- Eliminates clocks ICs, VCXO, loop filters, LDOs
- Simplifies PCB layout, power supply filtering

Carrier-grade performance

- Low phase noise
- Excellent spurious performance
- More reliable than VCXO-based PLL

Simple, easy to use

- Simplified PCB layout and design
- Intuitive ClockBuilder Pro software

www.silabs.com/timing