

**Fabrication Notes:**

1. All dimensions in inches. Tolerance = +/- 0.005 unless noted otherwise.
2. All materials: laminates, resins, metallizations and soldermask to be compliant to EU RoHS directive 2002/95/EC IAW SP-12509-01.
3. 370 HR FR-4 or similar grade glass epoxy.
4. Tg > 170 degrees celcius, glass transition temperature.
5. TD > 350 degrees celcius, thermal decomposition.
6. Er = 4.0 +/- 5% @ 2.5GHz.
7. Minimum flammability rating UL94V-0, maximum dissipation factor 0.025.
8. Adjust preprep for 0.062, +/- 0.003 finished thickness measured over soldermask.
9. Copper thickness 0.0014, (.1 oz).
10. Hole size tolerance = +/- 0.003 unless noted otherwise.
11. Hole centers and pad centers to be concentric within 0.002.
12. Drill chart dimensions are drill sizes and not finished hole sizes.
13. Finish - immersion gold over nickel. No exposed bare copper permitted.
14. Thieving not allowed on layer 1.
15. Solder mask over bare copper, LPI class 2 gen. industrial registration +/- 0.004.
16. No coverage on solder pads permitted.
17. Refer to soldermask gerbers for tenting of vias.
18. White silkscreen legend over red soldermask - both sides.
19. Manufacturer icons not permitted on the silkscreen top layer.
20. PCB serialization/panel placement ID on silkscreen bottom.
21. Full electrical test against IPC-356A netlist.

A

A

B

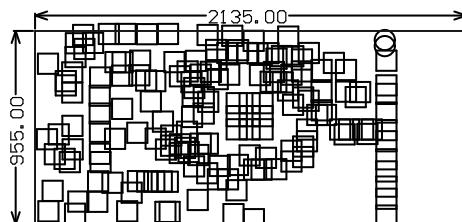
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C

C

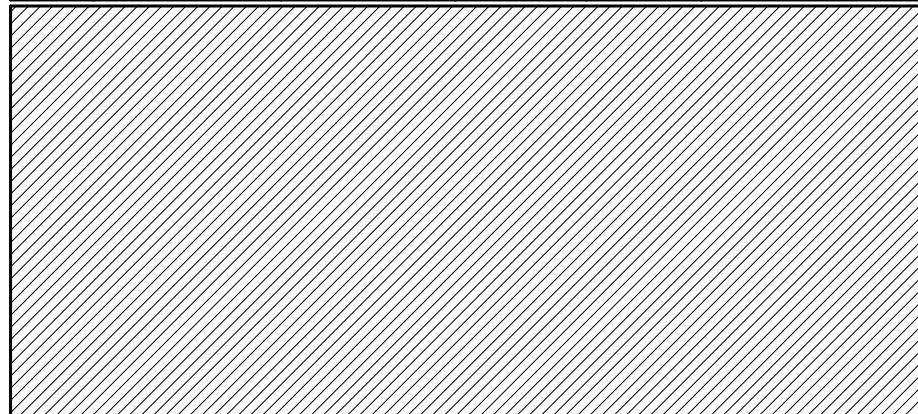
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Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
o	2	12.00mil (.305mm)	PTH	Round
□	166	10.00mil (.254mm)	PTH	Round
	168 Total			

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Paste				
2	Top Overlay				
3	Top Solder	Solder Resist	0.40mil	3.5	
4	Top Layer	Copper	1.40mil		
5	Dielectric1	HR370	16.00mil	3.9	
6	Gnd Layer 2	Copper	1.40mil		
7	Dielectric2	HR370	24.00mil	3.9	
8	Power Layer 3	Copper	1.40mil		
9	Dielectric3	HR370	16.00mil	3.9	
10	Bottom Layer	Copper	1.40mil		
11	Bottom Solder	Solder Resist	0.40mil	3.5	
12	Bottom Overlay				
13	Bottom Paste				

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25 Thomson Place  
2nd Floor  
Boston, MA 02210  
www.silabs.com  
617-951-0200

TITLE:  
Ceramic Balun W/USB 4 Layer Ref.Design

FILE NAME:  
EM358x\_REF\_DES\_CER\_USB\_INU-F.PcbDoc

Board NO.:  
EM358x\_REF\_DES\_CER\_USB\_INU-F

REV:  
A0

Layer:  
Drill Drawing

DATE:  
3/27/2014

A

A

B

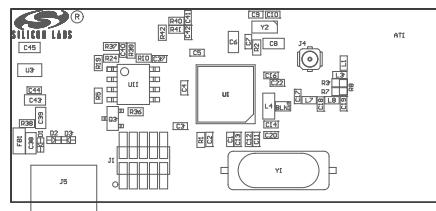
B

C

C

D

D



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**Board NO.:**  
EM358x\_REF\_DES\_CER\_USB\_INU-F

**REV:**  
A0

**Layer:**  
M1 Top Assembly

**DATE:**  
3/27/2014

A

A

B

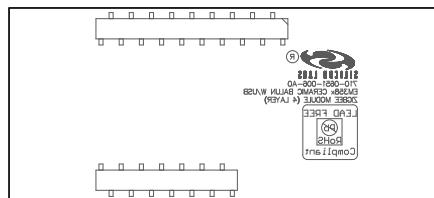
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25 Thomson Place 2nd Floor Boston, MA 02210 <a href="http://www.silabs.com">www.silabs.com</a> 617-951-0200	TITLE: Ceramic Balun W/USB 4 Layer Ref.Design	
	FILE NAME: EM358x_REF_DES_CER_USB_INU-F.PcbDoc	REV: A0
	Board NO.: EM358x_REF_DES_CER_USB_INU-F	DATE: 3/27/2014
	Layer: M2 Bottom Assembly	

A

A

B

B

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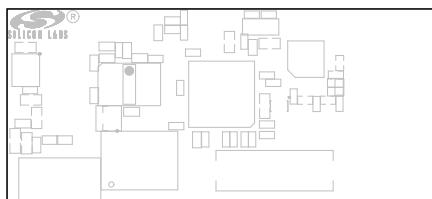
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D

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EM358x\_REF\_DES\_CER\_USB\_INU-F.PcbDoc

**Board NO.:**  
EM358x\_REF\_DES\_CER\_USB\_INU-F

**REV:**  
A0

**Layer:**  
Top Overlay

**DATE:**  
3/27/2014

A

A

B

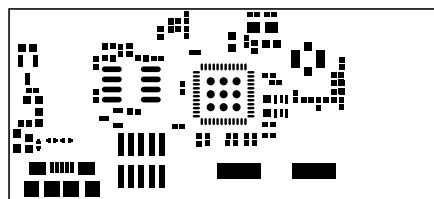
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Board NO.:  
EM358x\_REF\_DES\_CER\_USB\_INU-F

REV:  
A0

Layer:  
Top Paste

DATE:  
3/27/2014

A

A

B

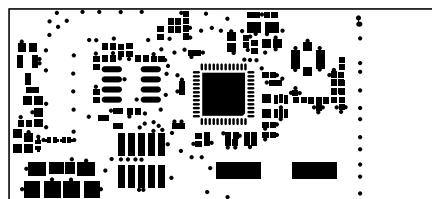
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Board NO.:  
EM358x\_REF\_DES\_CER\_USB\_INU-F

REV:  
A0

Layer:  
Top Solder

DATE:  
3/27/2014

A

A

B

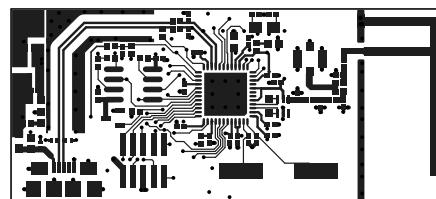
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Board NO.:  
EM358x\_REF\_DES\_CER\_USB\_INU-F

REV:  
A0

Layer:  
Top Layer

DATE:  
3/27/2014

A

A

B

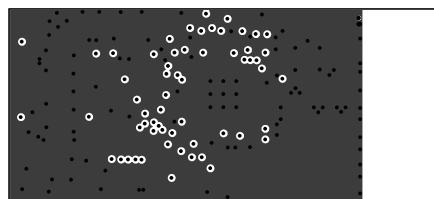
B

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Board NO.:  
EM358x\_REF\_DES\_CER\_USB\_INU-F

REV:  
A0

Layer:  
Gnd Layer 2

DATE:  
3/27/2014

A

A

B

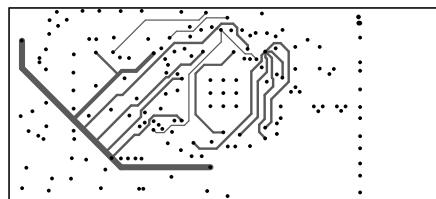
B

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Board NO.:  
EM358x\_REF\_DES\_CER\_USB\_INU-F

REV:  
A0

Layer:  
Power Layer 3

DATE:  
3/27/2014

A

A

B

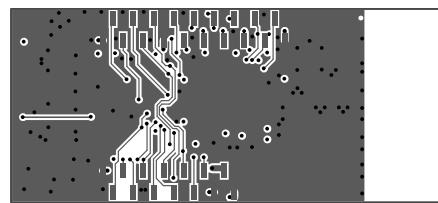
B

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617-951-0200

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EM358x\_REF\_DES\_CER\_USB\_INU-F.PcbDoc

Board NO.:  
EM358x\_REF\_DES\_CER\_USB\_INU-F

REV:  
A0

Layer:  
Bottom Layer

DATE:  
3/27/2014

A

A

B

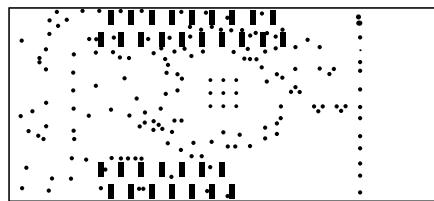
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Board NO.:  
EM358x\_REF\_DES\_CER\_USB\_INU-F

REV:  
A0

Layer:  
Bottom Solder

DATE:  
3/27/2014

A

A

B

B

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EM358x\_REF\_DES\_CER\_USB\_INU-F

REV:  
A0

Layer:  
Bottom Paste

DATE:  
3/27/2014

A

A

B

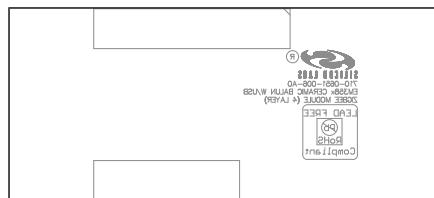
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	Layer:	DATE: 3/27/2014 Bottom Overlay