EM35x Reference Design With SiGe SE2434L Front End Module (FEM)

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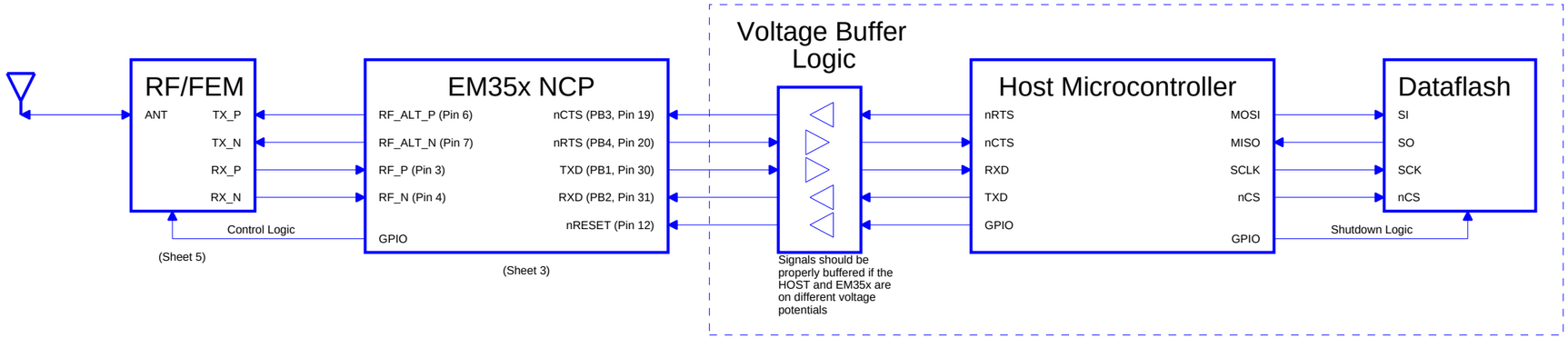
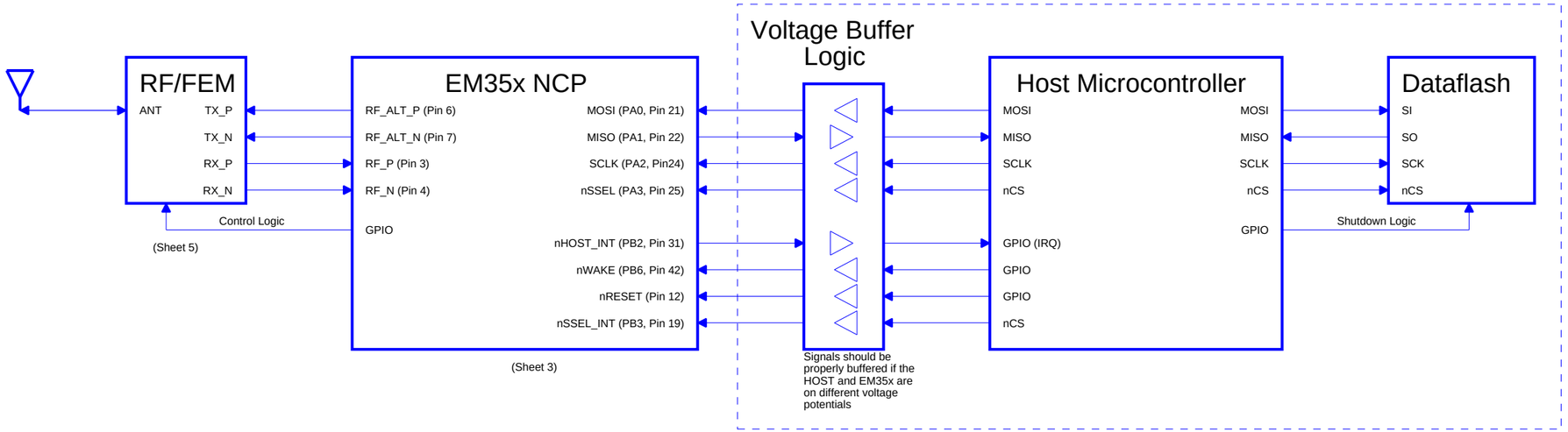
The schematics in this package can be used in both NCP & SOC designs involving the EM35x.
Connect NCP to the host using either UART or SPI serial connection as shown below.

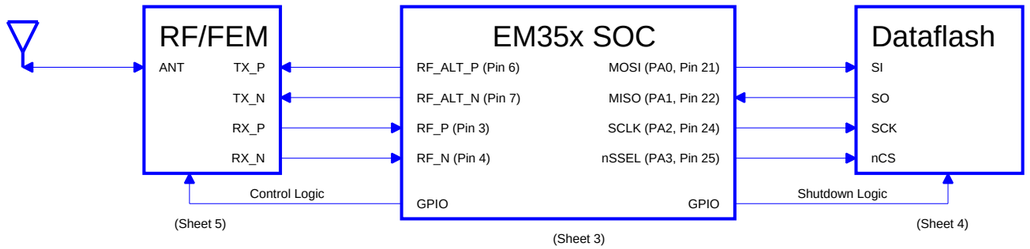
EM35x NCP with EZSP over Asynchronous Serial (UART)



EM35x NCP with EZSP over Synchronous Serial (SPI)



EM35x SOC Reference Design



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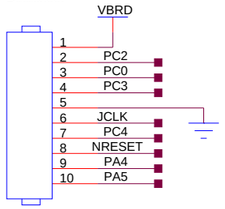
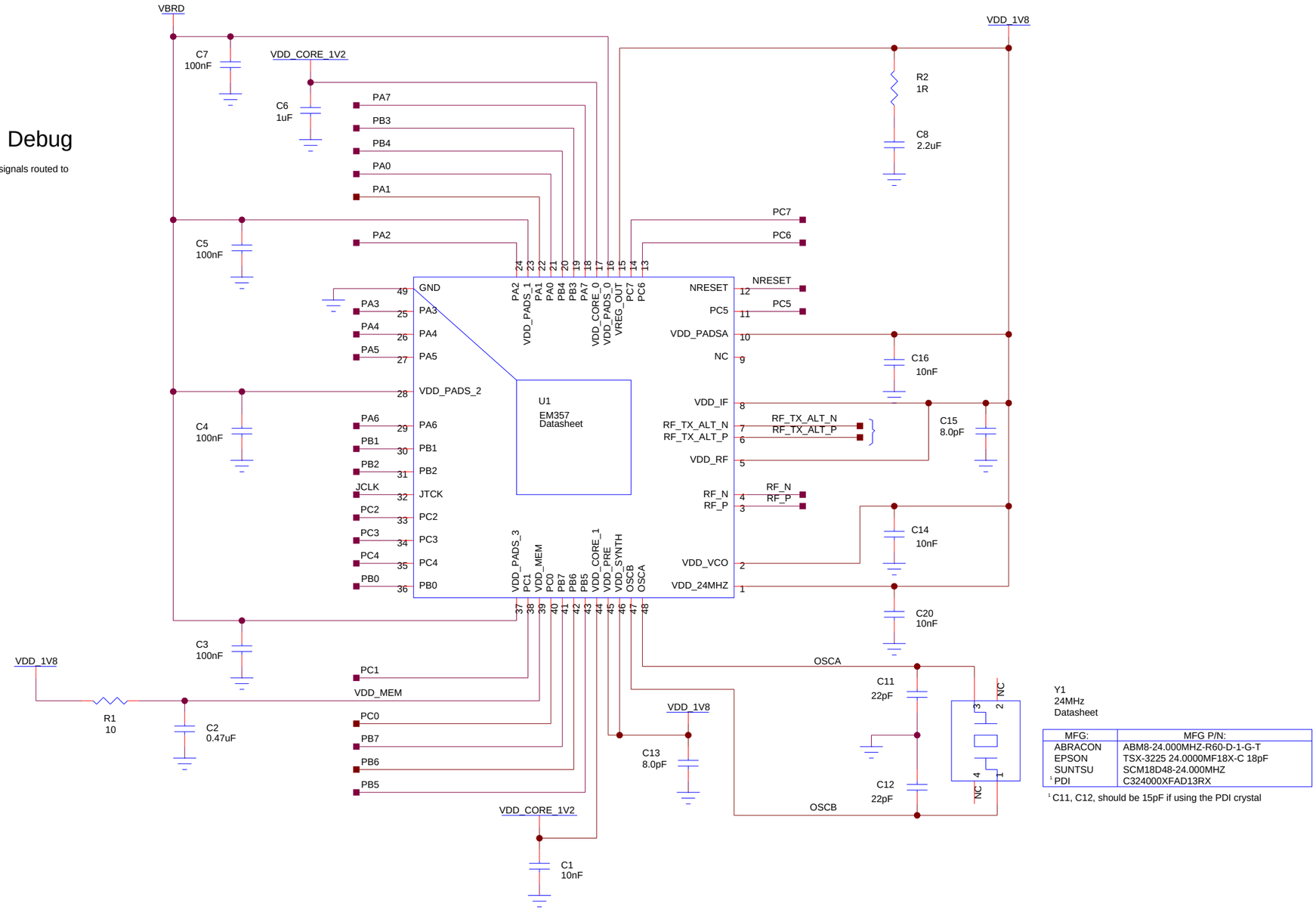
InSight Port for Programming and Debug

In order to make use of all of the features of Ember's Insight desktop tools, all signals routed to J1 need to be accessible by either a connector or test points.

In order to enable direct connection to an insight adapter, ember recommends J1 be a 10 pin dual row 0.05" pitch connector compatiple with Samtec FFSD series ribbon cable, (FFSD-05-D-12.00-01-N). This reference design uses the Samtec, FTSH-105-01-F-DV-K, connector.





MFG:	MFG P/N:
ABRACON	ABM8-24.000MHZ-R60-D-1-G-T
EPSON	TSX-3225 24.0000MF18X-C 18pF
SUNTSU	SCM18D48-24.000MHZ
[1] PDI	C324000XFAD13RX

[1] C11, C12, should be 15pF if using the PDI crystal

PCB3
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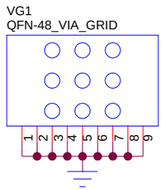
Digital Power

Using R1 isolates the digital switching noise from the analog VDD nets. This isolation improves RX Sensitivity by 2dB when compared with not using the resistor.

EM35x QFN Ground Connection



Layout Note: In order to provde adequate connection to the ground plane as well as thermal continuity during SMT reflow, Ember recommends a via grid of nine vias spaced 1.63mm apart centered under the EM35x QFN-48 package as shown in the EM35X datasheet.

PCB Layout Routing Considerations for the EM35x:

For best RF performance, follow the PCB layout guidelines detailed in the application note 120-5060-000, "PCB Design with an EM35X".
Below are some key items from that document:

* Duplicate exactly the matching network circuit layout connected to the EM35x RF port pins.
* To avoid possible manufacturing soldering issues, adhere to the QFN48 Footprint Recommendations listed in the EM35x datasheet.
* For optimal noise supression on VDD lines, each decoupling capacitor should be placed as close to its VDD pin as posssible.
* To further optimize noise supression, route the VDD source via, then the pad for the decoupling capacitor, then the EM35x VDD pin.
* Do not share ground vias between decoupling capacitors (note exception for crystal circuits).
* The VDDA_1V8 net should be star routed on Layer 3 to take advantage of the inductive filter characteristics of copper routes.
* Keep the 1V8 trace between the EM35x RF supply pins, decoupling capacitors and matching circuit supply pins as short and direct as possible.
* Refrain from placing routes between the thermal ground vias under the EM35x.
* Keep ground plane out of the EM35x top layer circuit.
* Avoid creating ground "islands" in the gound plane on layer 2.
* Make sure the InSight Port test points or connector are easily accessible.
* If using the connector specified, verify pin orientation.
* Be sure to place an easily accessible RF Test Port if using a PCB or on-board antenna.
* In order to reduce crystal loop currents from coupling through the ground plane to layer 1, Ember recommends the crystal shunt capacitors, C11 and C12 share a ground via and are geographically located close to each other.

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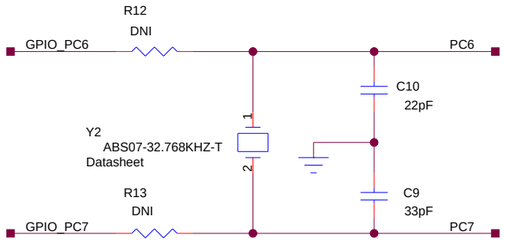
32.768kHz Clock Source (optional)

For increased accuracy of the sleep timer for the EM35x, Ember recommends using a 32.768kHz watch crystal. If accuracy is not required, the internal RC clock source can be used instead, allowing for PC6 and PC7 to be used as GPIO.

The Asymetric loading of the crystal, C9, C10, optimizes the drive level of the oscillator for lowest deep sleep current.



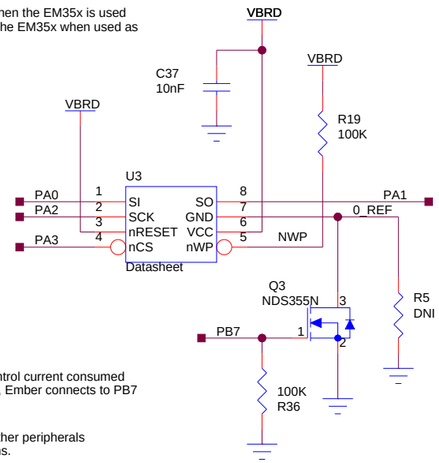
Layout Note: In order to reduce crystal loop currents from coupling through the ground plane to layer 1, Ember recommends the crystal shunt capacitors, C9 and C10 share a ground via and are geographically located close to each other.

DataFlash (Optional)

In order to support the Zigbee Over the Air (OTA) Bootloader profile, Ember supports the following 2MB serial DataFlash;

MFG	MFG P/N	SW Driver
ATMEL	AT45DB021D-SSH-B	at45db021d.c
MICRON	M45PE20-VMN6P	m45pe20.c

DataFlash is connected to the host processor when the EM35x is used as an NCP. DataFlash is directly connected to the EM35x when used as an SOC as shown below.

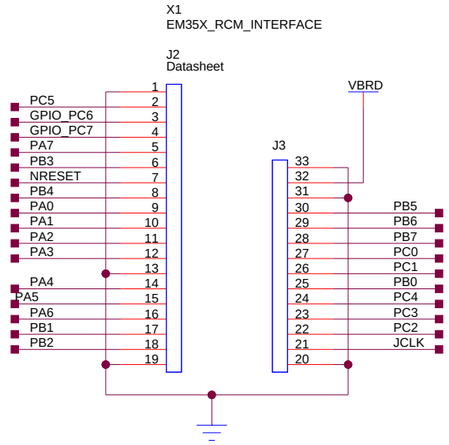


Q3 can be enabled/disabled by any GPIO to control current consumed by the dataFlash when not in use. For example, Ember connects to PB7 for the EM35x SOC reference design.

Shutdown signal for the DataFlash, FEM, and other peripherals can be tied to a single GPIO in some applications.

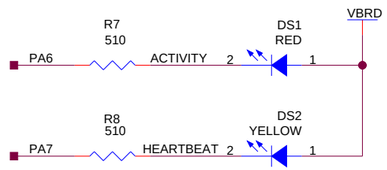
EM35x GPIO Interface Connector (Optional)

The J2 connector is not required for customer designs. This connector is used on Ember's Characterization Radio Control Module and Reference Design. It interfaces to Ember's EM35x Dev Kit Breakout Board.



EmberZnet Stack Indicators (Optional)

The LEDs represent Activity and Heartbeat and are optional, but could be implimented for Debug purposes



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SE2432L FEM

The Front End Module (FEM) from SiGe combines two baluns, PA, RX/TX switch, antenna port harmonic filter and an LNA. FEM is controlled by four EM35x GPIOS. As shown below, Ember uses PB0 for shutdown, (Pin 20), PB5 for LNA control, (Pin 21), PC1 for antenna select, (Pin 16), and PC5 for transmit/receive control, (Pin 24). Please note while any GPIO can be used for shutdown, only PC5 can be used for transmit/receive control.

Mode Selection Guide - EM35x with SE2432L

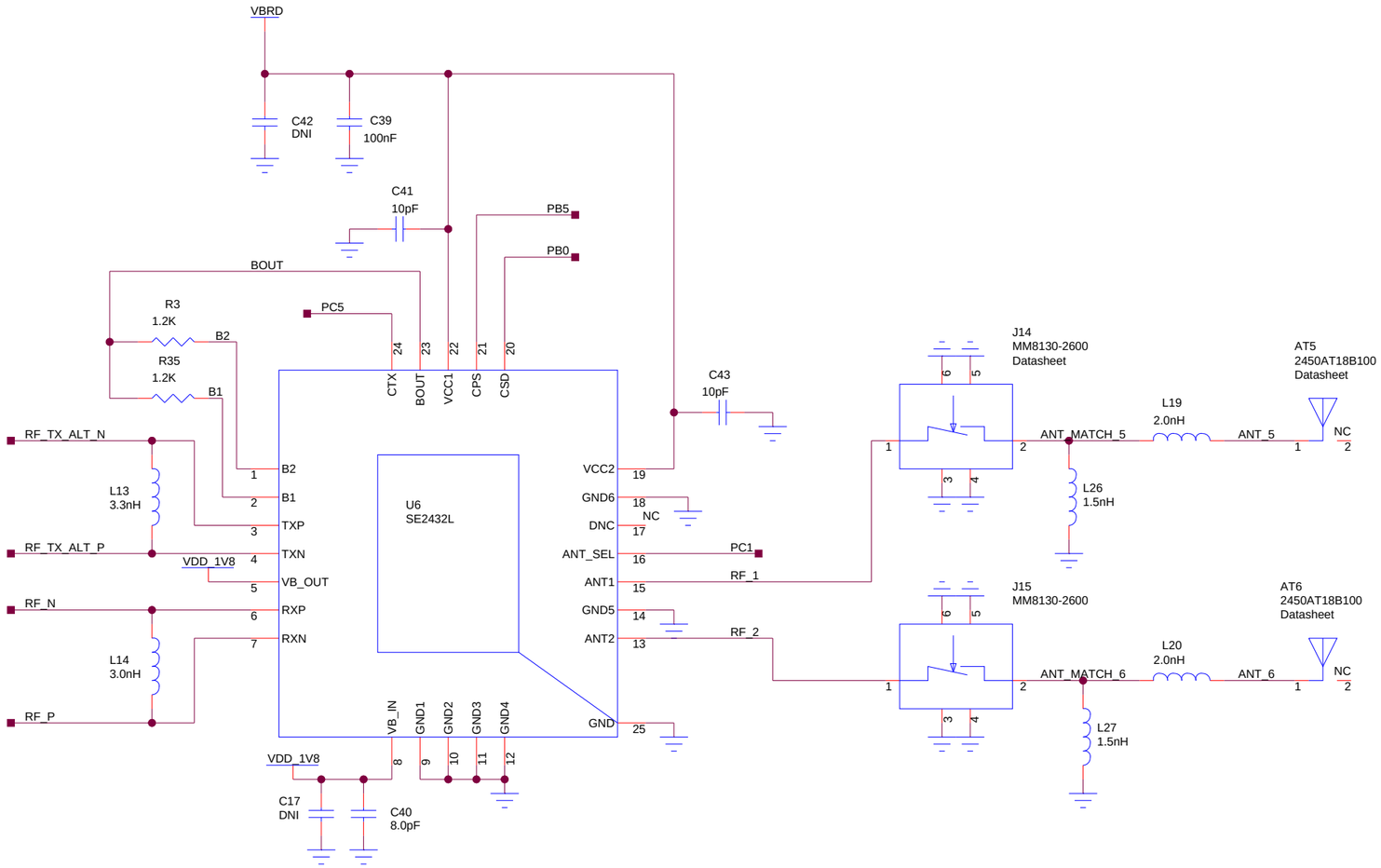
Mode	Mode Description	CSD (Pin 20)	CPS (Pin 21)	CTX (Pin 24)	ANT_SEL (PIN 16)	[2] Current Draw
1	Shutdown	0	0	0	X	<1uA
2	RX Mode w/o LNA	1	0	0	X	32mA
3	RX Mode w/LNA	1	1	0	X	38mA
4	TX Mode (20dBm)	1	1	1	X	150mA

[2] Includes EM35x

ANT_SEL (PIN 16)	Output Selected
0	ANT1
1	ANT2

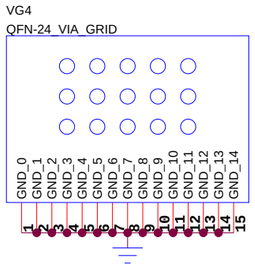
Notes:

* The pin names / numbers in the table are all defined by SiGe.
* The "DON'T CARE" states are allowed to be driven by the SW without effect on the operation of the FEM.
* The CSD, CPS, and ANT_SEL pins can be driven by any EM35x GPIO pin or by other peripheral logic control circuitry.
* EM35x Nodetest application software automatically controls the CSD pin through PB0.
* EM35x Nodetest application software automatically controls the CTX pin through PC5.
* EM35x Nodetest application software defaults to the ANT1 antenna port.
* EM35x Nodetest application software automatically controls the CPS pin through PB5.
* The CPS pin can be pulled to VBRD with a pull-up in applications which do not require shutdown.
* ANT_SEL can retain its state during Shutdown.
* For single antenna applications, use ANT1 and tie U6 pin 16 to GND through a pull-down resistor.
* Inductors, L13 and L14, are required between the FEM and the EM35X to tune the FEM baluns.
* Component values for L13 and L14 are PCB layout dependant and may need to be tuned on customer applications.
* All harmonic filtering is integrated in the FEM, therefore external filtering is not required.
* To facilatate test and measurement, an RF adapter cable for J14 and J15 is available from Murata, part number MXHS83QE3000.



SE2432L QFN Ground Connection

A 3 x 9 array of vias, shown as VG4, provides grounding and thermal continuity when placed centered under the SE2432L.



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SCHEMATIC NOTES:

-- Version A0.0 --
*Released: April 09, 2010
*Initial version released, Version A0

-- Version A1.0 --
*Released: September 16, 2010
*Changed Data Flash Shutdown Pin to PB7
*Changed SE2432L CPS (PIN21) control to PB5 for deep sleep
*Added antenna, RF test point and antenna matching circuit
*Changed L13 from TBD to 3.3nH
*Changed L14 from TBD to 3.0nH
*Changed C51, TBD, to L26, 1.5nH
*Changed C50, TBD, to L27, 1.5nH

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