

## Timing Solutions for Broadcom Switches/PHYs

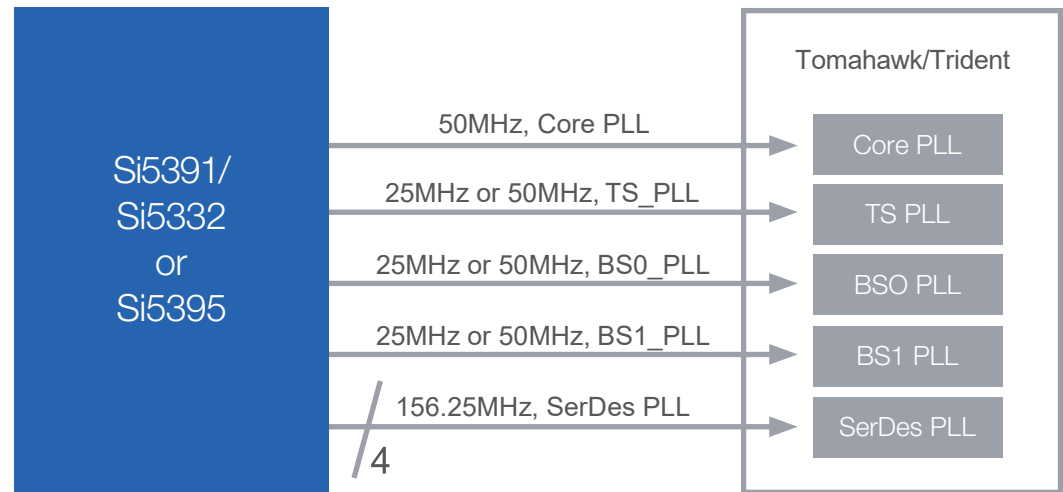
### Timing Simplified

Silicon Labs offers a broad portfolio of frequency flexible timing products that enable hardware designers to simplify clock generation, distribution, and jitter attenuation. The portfolio includes:

- Network synchronizers
- Jitter attenuating clocks
- Clock generators
- Clock buffers
- PCIe clocks and buffers
- Oscillators (XO/VCXO)

Silicon Labs clocks use proprietary DSPLL and MultiSynth technologies to generate any combination of frequencies with ultra-low jitter, enabling best-in-class clock tree integration. Clock buffers provide low-jitter, low-skew clock distribution with integrated format/voltage level translation. PCIe clocks/buffers combine Gen 1/2/3/4/5 compliance with on-chip series termination, simplifying design. XO/VCXOs are factory-customizable to any frequency, with samples available in one to two weeks.

### Timing Solutions for Tomahawk/Trident Switches



For more information related to reference designs or partner pricing, please contact your local Silicon Labs sales representative.



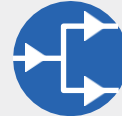
#### Oscillators

- Any frequency up to 3.0 GHz
- Ultra-low jitter: 80 fs RMS
- Short lead times: 1-2 weeks (samples)



#### Clock Generators

- Any-frequency, any-output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks and XOs
- PCI Express Gen 1/2/3/4/5 compliant



#### Clock Buffers

- Integrated format/level translation
- Ultra-low additive jitter: 50 fs RMS
- PCI Express Gen 1/2/3/4/5 compliant



#### Jitter Attenuating Clocks/Network Sync

- Any frequency, any output
- Ultra-low jitter: 69 fs RMS
- Clock tree on a chip replaces clocks, XOs, VCXOs

# Timing Solutions for Broadcom



Application		Broadcom Product Family	Silicon Labs XO	Silicon Labs Clock Buffer	Silicon Labs Clock
Broadband	DSL/G.fast/Cable Central Office	BCM33xx BCM65xxx	Si51x Si53x/Si54x/Si57x	Si5330x	Si5332 Si5341
	xPON OLT	BCM68xxx BCM55xxx	Si51x Si53x/Si54x/Si57x	Si5330x	Si5332 Si5341
Enterprise + Network Processors	StrataGX Communications Processors	BCM58xxx XLPxxx	Si51x	Si5330x	Si5332
	Knowledge-Based Processors	NLxxx NLAxxx	Si51x	Si5330x	Si5332
Wireless Infrastructure	Small Cells	BCM616xx	Si51x	Si5330x	Si538x
	DFE Processors	BCM510xx	Si51x	Si5330x	Si538x
	Microwave / Mobile Backhaul	BCM85xxx	Si51x Si53x/Si54x/Si57x	Si5330x	Si534x Si538x
Ethernet Communication + Switching	10G/25G/50G StrataConnect Switch	BCM53570	Si54x	Si5330x	Si5332 Si5341
	10/40/100G Retimer/Gearbox	BCM82xxx	Si53x/Si54x	Si5330x	Si534x
	10/100GbE PHY/retimer	BCM82xxx BCM81xxx	Si53x/Si54x	Si5330x	Si534x
	200/400 GbE PHY/Retimer	BCM81xxx	Si54x	Si5330x	Si539x
	10/40/100GbE Trident/Tomahawk Switch	BCM56860 BCM56870/970	Si54x	Si5330x	Si5332
	200/400GbE Tomahawk Switch	BCM56980	Si54x	Si5330x	Si539x
Storage Adapters and Controllers	SAS/SATA/NVMe Host Bus Adapters	HBA 9xxx	Si51x	Si5315x/ Si5330x	Si5332
	Fibre Channel Host Bus Adapters	LPe3200x	Si51x	Si5315x/ Si5330x	Si5332
	SAS/SATA Storage Controllers	SAS2xxx SAS3xxx	Si51x	Si5315x/ Si5330x	Si5332
	Fibre Channel Storage Controllers	XE2xx XE5xx	Si51x	Si5315x/ Si5330x	Si5332

# Broadcom Switch/PHY Jitter Requirements



Timing solutions from Silicon Labs meet Broadcom reference clock jitter requirements with significant margin.

Broadcom Family	Chipset	Frequency	Silicon Labs Device	BRCM Jitter Requirement	Silicon Labs RMS Jitter
Strata XGS	Trident2	4x 156.25MHz	Si5332 Clock Generator or Si5345 JA Clock	0.3ps	217fs RMS
		25 or 50MHz		2ps	209fs RMS
	Trident3	4x 156.25MHz		0.3ps	217fs RMS
		25 or 50MHz		2ps	209fs RMS
	Tomahawk1	4x 156.25MHz		0.3ps	217fs RMS
		25 or 50MHz		2ps	209fs RMS
	Tomahawk2	4x 156.25MHz	Si5341 Clock Generator or Si5345 JA Clock	0.15ps	83fs RMS
		25 or 50MHz	2ps	170fs RMS	
	Tomahawk3	8 x 312.5MHz	Si5391P Clock Generator or Si5395P JA Clock	0.15ps	68fs RMS
		100MHz		0.2ps	120fs RMS
		25 or 50MHz		0.2ps	120fs RMS

For more information, visit [silabs.com/timing](https://silabs.com/timing)

Request a custom clock or XO/VCXO at [silabs.com/custom-timing](https://silabs.com/custom-timing)