# Instruction

## Mandatory crystal adjustment for EFR32ZG14 based products

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<thead>
<tr>
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<th>INS14498</th>
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<tbody>
<tr>
<td>Version:</td>
<td>7</td>
</tr>
<tr>
<td>Description:</td>
<td>This document describes the mandatory adjustment of the system crystal which must be performed on a product based on the EFR32ZG14 Gateway device</td>
</tr>
<tr>
<td>Written By:</td>
<td>OPP;JFR;SCBROWNI</td>
</tr>
<tr>
<td>Date:</td>
<td>2020-06-17</td>
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<tr>
<td>Reviewed By:</td>
<td>LTHOMSEN;NTJ;PSH;SCBROWNI</td>
</tr>
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## REVISION RECORD

<table>
<thead>
<tr>
<th>Doc. Rev</th>
<th>Date</th>
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<th>Pages Affected</th>
<th>Brief Description of Changes</th>
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<tbody>
<tr>
<td>1</td>
<td>20181204</td>
<td>OPP</td>
<td>ALL</td>
<td>Initial version, added how to populate the CTune value as a manufacturing token</td>
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<tr>
<td>2</td>
<td>20181205</td>
<td>OPP</td>
<td>2, 5, 7</td>
<td>Type errors fixed, more correct sentences.</td>
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<td>2</td>
<td>20190116</td>
<td>MALEDESM</td>
<td>ALL</td>
<td>Grammar and structure (consistent format) modification</td>
</tr>
<tr>
<td>3</td>
<td>20190312</td>
<td>OPP</td>
<td>Section 3, Figure 1, Section 4 Table 4.1</td>
<td>Emphasized that only a 39MHz crystal is supported. Corrected crystal type number. Updated drawing, showing internal cap in EFR32ZG14. Rephrased wording at the start of the section. Added a table-structure for CTune measurement method</td>
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<tr>
<td>4</td>
<td>20190819</td>
<td>OPP</td>
<td>Section 6</td>
<td>Added second source description</td>
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<tr>
<td>5</td>
<td>20190911</td>
<td>SCBROWN</td>
<td>Section 3, 4 &amp; 6</td>
<td>Reviewed Sections</td>
</tr>
<tr>
<td>6</td>
<td>20200608</td>
<td>OPP</td>
<td>All</td>
<td>Removed description of batch calibration since this has proven not to be correct. Each individual product item must be calibrated.</td>
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<tr>
<td>7</td>
<td>20200611</td>
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1 Abbreviations

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<th>Explanation</th>
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<tr>
<td>ASIC</td>
<td>Application Specific Integrated Circuit</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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<tr>
<td>ppm</td>
<td>Parts Per Million</td>
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2 Introduction

2.1 Purpose

The purpose of this document is to describe the required method to match the system crystal of an EFR32ZG14-based product to the parasitic of that product. The procedure is required to ensure that the crystal tolerances of the product are within the specifications of the Z-Wave protocol.

2.2 Audience and Prerequisites

The intended readers of this document are:

- Product design engineers
- Production test engineers
- Z-Wave application programmers

The readers of this document are assumed to have knowledge of:

- The Z-Wave protocol
- Basic RF knowledge
- Basic RF measurement skills

Access to the bring-up software tool RailTest is required.

Knowledge and access to the following documents are essential:

- [1] “INS14283 Instruction for Bring-up/test HW development”
3 About Crystal Tolerances

The precision of the system crystal in a radio system, such as the Z-Wave radio system, is vital. If the transmitters and receivers in the Radio system are not operating with the correct clock frequency, and if the frequency difference between the parts is large, it will affect the obtainable range between the parts. This leads to customers experiencing a bad performance of the radio system. It is therefore mandatory to make sure that the system frequency of a radio product is as accurate as possible and adheres to the specifications of the radio protocol used, in this case, the Z-Wave protocol.

The total tolerance of a crystal is a sum of three contributions:

1. Initial tolerances
2. Temperature tolerances
3. Aging tolerances

For the Z-Wave protocol, the required tolerances for the crystal after five years of operation is +/-27 ppm.

To avoid frequency harmonics in any Z-Wave frequency band, only a 39MHz crystal is supported. The recommended crystal to use for EFR32ZG14 products is a 39MHz crystal from TXC, type 8Y39072002. For the specified crystal, the total tolerances are +/-24 ppm across the temperature range -40°C – 90°C after five years of service, and the individual contributions are:

Initial tolerances: +/-8 ppm
Temperature tolerances: +/-13 ppm from -40°C to 90°C
Aging tolerances: +/-3 ppm after 5 years

The Initial tolerances are affected by:

- Parasitic load capacitance at the crystal component connections
- Parasitic load of the Z-Wave ASIC
- Pressure exerted on the component package

The Temperature tolerances are affected by:

- The temperature of the environment

The Aging tolerances are affected by:

- Overdrive of the crystal
- Overheat of the component
- Mechanical stress due to normal usage

If it is assumed that the crystal is not stressed in any way, not mechanically nor electrically, there are two parameters left, which can give a tolerance change for the crystal, i.e., change the frequency of the crystal. These parameters are: the parasitic load capacitance added by the PCB of the product and the differences of the load capacitance of the crystal oscillators for the individual Z-Wave ASIC’s.
Depending on the implementation of the crystal oscillator circuit of an ASIC, external load-caps may be required. However, this is not the case for the EFR32ZG14 device, where the load-caps are integrated on the die of the EFR32ZG14, as illustrated in Figure 1:

![Figure 1. External vs. Internal Load Capacitance](image)

The amount of parasitic capacitance seen by the crystal depends on:

- Trace length
- PCB material properties
- Differences in the internal size of the ASIC load caps

These parameters vary from product-design to product-design and from Z-Wave ASIC to Z-Wave ASIC.

To counteract the parasitic load capacitance of the PCB, device implementation, and Z-Wave ASICs, the Z-Wave protocol offers the possibility to adjust the internal load capacitances in such a way that the total capacitance seen by the crystal fulfills the crystal specifications.
4 How to Adjust the System Crystal

As described in Section 3, implementing the 39MHz system crystal on a PCB and connect it to the Z-Wave ASIC will affect the crystal frequency. This is due to the parasitic load capacitance added to the crystal terminals by the traces from the EFR32ZG14 device to the crystal component and due to the variance in the internal load capacitance of the Z-Wave ASICs.

To counteract the added parasitic load capacitance, the Z-Wave protocol offers the possibility to change the value of the internal load capacitance in such a way that the sum of the internal load capacitance and the parasitic load capacitance is equal to the nominal load capacitance of the crystal. When the crystal operates with the nominal load capacitance, the frequency of the crystal will also be the nominal frequency:

![Distribution of initial tolerance error](image1)

![Example of distribution of initial tolerance error](image2)

Figure 2. Offset Error Due to Parasitic Load Capacitance

Figure 2 shows how the distribution of the initial frequency errors will be for two various products: one ideal product (not realistic to realize) with no parasitic capacitances at all and one product with a parasitic capacitance from both the PCB and the Z-Wave ASIC.
The frequency error of an RF-enabled product can be measured by measuring the RF frequency of a Carrier Wave (CW) transmitted by the product. If the product is designed for the EU region, and a CW is enabled for, as an example, channel 2, then any measured average frequency offset from 868420000 Hz is an RF frequency error that must be corrected.

Refer to [1] to see how a CW is set up in connection with the usage of the test software RailTest.

Since the parasitic capacitances seen by the crystal consists of two parts: A “stationary part” origin from the PCB traces and a “variable part” origin from the variation of the internal load capacitances of the Z-Wave ASIC, each individual product of the product range must be calibrated during the production flow.

The frequency of a product is changed by adjusting a value called the CTune value. The determination of the CTune value for each part is an iterative process and can be described as shown below:

<p>| | |</p>
<table>
<thead>
<tr>
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<tbody>
<tr>
<td>1</td>
<td>Program RailTest to the item to calibrate. Refer to [1] for more information.</td>
</tr>
<tr>
<td>2</td>
<td>For each item, follow the procedure described in [1] and measure and adjust the CW frequency.</td>
</tr>
<tr>
<td>3</td>
<td>Using the method described in [1], adjust the CTune value for this item until $f_{measured} = f_{target}$.</td>
</tr>
<tr>
<td>4</td>
<td>Program the found CTune value for the item into the flash memory of the Z-Wave ASIC [2] and [3]</td>
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</table>

The found CTune value is incorporated into the Z-Wave protocol by setting the token TOKEN_MFG_CTUNE equal to the CTune value found. For handling of manufacturing tokens, refer to [2].

Once adjusted, the average frequency error should be within +/-1 ppm for each product item at 25°C.

The CTune found is valid for the specific product item. If the firmware is updated, the new firmware must use the initially found CTune value. In other words, the CTune value must follow the product item during its entire life.
5 Effect of the Production Calibration the System Crystal

Section 4 describes how to remove the frequency offset of a product. This will ensure that the system frequency error is reduced to +/-1 ppm.

When each product is production calibrated, the net result will be as shown below:

As seen from Figure 3, the initial crystal tolerance is at +/-8 ppm, and the offset due to layout parasitic and Z-Wave ASIC variance is reduced to e.g., +/-1 ppm since each product is individually measured and calibrated.
To sum up: to individually calibrate each product item, one must:

1. Be able to download RailTest during the manufacturing of the product
2. Be able to control RailTest during the manufacturing of the product
3. Be able to precisely measure a CW from the product with a precision of +/- 1 ppm
   a. With the aid of a spectrum analyzer or an RF frequency counter
4. Be able to derive a CTune value from the frequency measured
5. Be able to incorporate the CTune value found into the Z-Wave protocol code to download

As seen in the procedure description above, the CTune value found must be incorporated into the Z-Wave protocol. This is done in the form of a TOKEN_MFG_CTUNE value, with value = CTune, which is programmed into memory according to the description given in [2].
6 Second Source Crystal Component

In case a second source component for the TXC, type 8Y39072002, is needed, the following component is suggested:

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Supplier</th>
</tr>
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<tbody>
<tr>
<td>XTL501140-S315-020</td>
<td>Siward</td>
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</table>

Other crystal vendors that meet these requirements can be used:

Crystal minimum requirements:

- Fundamental mode crystal
- +/- 25ppm after five years across a temperature range of the product
- Load capacitance 10pF (range: 8pF – 12pF)
- ESR: Max 50Ω
- $C_0$: 2pF – 7pF ($C_0$ for the first source and second source components: 2pF and 3pF)

**NOTE:** The “CTune” value must be measured and applied to each unit manufactured.

**NOTE:** Selecting a crystal is an important step in the design of an end-product. Once an end-product has obtained RF regulatory certifications, the RF regulatory authorities do not allow the change of the crystal without re-certification.
7 References

[1] INS14283, Instruction for Bring-up/test HW development.
[3] INS14285, Manufacture Z-Wave 700 product in volume