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PG23 Pro Kit	
Board Function	Page
Title Page	1
User Interface	2
Signal Assignments	3
EFM32 Power	4
EFM32 I/O	5
Segment LCD	6
Target Voltage Supply	7
AEM & Voltage Sense	8
Debug Interface	9
Simplicity & VCOM	10
Power	11
Board Controller	12
Board Controller Misc	13

Revision History	
Rev.	Description
A00	Initial version.
A01	Bump U1 revision.
A02	Not mount clamping diodes for ADC input.
A03	Remove AEM bypass, clamping diodes.
A04	Updated U1 OPN.

 <b>SILICON LABS</b>		Board Name <b>EFM32PG23 Pro Kit</b>	
		Page Title <b>Title Page</b>	
Designed <b>MAH</b>	Approved <b>RGU</b>	Board Number <b>BRD2504A</b>	Revision <b>A04</b>
Size <b>A3</b>	Sheet Modified Date <b>Friday, April 29, 2022</b>	Copyright Silicon Laboratories Inc. 2021    CONFIDENTIAL – SUBJECT TO TERMS OF USE	
		Sheet <b>1 of 13</b>	

5



## 3



1

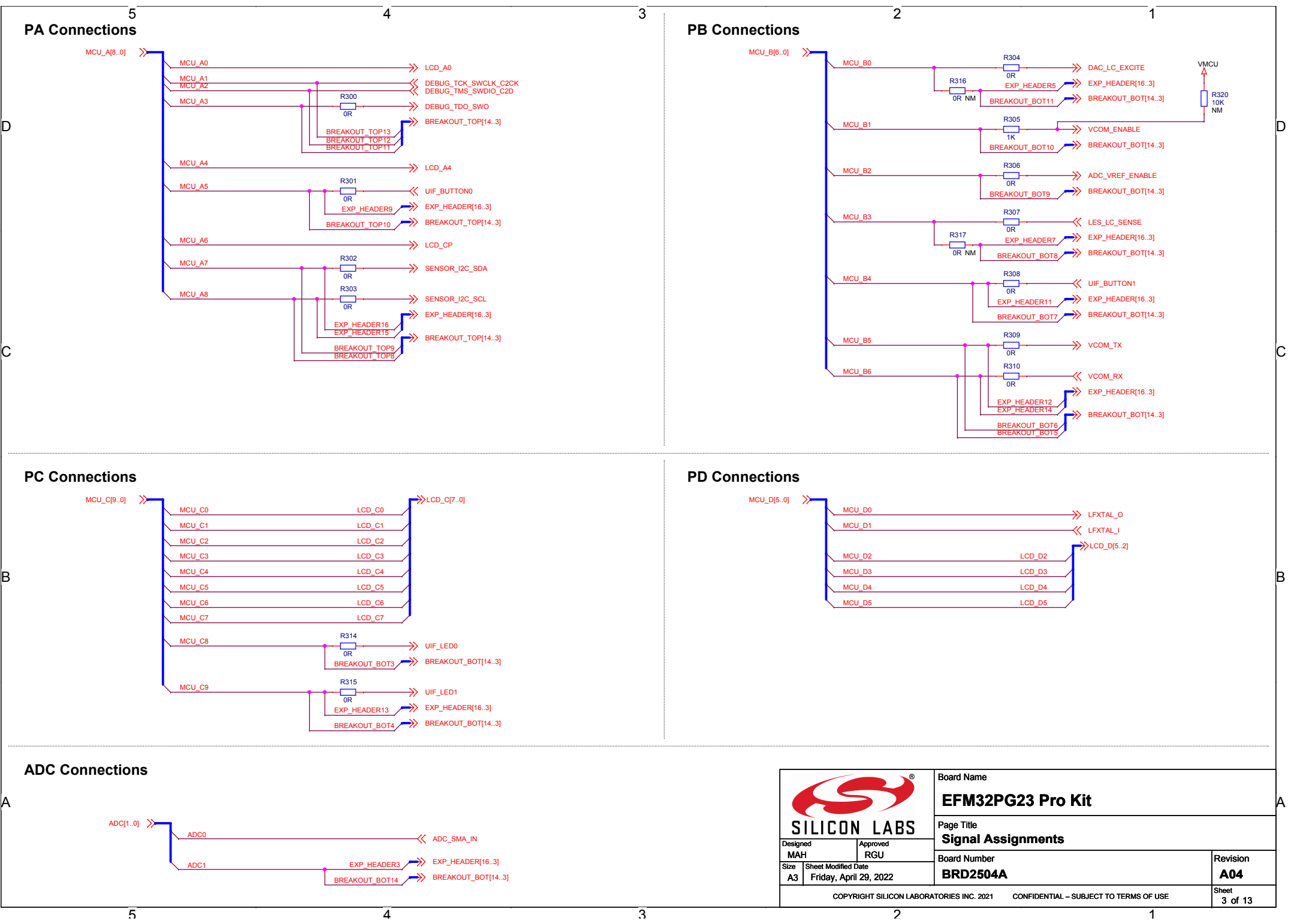



## C



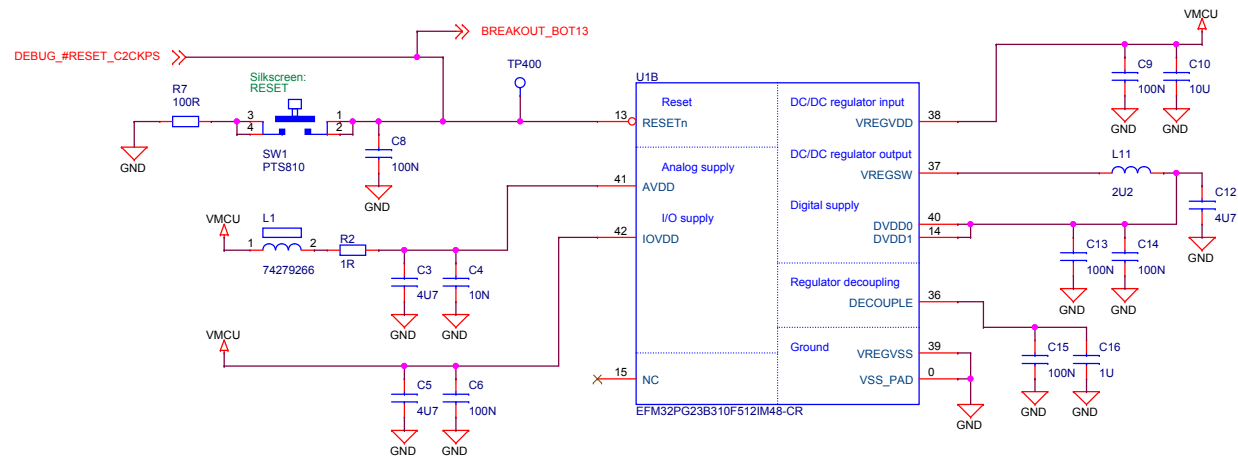
## B





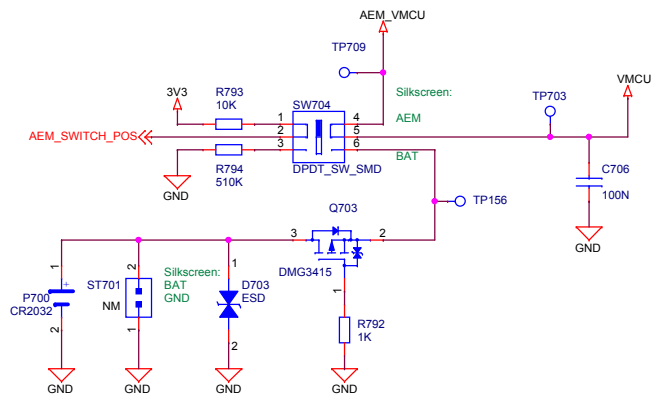
 <b>SILICON LABS</b>		Board Name <b>EFM32PG23 Pro Kit</b>	
		Page Title <b>Signal Assignments</b>	
Designed MAH	Approved RGU	Board Number <b>BRD2504A</b>	Revision <b>A04</b>
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		Sheet 3 of 13	

## EFM32 Power and Decoupling

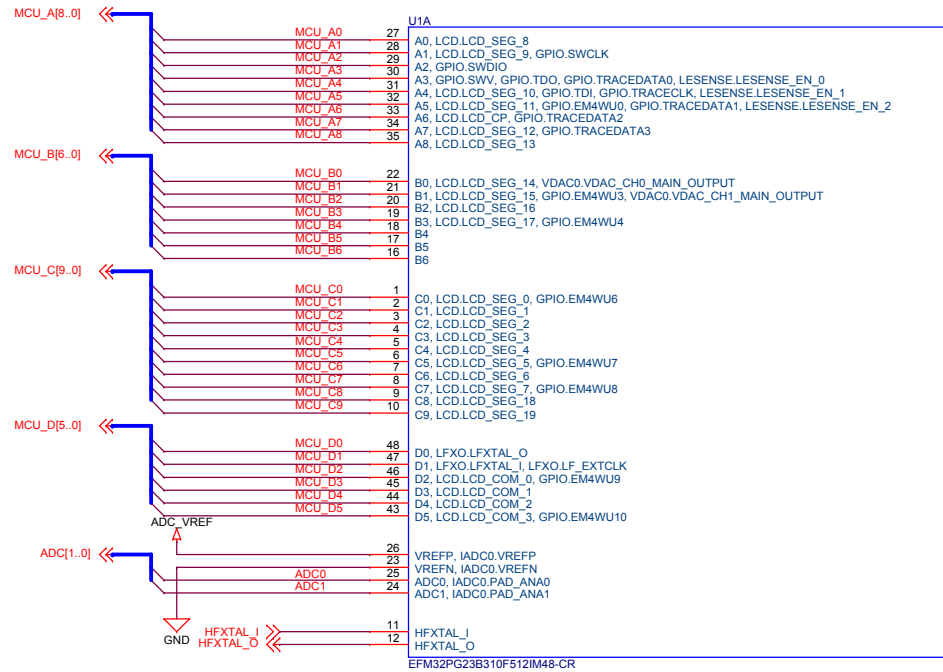


## Power Select Switch: AEM/BAT

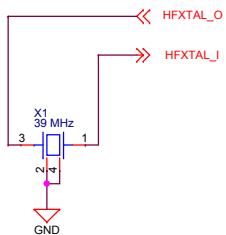
SWITCH POS	MODE DESCRIPTION
AEM	AEM Enabled, VMCU sourced from external 3.3V LDO powered by BC USB 5V supply
BAT	AEM Disabled, VMCU sourced from coin-cell battery or external power supply



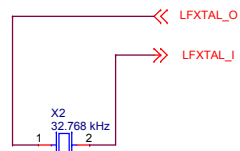
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		Page Title <b>EFM32 Power</b>	
Designed MAH	Approved RGU	Board Number <b>BRD2504A</b>	Revision <b>A04</b>
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		Sheet 4 of 13	



## High Frequency Clock

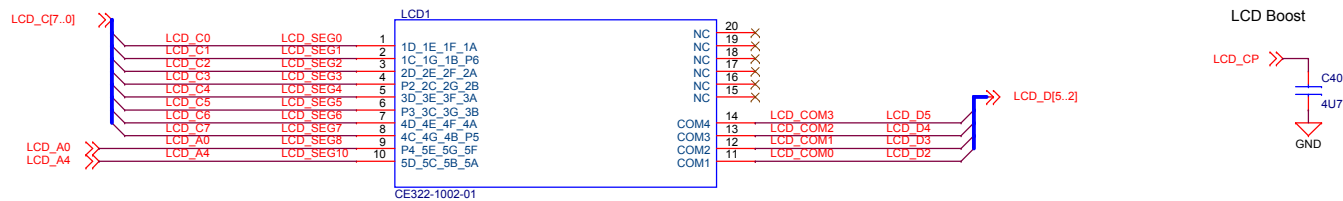


## Low Frequency Clock



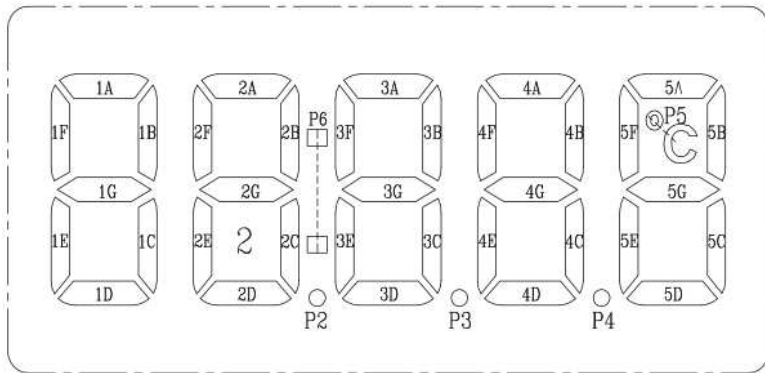
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		EFM32PG23 Pro Kit	
Designed		Page Title	
MAH		EFM32 I/O	
Size		Board Number	
A3		BRD2504A	
Sheet Modified Date		Revision	
Friday, April 29, 2022		A04	
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## Segment LCD Signal Connections



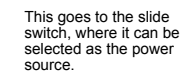
## Segment Names

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
COM1	1D	1C	2D	P2	3D	P3	4D	4C	P4	5D	COM1	--	--	--	--	--	--	--	--	--
COM2	1E	1G	2E	2C	3E	3C	4E	4G	5E	5C	--	COM2	--	--	--	--	--	--	--	--
COM3	1F	1B	2F	2G	3F	3G	4F	4B	5G	5B	--	--	COM3	--	--	--	--	--	--	--
COM4	1A	P6	2A	2B	3A	3B	4A	P5	5F	5A	--	--	--	COM4	--	--	--	--	--	--

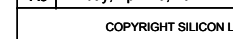


 <b>SILICON LABS</b>		Board Name	
		<b>EFM32PG23 Pro Kit</b>	
Designed MAH		Approved RGU	
Page Title		<b>Segment LCD</b>	
Size A3		Board Number	
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		Revision <b>A04</b>	
		Sheet 6 of 13	

## A



CALIBRATE	Calibration Current
0x1	3.30 uA
0x2	132.5 uA
0x4	323.5 uA
0x6	456.1 uA
0x8	12.36 mA

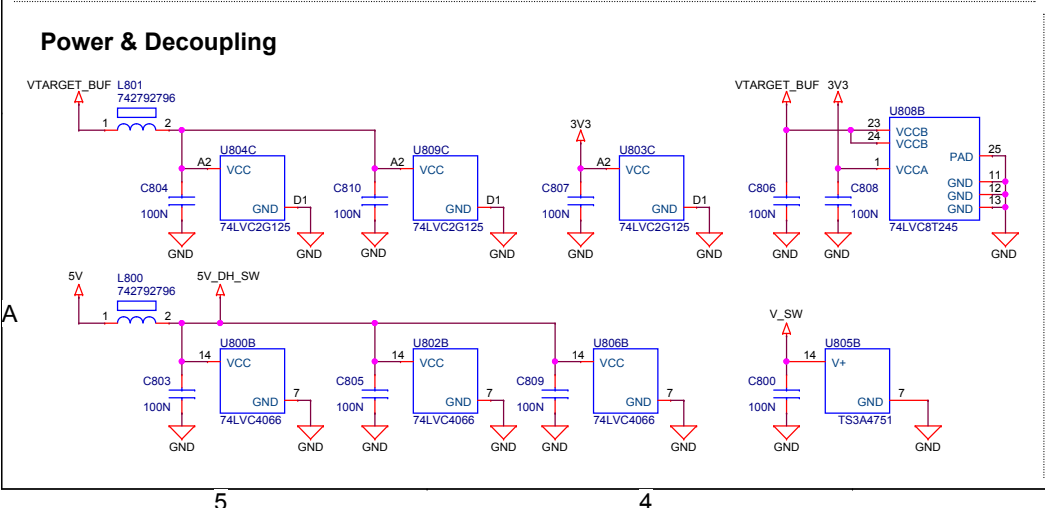
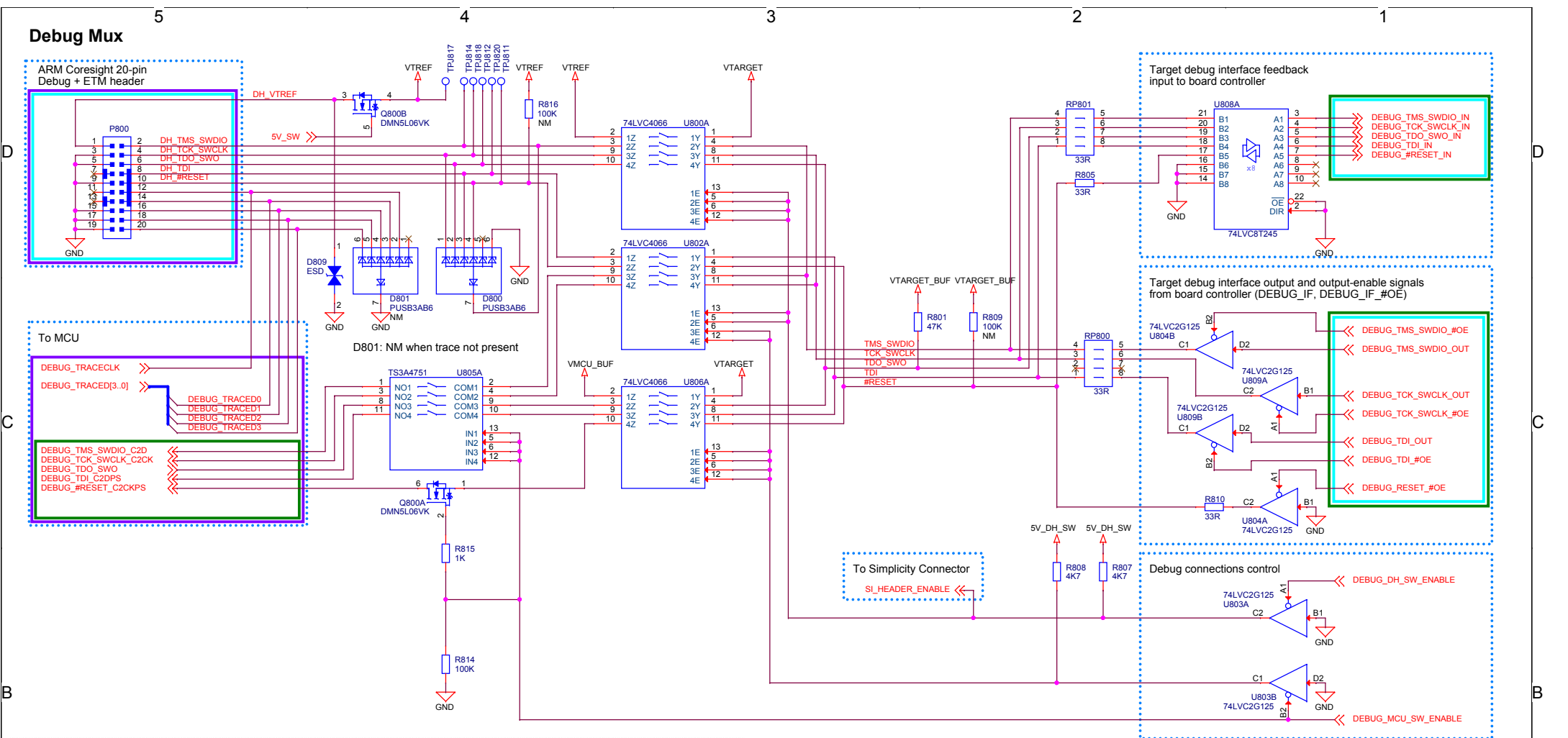


Sheet  
7 of 13

## A







Mode	DEBUG_DH_SW_ENABLE	DEBUG_MCU_SW_ENABLE	DEBUG_IF_#OE	VTREF	VTARGET
Debug Out	1	0	0/1	External voltage	External voltage
MCU Debug	0	1	0/1	Disconnected	VMCU
Debug In	1	1	1	VMCU	VMCU
Debug Off	0	0	1	-	-

Color coded frames indicates which groups of signal nodes that are active in a given debug mode



**SILICON LABS**

Designed MAH Approved RGU

Size A3 Sheet Modified Date Friday, April 29, 2022

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Board Name  
**EFM32PG23 Pro Kit**

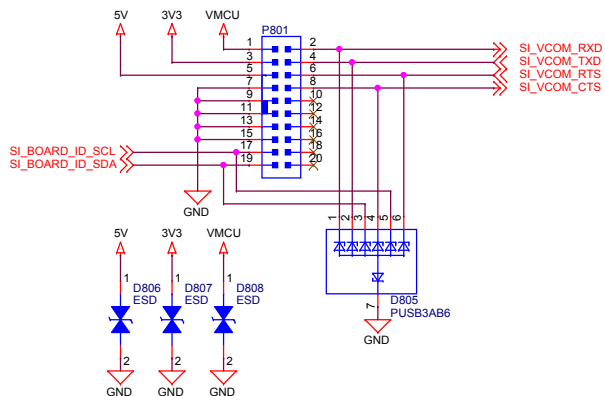
Page Title  
**Debug Interface**

Board Number  
**BRD2504A**

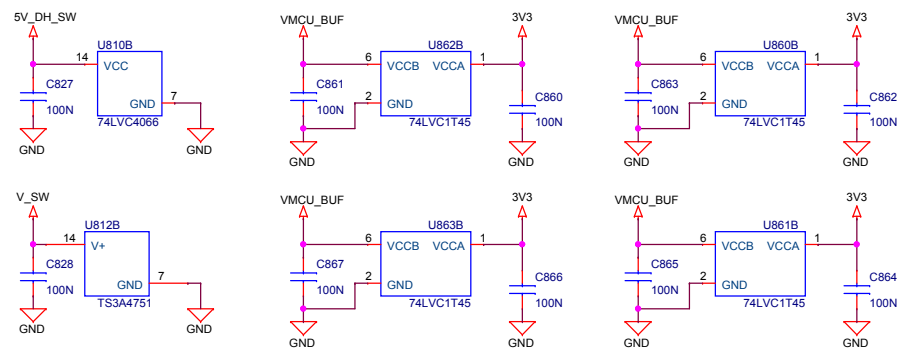
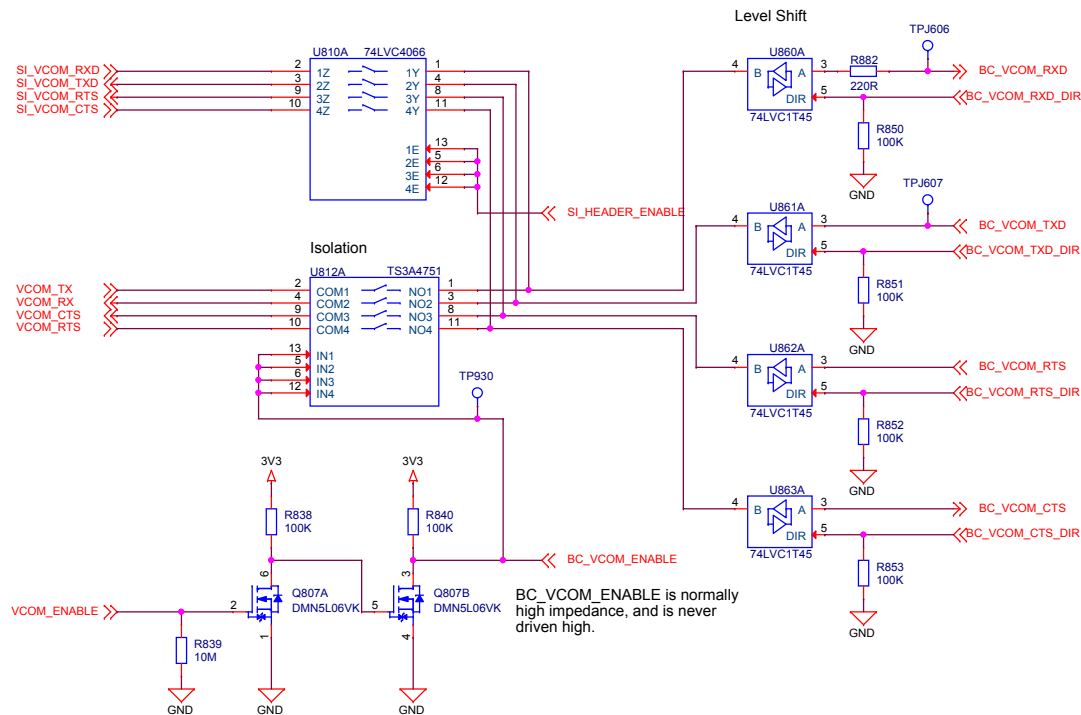
Revision  
**A04**

Sheet 9 of 13

## Simplicity Connector



## VCOM Interface



		Board Name	
		<b>EFM32PG23 Pro Kit</b>	
Designed MAH		Page Title	
Size A3		<b>Simplicity &amp; VCOM</b>	
Sheet Modified Date Friday, April 29, 2022		Board Number	Revision
		<b>BRD2504A</b>	<b>A04</b>
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Sheet 10 of 13			

**Diagram 5: J-Link USB Port (Left)**

This diagram shows the connection of a J-Link USB Port to an AMPHI 10137065 module. The module has a central shielded area with pins labeled A1 through A12 and B1 through B12. The connections are as follows:

- USB\_DM** (red) connects to A12.
- USB\_DP** (red) connects to A11.
- USB\_CC1** (red) connects to A10.
- VBUS** (purple) connects to A9.
- SBU1** (purple) connects to A8.
- D-** (purple) connects to A7.
- D+** (purple) connects to A6.
- CC1** (purple) connects to A5.
- VBUS** (purple) connects to A4.
- TX1-** (purple) connects to A3.
- TX1+** (purple) connects to A2.
- GND** (purple) connects to A1.
- GND** (purple) connects to B1.
- GND** (purple) connects to B2.
- TX2+** (purple) connects to B3.
- TX2-** (purple) connects to B4.
- VBUS** (purple) connects to B5.
- CC2** (purple) connects to B6.
- D+** (purple) connects to B7.
- D-** (purple) connects to B8.
- SBU2** (purple) connects to B9.
- VBUS** (purple) connects to B10.
- RX1-** (purple) connects to B11.
- RX1+** (purple) connects to B12.
- GND** (purple) connects to B12.

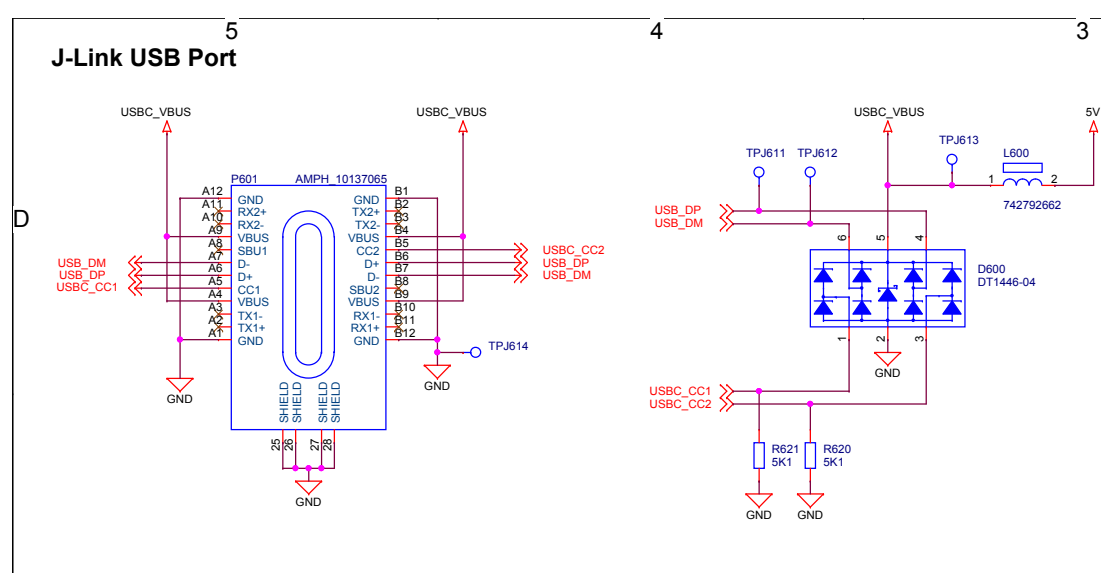
The module is labeled **P601 AMPHI 10137065**. The shielded area is labeled **SHIELD**. The module is connected to a **GND** (purple) and a **TPJ614** (blue) test point.

**Diagram 4: J-Link USB Port (Right)**

This diagram shows the connection of a J-Link USB Port to a D600 DT1446-04 module. The module is a dual in-line package (DIP) with pins labeled 1 through 12. The connections are as follows:

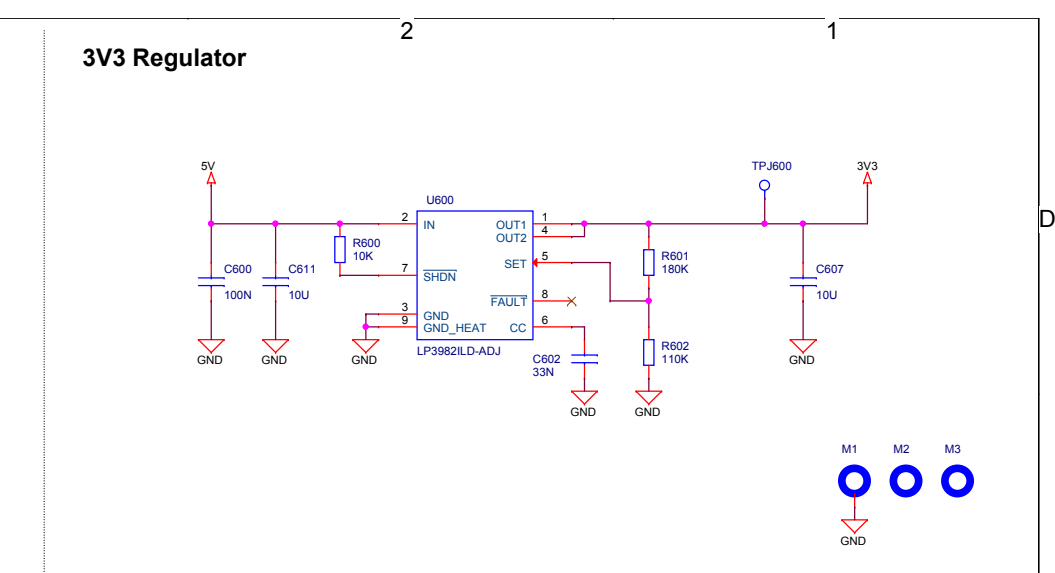
- USB\_DM** (red) connects to pin 1.
- USB\_DP** (red) connects to pin 2.
- USB\_CC1** (red) connects to pin 3.
- USB\_CC2** (red) connects to pin 4.
- VBUS** (purple) connects to pin 5.
- GND** (purple) connects to pin 6.
- GND** (purple) connects to pin 7.
- GND** (purple) connects to pin 8.
- GND** (purple) connects to pin 9.
- GND** (purple) connects to pin 10.
- GND** (purple) connects to pin 11.
- GND** (purple) connects to pin 12.

The module is labeled **D600 DT1446-04**. The module is connected to a **GND** (purple) and a **TPJ612** (blue) test point. A **TPJ611** (blue) test point is also shown. A **TPJ613** (blue) test point is connected to a **5V** (purple) supply. A **L600** (purple) inductor is connected between the **5V** supply and the **TPJ613** test point. The inductor is labeled **742792662**.



### 3V3 Regulator

The schematic diagram illustrates a 3V3 Regulator circuit. The central component is the LP3982ILD-ADJ (U600) regulator. The input is 5V, connected to the IN pin (pin 2). The IN pin is bypassed to GND with a 100nF capacitor (C600) and a 10uF capacitor (C611). The IN pin is also connected to the SHDN pin (pin 7) through a 10k resistor (R600). The SHDN pin is connected to GND (pin 3). The GND pin (pin 9) is connected to GND. The OUT1 pin (pin 1) is connected to the OUT2 pin (pin 4). The SET pin (pin 5) is connected to the OUT1/OUT2 node through a 180k resistor (R601). The FAULT pin (pin 8) is connected to GND through a 33nF capacitor (C602). The CC pin (pin 6) is connected to GND through a 110k resistor (R602). The output is 3V3, connected to the OUT1/OUT2 node. The output is bypassed to GND with a 10uF capacitor (C607). A test point TPJ600 is located at the output. Three measurement points M1, M2, and M3 are indicated at the output, with M1 connected to GND.

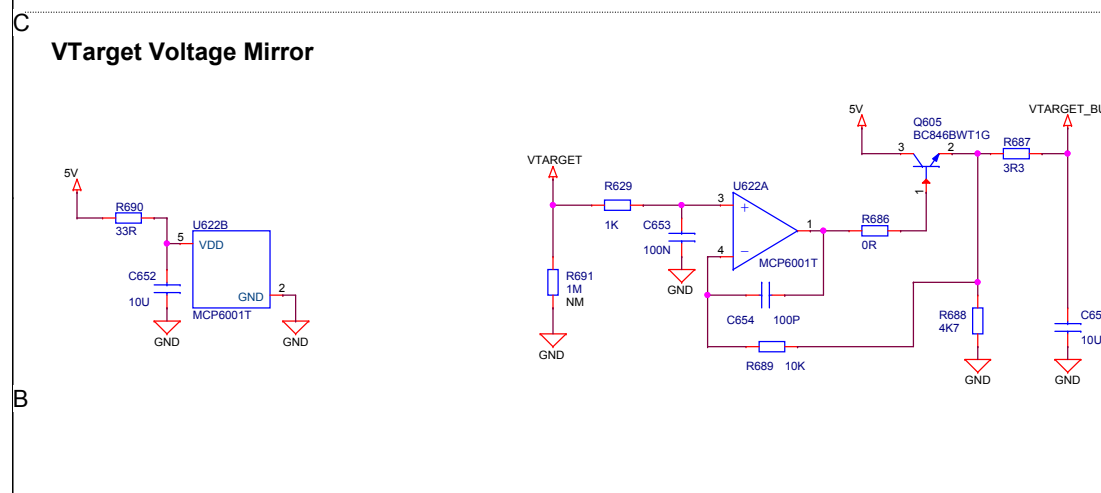


**C**

### VTarget Voltage Mirror

The circuit diagram shows the VTarget voltage mirror. It consists of two main stages. The first stage is a buffer circuit where a 5V input is connected through resistor R690 (33R) to the non-inverting input (+) of op-amp U622B (MCP6001T). A feedback capacitor C652 (10U) connects the output (pin 2) back to the non-inverting input. The output of this stage is connected to the non-inverting input (+) of a second op-amp U622A (MCP6001T). The inverting input (-) of U622A is connected to ground through a network consisting of resistor R689 (10K), capacitor C654 (100P), and resistor R691 (1M NM). The output of U622A (pin 1) is connected to the base of transistor Q605 (BC846BWT1G) through resistor R686 (0R). The emitter of Q605 is connected to ground through resistor R688 (4K7). The collector of Q605 is connected to the VTARGET output node through resistor R687 (3R3). A capacitor C653 (100N) is connected between the output of U622B and ground.

**B**



## Power Supply for Analog Switches

Analog switches used for isolation are powered by 3V6\_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated

## Power Supply for Analog Switches

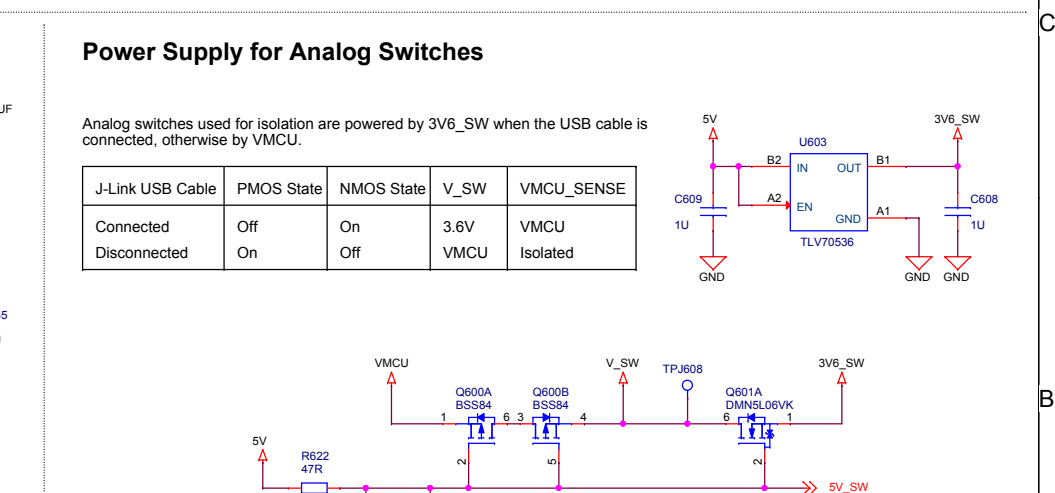
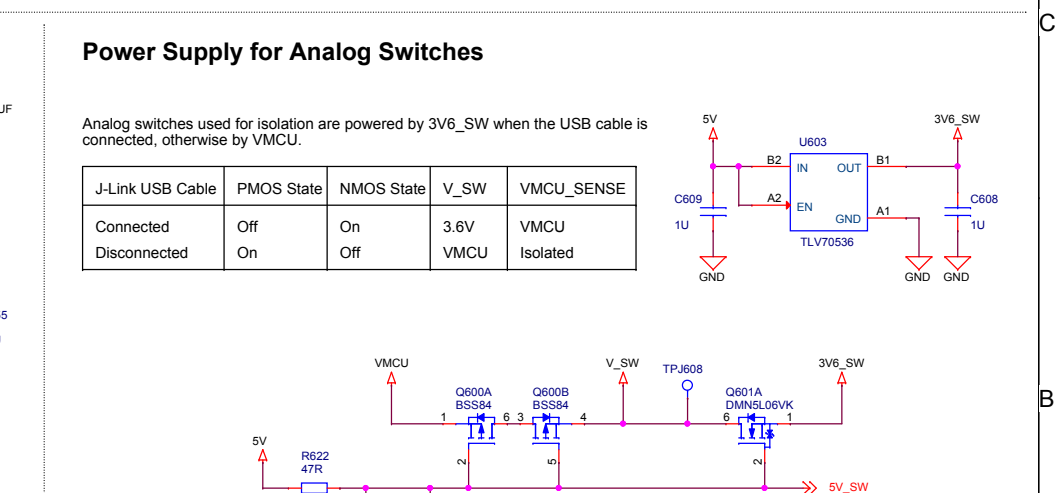
Analog switches used for isolation are powered by 3V6\_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated

## Power Supply for Analog Switches

Analog switches used for isolation are powered by 3V6\_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated



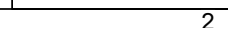
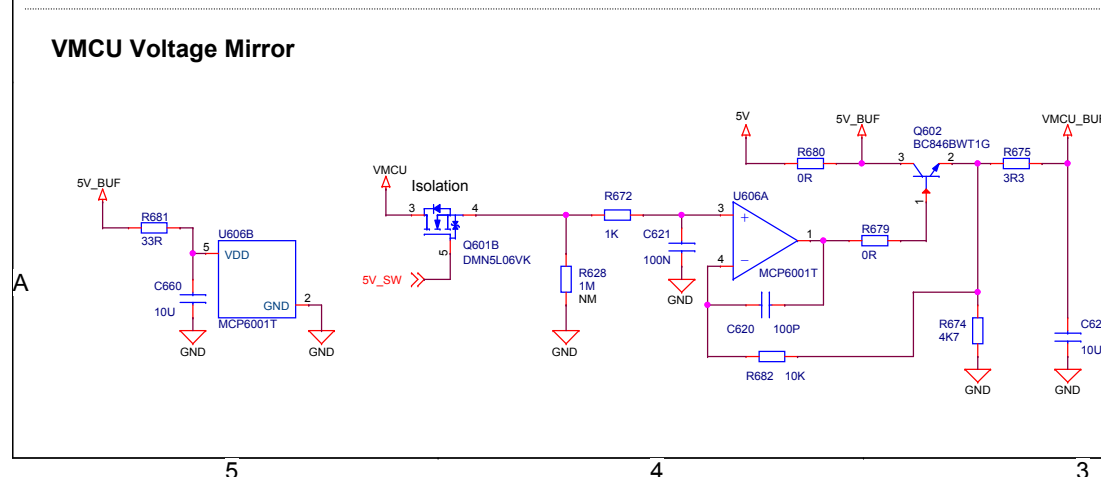
### VMCU Voltage Mirror

The schematic diagram illustrates the VMCU Voltage Mirror circuit, which is divided into three main sections labeled 5, 4, and 3.

**Section 5:** The 5V\_BUF input is connected to a 33R resistor (R681) and a 10uF capacitor (C660) to ground. The other end of the capacitor is connected to the VDD pin (pin 5) of the MCP6001T op-amp (U606B). The op-amp's GND pin (pin 2) is connected to ground.

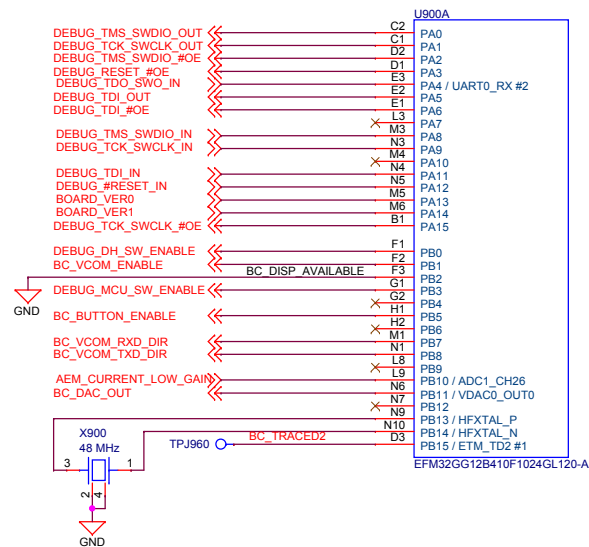
**Section 4:** The VMCU input is connected to the gate of a DMN5L06VK MOSFET (Q601B) through a 1M resistor (R628). The MOSFET's source is connected to ground, and its drain is connected to the non-inverting input (pin 3) of the MCP6001T op-amp through a 1K resistor (R672). The op-amp's inverting input (pin 4) is connected to ground through a 100nF capacitor (C621). The op-amp's output (pin 1) is connected to the base of a BC846BWT1G NPN transistor (Q602) through a 100pF capacitor (C620). The transistor's emitter is connected to ground through a 4K7 resistor (R674). The transistor's collector is connected to a 5V supply through a 0R resistor (R680) and to the VMCU\_BUF output through a 3R3 resistor (R675). A 10K resistor (R682) is connected between the output and the inverting input of the op-amp.

**Section 3:** The VMCU\_BUF output is connected to a 10uF capacitor (C62) to ground.

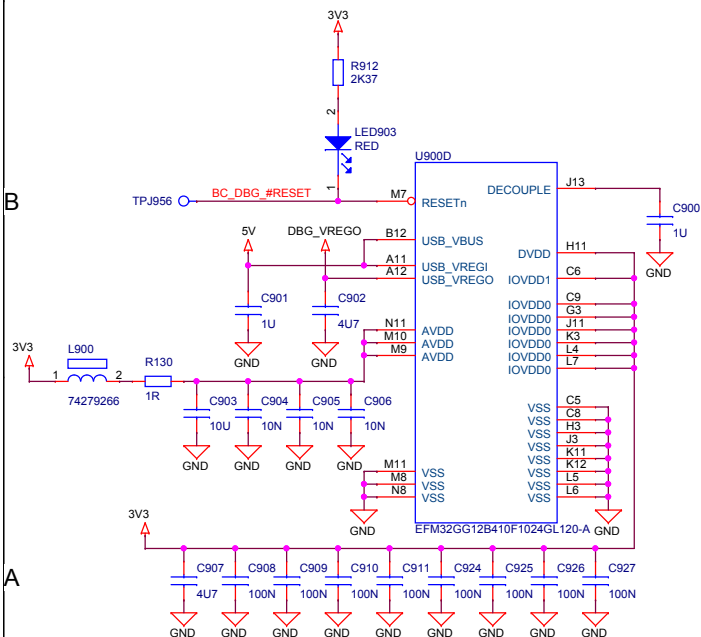


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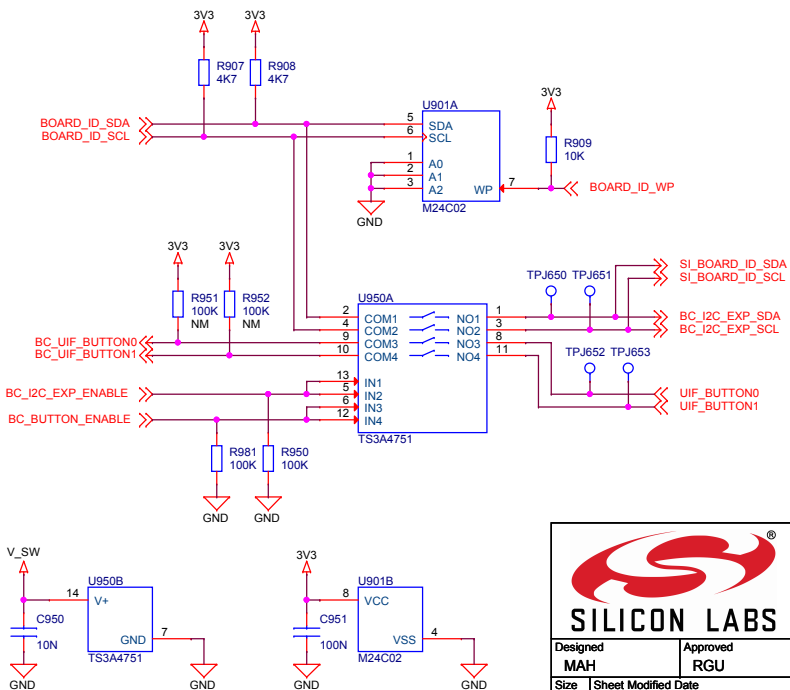
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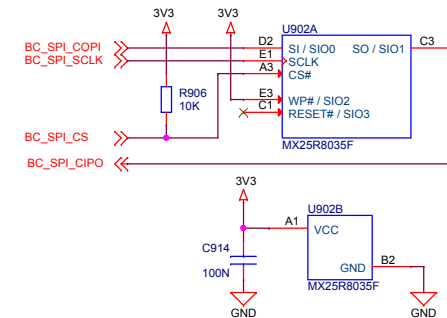
## Power & Decoupling



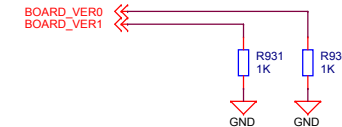
## Board ID & Button Isolation



## BC Serial Flash

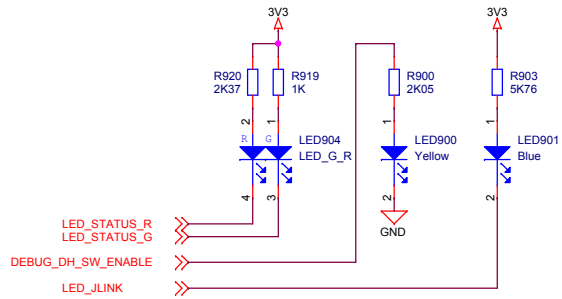


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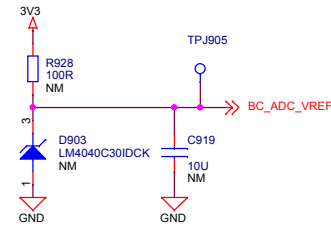


 <b>SILICON LABS</b>		Board Name	
		<b>EFM32PG23 Pro Kit</b>	
Page Title		<b>Board Controller</b>	
Designed MAH			
Board Number		Revision	
Size A3		Sheet Modified Date Friday, April 29, 2022	
<b>BRD2504A</b>		<b>A04</b>	
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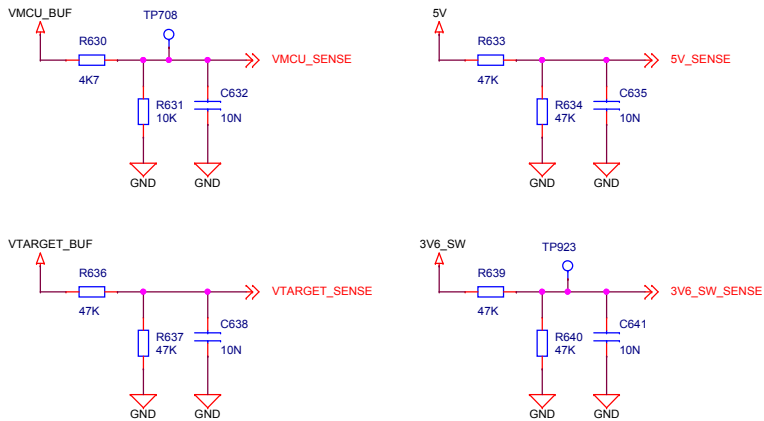
## Indicator LEDs



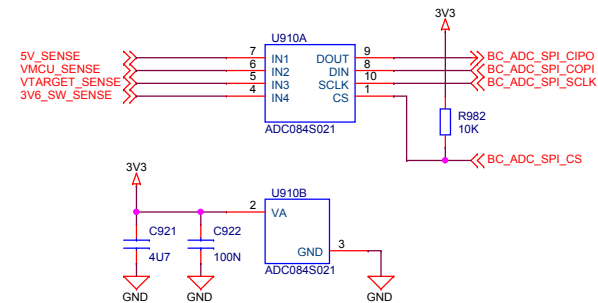
## BC ADC Reference



## BC Voltage Sense



## BC Voltage Sense ADC



		Board Name	
		EFM32PG23 Pro Kit	
Designed MAH		Page Title	
Size A3		Board Controller Misc	
Sheet Modified Date Friday, April 29, 2022		Board Number	Revision
		BRD2504A	A04
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