

*** PCB SPECIFICATION FOR BARE BOARD MANUFACTURING ***

PRODUCT OWNER : Silicon Labs
DOCUMENT/BOARD : PCB2603A Rev A00
DATE : 2021-12-08
REVISION : A00

PREPARED BY : Raghunath Yarlagadda
BOARDS pr PANEL : 12 (4 X 3)
PANEL SIZE : 210.2 x 205.4 mm
BOARD SIZE : 35.56 x 55.88mm
BOARD THICKNESS : 1.6 mm +/- 10 %
NO OF LAYERS : 8
MATERIAL(S) : Glass Epoxy FR-4, IPC-4101 (current revision) /99 or /124
(Tg min 150 C) Materials in compliance with the RoHS and
WEEE directives

MARKINGS : All PCB manufacturer's markings (logo/UL code/DC code) shall be
put in the PCB frame. No marking on the boards is allowed.
(Avoid areas reserved for DataMatrix, Barcodes or Labels)

QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications
referred to by IPC-A-600

GENERAL REQ. :- Copper must not be added or removed from inside the board
outline(s), without written consent/approval.
Use the balancing of the panel that comes with the
Gerber files (without alterations)
If applicable, the following requirements are valid:
- If Build-Up (Stack-Up) is specified, follow Build-Up,
otherwise use (board manufacturer) standard Build-Up.
- Break-away areas may be used for patterns, holes etc
by manufacturer for QA purposes.
- If V-CUT, use angle 30 +/- 5 degrees.
V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.
Use of V-CUT test pads is allowed.
- Inner radius (contour/outline) 1.2 mm, unless stated
otherwise

COPPER THK. : Cu thickness outer layers: 35 um (ca) After plating
COPPER PASSIV. : ENIG to meet IPC-4552 Class 2 requirements (current revision)
(Electroless Nickel/Immersion Gold)

SOLDER MASK : Solder Mask Color: GLOSSY BLACK
Photo Polymer Wet film
to IPC-SM-840 Class 2 (T) requirements (current revision)

VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b
Plugged and Covered Both Sides, Low CTE Plugging Paste
If Type IV-b is not available as a process, then Type IV-a
for the Top Side, and Overprinted (Tented) Bot Side is OK

LEGEND/SILKSCR. : WHITE, BOTH SIDES (TOP + BOT)

2(2)

CONTROLLED IMP : Design has Controlled impedances. FOLLOW BUILD-UP STRICTLY!
- 90 ohm (DP) $\pm 10\%$ L1, REF=L2, and L8, REF=L7,
W=0.203mm Gap=0.1mm
Gap to Coplanar plane 0.25 mm (for 90 ohm (DP))
- 50 ohm $\pm 1\%$ L1, REF=L2 , W=0.457mm Gap to coplanar plane
0.25mm(50 ohm single ended)
NOMINAL VALUES for Width, Spacing and VIA Diameter:
Cu TRACK(TRACE) : Minimum conductor width : 0.1mm
Cu SPACING : Minimum conductor spacing: 0.1mm
MINIMUM VIA : Minimum via pad diameter : 0.508 mm (20 mil) (Via hole 0.25mm)
Min via hole may have more than one pad diameter.
BUILD UP :

L1	===== =====	35 um Cu (ca) After plating
	////// //////// C O R E //////////	304 um
L2	===== =====	18 um Cu (0.5 Oz)
	- - - - - P R E P R E G - - - - -	100 um
L3	===== =====	18 um Cu
	////// //////// C O R E //////////	100 um
L4	===== =====	18 um Cu
	- - - - - - - P R E P R E G - - - - -	300 um - - CENTER - -
L5	===== =====	18 um Cu
	////// //////// C O R E //////////	100 um
L6	===== =====	18 um Cu
	- - - - - P R E P R E G - - - - -	100 um
L7	===== =====	18 um Cu
	////// //////// C O R E //////////	304 um
L8	===== =====	35 um Cu

TEST : 100% Electrical Test
Optical test, AOI (with automatic scanner)
Visual inspection
(Generate netlist from Gerber and Drill files)

Avoid use of 2125 Prepreg

Nominal tolerances (if no other tolerances given)

PTH ± 0.10 mm for $d \leq 2.0$ mm
PTH ± 0.15 mm for $2.0 < d \leq 5.3$ mm
PTH ± 0.20 mm for $d > 5.3$ mm
NPTH ± 0.10 mm for $d \leq 5.3$ mm
NPTH ± 0.10 mm for $d > 5.3$ mm