*** PCB SPECIFICATION FOR BARE BOARD MANUFACTURING ***

PRODUCT OWNER : Silicon Labs
DOCUMENT/BOARD : PCB4001 Rev A03
DATE : 2014-10-31
REVISION : A03

PREPARED BY : Ole Jacob Bryhni Frostad
BOARDS pr PANEL: 4 (1 x 4)
PANEL SIZE : 136.0 x 280.0 mm
BOARD SIZE : 115.0 x 60.0 mm
BOARD THICKNESS: 1.6 mm +/- 10 %
NO OF LAYERS : 6
MATERIAL(S) : Glass Epoxy FR-4, IPC-4101 (current revision) /124
Materials in compliance with the RoHS and WEEE directives
MARKINGS: Logo, Week/Year, UL
(Avoid areas reserved for DataMatrix, Barcodes or Lables)
QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications
refered to by IPC-A-600
GENERAL REQ. : - Copper must not be added or removed from inside the board outline(s),
without written consent/approval.
If applicable, the following requirements are valid:
- Copper balancing may be applied on break-away-tabs,
or otherwise outside board outline(s), but must have
a minimum 1.5 mm clearance to possible fiducials.
- If Build-Up (Stack-Up) is specified, follow Build-Up,
otherwise use (board manufacturer) standard Build-Up.
- Break-away areas may be used for patterns, holes etc
by manufacturer for QA purposes.
- If V-CUT, use angle 30 +/- 5 degrees.
V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.
Use of V-CUT test pads is allowed.
- Inner radius (contour/outline) 1.2 mm, unless stated otherwise.
- Manufacturer may plug tented via holes in order to improve yield.
Tenting must then be replaced by plugging to IPC-4761 Type IV-a,
or better.
COPPER THK. : SEE BUILD-UP
COPPER PASSIV. : ENIG to meet IPC-4552 requirements (Electroless Nickel/Immersion Gold)
RESIST MASK : Solder Mask Color: BLACK (NB! NON-STANDARD)
Photo Polymer Wet film
to IPC-SM-840 Class T requirements (current revision)
Thickness minimum 8 um, maximum 20 um
VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-a
from Primary Side (TOP)
UNLESS OPTIONALLY: EXPLICIT OTHER VIA TREATMENT REQUESTED
LEGEND/SILKSCR.: WHITE, BOTH SIDES (TOP + BOT)
CONTROLLED IMP : Design has Controlled impedances. Follow Build up strictly!
Unless explicitly stated otherwise, controlled impedance
has been designed into the board. Use of test strip is
hence normally not required.
NOMINAL VALUES for Width, Spacing and VIA Diameter:
Cu TRACK(TRACE): Minimum conductor width : 0.10 mm (4 mils)
Cu SPACING : Minimum conductor spacing: 0.0889 mm (3.5 mils)
MINIMUM VIA : Minimum via pad diameter : 0.33 mm (13 mils) u-vias
Min via hole (SEE HOLE INFORMATION FURTHER DOWN)
Min via hole may have more than one pad diameter.
MINIMUM VIA : Minimum via pad diameter : 0.51 mm (20 mils) Normal vias
Min via hole (SEE HOLE INFORMATION FURTHER DOWN)
Min via hole may have more than one pad diameter.
u-vias L1-L2

(SPECIFICATION CONTINUED ON NEXT PAGE)

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BUILD UP :

u-vias L1 - L2

```
L1  ============================  42 um Cu (1.0 Oz + Plating)
    - - - - P R E P R E G - - - -  90 um
L2  ============================  33 um Cu (1.0 Oz)
    ////////// C O R E ////////// 533 um
L3  ============================  33 um Cu
- - - - - - P R E P R E G - - - - 120 um     - - CENTER - -
L4  ============================  33 um Cu
    ////////// C O R E ////////// 533 um
L5  ============================  33 um Cu
    - - - - P R E P R E G - - - -  90 um
L6  ============================  42 um Cu
```

(Approximate Prepreg thicknesses)

TEST : 100% Electrical Test
Optical test, AOI (with automatic scanner)
Visual inspection
(Generate netlist from Gerber and Drill files)

Avoid use of 2125 Prepreg

If NB! is used in this specification, it means:
abbreviation for nota bene!, a Latin expression meaning "note well!"

(SPECIFICATION CONTINUED ON NEXT PAGE)

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NC DRILL - HOLE INFORMATION:

WARNING: Drill dimensions must be taken from the Excellon (.exc) file(s).
NON-PLATED holes may have a small center marker in the Gerber files.
Under no circumstance must these Gerber flashes be mistaken for the
hole drill dimensions!

The drill file may contain slots. See drill information below.
The Gerber file mb4001.gex may also contain slot information.
Dimensions for the finished board (after plating).
Tolerances +/- 0.1 mm, unless specified otherwise below.
Via Holes +0.05 mm/-Via Size, unless specified otherwise below.

PLATED HOLES:
T01 VH DIA = 0.25 mm QTY = 3760 (VIA-HOLES)
T02 VH DIA = 0.3 mm QTY = 1256 (VIA-HOLES)
T03 PTH DIA = 0.8 mm QTY = 32
T04 PTH DIA = 1.0 mm QTY = 296
T05 PTH DIA = 1.45 mm QTY = 16
T06 PTH DIA = 1.6 mm QTY = 8
T07 PTH DIA = 1.8 mm QTY = 8
T08 PTH DIA = 3.0 mm QTY = 4

NON-PLATED HOLES:
T09 NP DIA = 0.9 mm QTY = 8
T10 NP DIA = 1.8 mm QTY = 8
T11 NP DIA = 3.0 mm QTY = 8
T12 NP DIA = 3.25 mm QTY = 8

The following are u-vias
(Microvias (Blind vias), Stacked Microvias and/or Burried vias)

PLATED HOLES u-via L1-L2 (in separate file):
T01 VH DIA = 0.15 mm QTY = 488

Contec Electronics AS * ECAD Center * Norway
email: post@contecel.com URL: www.contecel.com
Phone: +47 6677 5340 or +47 472 55 462 Fax: +47 6677 5341

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