

*** PCB SPECIFICATION FOR BARE BOARD MANUFACTURING ***

PRODUCT OWNER : Silicon Labs
DOCUMENT/BOARD : PCB4002A_Rev A04
DATE : 2021-11-04
REVISION : A04

PREPARED BY : Øyvind Schibsted
BOARDS pr PANEL: 4 (1 x 4)
PANEL SIZE : 141.0 x 280.0 mm
BOARD SIZE : 125.0 x 60.0 mm
BOARD THICKNESS: 1.6 mm +/- 10 %
NO OF LAYERS : 8
u-vias L1-L2
u-vias L2-L3
MATERIAL(S) : Glass Epoxy FR-4, IPC-4101 (current revision) /99 or /124 (Tg min 150 C)
Materials in compliance with the RoHS and WEEE directives
MARKINGS : All PCB manufacturer's markings (logo/UL code/DC code)
shall be put in the PCB frame. No marking on the boards is allowed.
(Avoid areas reserved for DataMatrix, Barcodes or Labels)
QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications
referred to by IPC-A-600
GENERAL REQ. : - Copper, e.g. balancing, must not be added or removed from inside
the board outline(s), without written consent/approval.
If applicable, the following requirements are valid:
- Copper balancing may be applied on break-away-tabs,
or otherwise outside board outline(s), but must have
a minimum 1.5 mm clearance to possible fiducials.
- If Build-Up (Stack-Up) is specified, follow Build-Up,
otherwise use (board manufacturer) standard Build-Up.
- Break-away areas may be used for patterns, holes etc
by manufacturer for QA purposes.
- If V-CUT, use angle 30 +/- 5 degrees.
V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.
Use of V-CUT test pads is allowed.
- Inner radius (contour/outline) 1.2 mm, unless stated otherwise.
COPPER THK. : SEE BUILD-UP
COPPER PASSIV. : ENIG to meet IPC-4552 Class 2 requirements (current revision)
(Electroless Nickel/Immersion Gold)
SOLDER MASK : IPC-SM-840 Class 2 (T) (current revision)
Solder Mask Color: GLOSSY BLACK
VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b
Plugged and Covered Both Sides, Low CTE Plugging Paste
If Type IV-b is not available as a process, then Type IV-a
for the Top Side, and Overprinted (Tented) Bot Side is OK
LEGEND/SILKSCR.: WHITE, BOTH SIDES (TOP + BOT)
CONTROLLED IMP : Edge-coupled Coated Microstrip:
CONTROLLED IMP : 90 ohm (DP) +/-10% L8, REF=L7, W=0.1mm Gap=0.13mm
Edge-coupled Offset Stripline:
100 ohm (DP) +/-10% L1, REF=L2, W=0.1mm mil Gap=0.28mm
NOMINAL VALUES for Width, Spacing and VIA Diameter:
Cu TRACK(TRACE): Minimum conductor width : 0.10 mm
Cu SPACING : Minimum conductor spacing: 0.0889 mm (3.5 mil)
MINIMUM VIA : Minimum via pad diameter : 0.33 mm (13 mils) u-vias Via holes 0.15 mm
Min via hole may have more than one pad diameter.
MINIMUM VIA : Minimum via pad diameter : 0.51 mm (20 mils) Normal vias Via holes 0.25
Min via hole may have more than one pad diameter.

(SPECIFICATION CONTINUED ON NEXT PAGE)

BUILD-UP :

u-vias L1 - L2 & L2 - L3

L1	===== =====	29.3	um	Cu (ca)
- - -	- P R E P R E G - \ / - - -	72.58	um	
L2	===== =====	35	um	Cu (1.0 Oz)
- - -	- P R E P R E G - \ / - - -	72.58	um	
L3	===== =====	35	um	Cu
/////	///// C O R E /////	400	um	
L4	===== =====	35	um	Cu
- - - -	- P R E P R E G - - - -	207	um	- - CENTER - -
L5	===== =====	35	um	Cu
/////	///// C O R E /////	400	um	
L6	===== =====	35	um	Cu
- - -	- P R E P R E G - - - -	72.58	um	
L7	===== =====	35	um	Cu
- - -	- P R E P R E G - - - -	72.58	um	
L8	===== =====	29.3	um	Cu

(Approximate Prepreg thicknesses)

TEST : 100% Electrical Test
Optical test, AOI (with automatic scanner)
Visual inspection
(Generate netlist from Gerber and Drill files)

Avoid use of 2125 Prepreg

If NB! (Nota Bene) is used in this specification, it is latin, meaning "notice well" or "observe particularly"

Nominal tolerances (if no other tolerances given)
PTH +/- 0.10 mm for d <= 2.0 mm
PTH +/- 0.15 mm for 2.0 < d <= 5.3 mm
PTH +/- 0.20 mm for d > 5.3 mm
NPTH +/- 0.05 mm for d <= 5.3 mm
NPTH +/- 0.10 mm for d > 5.3 mm

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