

## \*\*\* PCB SPECIFICATION FOR BARE BOARD MANUFACTURING \*\*\*

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PRODUCT OWNER : Silicon Labs  
DOCUMENT/BOARD : PCB4108A Rev A02  
DATE : 2021-06-01  
REVISION : A02

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PREPARED BY : Tamas Bodi  
BOARDS pr PANEL: 12 (4 x 3)  
PANEL SIZE : 210.2 x 205.4 mm  
BOARD SIZE : 35.56 x 55.88 mm (1.4" x 2.2")  
BOARD THICKNESS: 1.6 mm +/- 10 %  
NO OF LAYERS : 2  
MATERIAL(S) : Glass Epoxy FR-4, IPC-4101 (current revision) /101 or /121 (Tg min 130 C)  
Materials in compliance with the RoHS and WEEE directives  
MARKINGS : All PCB manufacturer's markings (logo/UL code/DC code)  
shall be put in the PCB frame. No marking on the boards is allowed.  
(Avoid areas reserved for DataMatrix, Barcodes or Labels)  
QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications  
referred to by IPC-A-600  
GENERAL REQ. : - Copper must not be added or removed from inside the board outline(s),  
without written consent/approval.  
Use the balancing of the panel that comes with the  
Gerber files (without alterations)  
If applicable, the following requirements are valid:  
- If Build-Up (Stack-Up) is specified, follow Build-Up,  
otherwise use (board manufacturer) standard Build-Up.  
- Break-away areas may be used for patterns, holes etc  
by manufacturer for QA purposes.  
- If V-CUT, use angle 30 +/- 5 degrees.  
V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.  
Use of V-CUT test pads is allowed.  
- Inner radius (contour/outline) 1.2 mm, unless stated otherwise.  
COPPER THK. : Cu thickness outer layers: 35 um (ca) After plating  
COPPER PASSIV. : OSP (Organic Solderability Preservative)  
RESIST MASK : Solder Mask Color: GLOSSY BLACK  
Photo Polymer Wet film  
VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b  
Plugged and Covered Both Sides, Low CTE Plugging Paste  
If Type IV-b is not available as a process, then Type IV-a  
for the Top Side, and Overprinted (Tented) Bot Side is OK  
LEGEND/SILKSCR.: WHITE, BOTH SIDES (TOP + BOT)  
Edge-coupled Coated Microstrip:  
CONTROLLED IMP : 90 ohm (DP) +/-10% L1, REF=L2, W=0.203mm Gap=0.127mm  
Gap to Coplanar plane 0.127 mm (for 90 ohm (DP))  
NOMINAL VALUES for Width, Spacing and VIA Diameter:  
Cu TRACK(TRACE): Minimum conductor width : 0.10 mm  
Cu SPACING : Minimum conductor spacing: 0.125 mm  
MINIMUM VIA : Minimum via pad diameter : 0.508 mm (20 mil) (via hole 0.25 mm)  
Min via hole may have more than one pad diameter.  
(SPECIFICATION CONTINUED ON NEXT PAGE)

TEST

: 100% Electrical Test  
Optical test, AOI (with automatic scanner)  
Visual inspection  
(Generate netlist from Gerber and Drill files)

Avoid use of 2125 Prepreg

Nominal tolerances (if no other tolerances given)

PTH +/- 0.10 mm for  $d \leq 2.0$  mm

PTH +/- 0.15 mm for  $2.0 < d \leq 5.3$  mm

PTH +/- 0.20 mm for  $d > 5.3$  mm

NPPTH +/- 0.10 mm for  $d \leq 5.3$  mm

NPPTH +/- 0.10 mm for  $d > 5.3$  mm