

## \*\*\* PCB SPECIFICATION FOR BARE BOARD MANUFACTURING \*\*\*

PRODUCT OWNER : Silicon Labs  
DOCUMENT/BOARD : PCB4111B

DATE : 2023. 04. 27.  
REVISION : A01

PREPARED BY : Szabolcs Lorincz  
BOARDS pr PANEL : 12 (4 x 3)  
PANEL SIZE : 210.0 x 205.5 mm  
BOARD SIZE : 30.0 x 47.0 mm  
BOARD THICKNESS : 1.6 mm +/-10%  
NO OF LAYERS : 4  
MATERIAL(S) : Glass Epoxy FR-4, NEMA Class 2, UL 94V-0, Tg min 150 C  
Materials in compliance with the RoHS and WEEE directives  
MARKINGS : Logo, Week/Year, UL (ON SECONDARY SIDE (BOT))  
(Avoid areas reserved for DataMatrix, Barcodes or Labels)  
All PCB manufacturer's markings (Logo, Week/Year, UL)  
shall be put in the breakaway areas of the panel frame,  
to the bottom silkscreen. No marking on the boards is allowed!  
QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications  
referred to by IPC-A-600  
GENERAL REQ. : - Copper must not be added or removed from inside the board  
outline(s), without written consent/approval.  
Use the balancing of the panel that comes with the  
Gerber files (without alterations)  
If applicable, the following requirements are valid:  
- If Build-Up (Stack-Up) is specified, follow Build-Up,  
otherwise use (board manufacturer) standard Build-Up.  
- Break-away areas may be used for patterns, holes etc.  
by manufacturer for QA purposes.  
- If V-CUT, use angle 30 +/- 5 degrees.  
V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.  
Use of V-CUT test pads is allowed.  
- Inner radius (contour/outline) 1.2 mm, unless stated  
otherwise.  
COPPER THK. : SEE BUILD-UP  
COPPER PASSIV. : ENIG to meet IPC-4552 requirements (current revision)  
(Electroless Nickel/Immersion Gold)  
RESIST MASK : Solder Mask Color: MATTE OR GLOSSY BLACK  
Photo Polymer Wet film  
to IPC-SM-840 Class T requirements (current revision)  
Thickness minimum 8 um.  
If needed, removal of thin (less than 0.25mm) solder  
resist dams (between QFN and BGA pads) is allowed.  
VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b  
Plugged and Covered Both Sides, Low CTE non-conductive plugging  
material. If Type IV-b is not available as a process, Type IV-a  
for the Top Side, and Overprinted (Tented) Bot Side is OK.  
Vias opened on one side should be plugged only from the other  
side. (CTE: Coefficient of Thermal Expansion)  
LEGEND/SILKSCR. : WHITE, BOTH SIDES (TOP + BOT)  
NOMINAL VALUES for Width, Spacing and VIA Diameter:  
Cu TRACK(TRACE) : Minimum conductor width : 0.10 mm (4 mils)  
Cu TRACK(TRACE) : Minimum conductor spacing : 0.10 mm (4 mils)  
MINIMUM VIA : Minimum via pad diameter : 0.25 mm (10 mils)  
Minimum finished via hole diameter : 0.10 mm (4 mils)  
Min via hole may have more than one pad diameter.  
Blind vias between TOP and L1

<SPECIFICATION CONTINUED ON NEXT PAGE>

```

BUILD UP      :
TOP ==||| |=====| |== 30-38 um Cu (ca) After plating
      //||| |// PREPREG or CORE ||| |// 100um *
L1  ==||| |=====| |== 11-18 um Cu
      //||| |// PREPREG or CORE //||| |// **
L2  ==||| |=====| |== 11-18 um Cu
      - - - |// PREPREG or CORE //||| |// 100um *
BOT ==||| |=====| |== 30-38 um Cu (ca) After plating

```

\*)

The distance between Top-L1 and Bottom-L2 should be as close to 100 um as possible! +/-10um tolerance is allowed.

\*\*)

Select Center Prepreg thickness in order to reach specified board thickness

```

TEST          : 100% Electrical Test
                Optical test, AOI (with automatic scanner)
                Visual inspection
                (Generate netlist from Gerber and Drill files)

                Avoid use of 2125 Prepreg

```

#### NC DRILL - HOLE INFORMATION:

WARNING : Drill dimensions must be taken from the Excellon (.DRL) file(s), and the drill report file(s) (.DRR).  
 NON-PLATED holes may have a small center marker in the Gerber files.  
 Under no circumstance must these Gerber flashes be mistaken for the hole drill dimensions!

The drill data may contain slots (in a separate file).

Dimensions for the finished board (after plating).

Nominal tolerances (if no other tolerances given)

PTH +/- 0.10 mm for d <= 2.0 mm

PTH +/- 0.15 mm for 2.0 < d <= 5.3 mm

PTH +/- 0.20 mm for d > 5.3 mm

NPTH +/- 0.10 mm for d <= 5.3 mm

NPTH +/- 0.10 mm for d > 5.3 mm

The board may contain a special testpoint on the bottom layer with an exposed ground copper ring around the testpoint. This exposed copper ring is intentional. Please follow the gerbers!

Fiducials could also have different solder mask size/shape exposing or covering the surrounding copper. Please follow the gerbers for those as well!