

## \*\*\* PCB SPECIFICATION FOR BARE BOARD MANUFACTURING \*\*\*

PRODUCT OWNER : Silicon Labs  
 DOCUMENT/BOARD : PCB4161A

---

DATE : 2017.01.26.  
 REVISION : A01

---

PREPARED BY : Tamas Bodi  
 BOARDS pr PANEL: 12 (4 X 3)  
 PANEL SIZE : 210.2 x 205.4 mm  
 BOARD SIZE : 30.0 x 51 mm  
 BOARD THICKNESS: 1.6 mm +/- 10 %  
 NO OF LAYERS : 6  
 MATERIAL(S) : Glass Epoxy FR-4, IPC-4101 (current revision) /124, /126 or /129 Td min 340 C (Decomposition Temperature), Tg min 170 C CTE, Z-axis max 3.5 % (50 - 260 C)  
 Materials in compliance with the RoHS and WEEE directives

MARKINGS : Logo, Week/Year, UL (ON SECONDARY SIDE (BOT))  
 (Avoid areas reserved for DataMatrix, Barcodes or Labels)  
 All PCB manufacturer's markings (Logo, Week/Year, UL) shall be put in the PCB frame. No marking on the boards is allowed.

QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications referred to by IPC-A-600

GENERAL REQ. : - Copper must not be added or removed from inside the board outline(s), without written consent/approval.  
 Use the balancing of the panel that comes with the Gerber files (without alterations)  
 If applicable, the following requirements are valid:  
 - If Build-Up (Stack-Up) is specified, follow Build-Up, otherwise use (board manufacturer) standard Build-Up.  
 - If V-CUT, use angle 30 +/- 5 degrees.  
 V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.  
 Use of V-CUT test pads is allowed.  
 - Inner radius (contour/outline) 1.2 mm, unless stated otherwise.

COPPER THK. : SEE BUILD-UP  
 COPPER PASSIV. : ENIG to meet IPC-4552 requirements (current revision) (Electroless Nickel/Immersion Gold)

RESIST MASK : Solder Mask Color: BLACK (NB! NON-STANDARD)  
 Photo Polymer Wet film  
 to IPC-SM-840 Class 2 (T) requirements (current revision)  
 Thickness minimum 8 um, maximum 20 um

VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b  
 Plugged and Covered Both Sides, Low CTE Plugging Paste  
 If Type IV-b is not available as a process, then Type IV-a for the Top Side, and Overprinted (Tented) Bot Side is OK  
 u-Vias (microvias) must be 100% Copper Filled

LEGEND/SILKSCR.: WHITE, BOTH SIDES (TOP + BOT)

CONTROLLED IMP : Design has Controlled impedances. FOLLOW BUILD-UP STRICTLY!  
 Unless explicitly stated otherwise, controlled impedance has been designed into the board. Use of test strip is hence normally not required.  
 NOMINAL VALUES for width, Spacing and VIA Diameter:

Cu TRACK(TRACE): Minimum conductor width : 0.10 mm (4 mils)  
 Cu SPACING : Minimum conductor spacing : 0.10 mm (4 mils)  
 MINIMUM VIA : Minimum via pad diameter : 0.33 mm (13 mils) u-vias  
 Minimum via hole diameter : 0.15 mm (5.9 mils) u-vias  
 Min via hole may have more than one pad diameter.

MINIMUM VIA : Minimum via pad diameter : 0.51 mm (20 mils) Normal vias  
 Minimum via hole diameter : 0.25 mm (9.8 mils) Normal vias  
 Min via hole may have more than one pad diameter.  
 Blind vias L1-L2  
 u-vias L1-L2

(SPECIFICATION CONTINUED ON NEXT PAGE)

```

BUILD UP      :
L1 =====|=====|===== 38 um Cu (ca) After plating
- - -| - P R E P R E G -| - - - 90 um *)
L2 =====|=====|===== 18 um Cu (ca) (0.5 oz)
/////|///// C O R E ///// 180 um *)
L3 =====|=====|===== 18 um Cu
- - -| - P R E P R E G - - - - - **) - - CENTER - -
L4 =====|=====|===== 18 um Cu
/////|///// C O R E ///// 180 um
L5 =====|=====|===== 18 um Cu
- - -| - P R E P R E G - - - - - 90 um
L6 =====|=====|===== 38 um Cu

```

\*)

The distance from bottom of L1 to top of L3 should be as close to 300 um as possible!

\*\*)

Select Center Prepreg thickness in order to reach specified board thickness

```

TEST      : 100% Electrical Test
            Optical test, AOI (with automatic scanner)
            Visual inspection
            (Generate netlist from Gerber and Drill files)

```

Avoid use of 2125 Prepreg

If NB! is used in this specification, it means:  
 abbreviation for nota bene!, a Latin expression meaning  
 "note well!"