

*** PCB SPECIFICATION FOR BARE BOARD MANUFACTURING ***

PRODUCT OWNER : Silicon Labs
DOCUMENT/BOARD : PCB4191A
DATE : 2022. 03. 09.
REVISION : A01

PREPARED BY : Adam Sule
BOARDS pr PANEL : 2
PANEL SIZE : 210.2 x 205.4 mm
BOARD SIZE : 160 x 160 mm; 33 x 160 mm
BOARD THICKNESS : 1.55 mm +/-10%
NO OF LAYERS : 6
MATERIAL(S) : See layer stack up below.

MARKINGS : Logo, Week/Year, UL (ON SECONDARY SIDE (BOT))
(Avoid areas reserved for DataMatrix, Barcodes or Lables)
All PCB manufacturer's markings (Logo, Week/Year, UL)
shall be put in the PCB frame, No marking on the boards
is allowed

QUALITY REQ. : IPC-A-600 (current revisions) Class 2, and IPC specifications
referred to by IPC-A-600

GENERAL REQ. : - Copper must not be added or removed from inside the board
outline(s), without written consent/approval.
If applicable, the following requirements are valid:
- Copper balancing may be applied on break-away-tabs,
or otherwise outside board outline(s), but must have
a minimum 1.5 mm clearance to possible fiducials.
- If Build-Up (Stack-Up) is specified, follow Build-Up,
otherwise use (board manufacturer) standard Build-Up.
- Break-away areas may be used for patterns, holes etc.
by manufacturer for QA purposes.
- If V-CUT, use angle 30 +/- 5 degrees.
V-CUT minimum remaining thickness 0.5 +/- 0.1 mm.
Use of V-CUT test pads is allowed.
- Inner radius (contour/outline) 1.2 mm, unless stated otherwise.

COPPER THK. : SEE BUILD-UP

COPPER PASSIV. : ENIG to meet IPC-4552 Class 2 requirements (current revision)
(Electroless Nickel/Immersion Gold)

RESIST MASK : Solder Mask Color: BLACK (NBI NON-STANDARD)
Photo Polymer Wet film
to IPC-SM-840 Class T requirements (current revision)
Thickness minimum 8 um, maximum 20 um
Removal of thin solder resist dams (between QFN and BGA pads)
is allowed.

VIA HOLES : PLUGGED/FILLED, IPC-4761 (current revision) Type IV-b
Plugged and Covered Both Sides, Low CTE Plugging Paste
If Type IV-b is not available as a process, then Type IV-a
for the Top Side, and Overprinted (Tented) Bot Side is OK

LEGEND/SILKSCR. : WHITE, BOTH SIDES (TOP + BOT)

NOMINAL VALUES for Width, Spacing and VIA Diameter:

Cu TRACK(TRACE) : Minimum conductor width : 0.10 mm (4 mil)

Cu SPACING : Minimum conductor spacing : 0.10 mm (4 mil)

MINIMUM VIA : Minimum via pad diameter : 0.6 mm (23.6 mil) blind vias
Min via hole (SEE HOLE INFORMATION FURTHER DOWN)
Min via hole may have more than one pad diameter.
Blind Vias for L6-L5 connection

MINIMUM VIA : Minimum via pad diameter : 0.60 mm (23.6 mil)
Min via hole (SEE HOLE INFORMATION FURTHER DOWN)
Min via hole may have more than one pad diameter.

<SPECIFICATION CONTINUED ON NEXT PAGE>

BUILD UP :

Blind vias L5-L6

L1 ===== | |===== 35 um Cu (ca) After plating
- - - | | Core - FR4-Improved - - 200 um

L2 ===== | |===== 18 um Cu
- - - | | PREPREG - 2x2116-47 - - 240 um
- - - | | PREPREG - 7628-45 - - 180 um

L3 ===== | |===== 18 um Cu
- - - | | Core - FR4-Improved - - 200um - - CENTER - -

L4 ===== | |===== 18 um Cu
- - - | | PREPREG - 7628-45 - - 180 um
- - - | | PREPREG - 2x2116-47 - - 240 um

L5 ==| |= | |===== 18 um Cu
- | |- | | Core - FR4-Improved - - 200 um

L6 ==| |= | |===== 35 um Cu (ca) After plating

JL-2800 shall be used as base material. Core dielectric constant shall be as close to 4.3 at 2.4 GHz as possible.

TEST : 100% Electrical Test
Optical test, AOI (with automatic scanner)
Visual inspection
(Generate netlist from Gerber and Drill files)

If NBI is used in this specification, it is latin, meaning mark well or observe particularly