



EFR32FG13 Dual Band Radio Board
2.4 GHz / 868 MHz 10 dBm, VDCDC to PAVDD

Board Function	Page
Title Page	1
RF, Antenna & Power	2
EFR32 Signal Assignments	3
WSTK Connectors & Board ID	4

LEGAL NOTICE:
SILICON LABORATORIES INC. ("SILICON LABS") AND/OR ITS LICENSORS DO NOT WARRANT THE ACCURACY OR COMPLETENESS OF THIS SCHEMATIC OR ANY INFORMATION CONTAINED WITHIN THIS SCHEMATIC. IT IS PROVIDED "AS-IS" FOR REFERENCE ONLY. SILICON LABS DOES NOT WARRANT THAT THIS DESIGN WILL MEET THE SPECIFICATIONS, BE SUITABLE FOR YOUR APPLICATION OR FIT FOR ANY PARTICULAR PURPOSE, OR WILL OPERATE IN YOUR IMPLEMENTATION. SILICON LABS AND ITS LICENSORS DO NOT WARRANT THAT THE DESIGN IMPLIED IN THIS SCHEMATIC IS PRODUCTION-WORTHY. YOU SHOULD COMPLETELY VALIDATE AND TEST YOUR DESIGN IMPLEMENTATION TO CONFIRM SYSTEM FUNCTIONALITY FOR YOUR APPLICATION.



Revision History	
Rev.	Description
A00	Initial revision.
A01	Updated EFR32 revision to Rev. C. Fixing 32 kHz crystal P/N.

<Schematic Path>
SCHEMATIC1

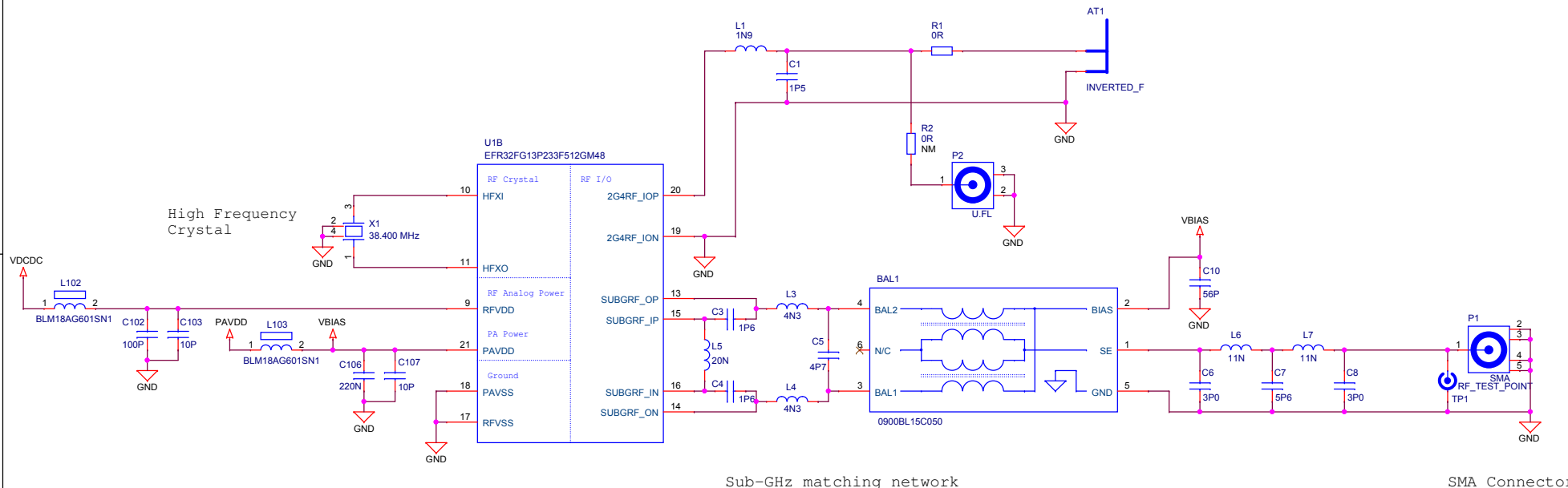
 SILICON LABS		Schematic Title	
		EFR32FG13 Dual Band 2400/868 MHz Radio Bo	
Designed: JSH		Page Title	
Approved: JNO		Title Page	
Size: A3	BOM Doc No: <Cage Code>	Document number	Revision
Design Created Date: Monday, April 02, 2012		BRD4256A	A01
Sheet Created Date: Monday, April 02, 2012		Sheet Modified Date: Friday, October 20, 2017	Sheet 1 of 4

Antenna & Radio Interface

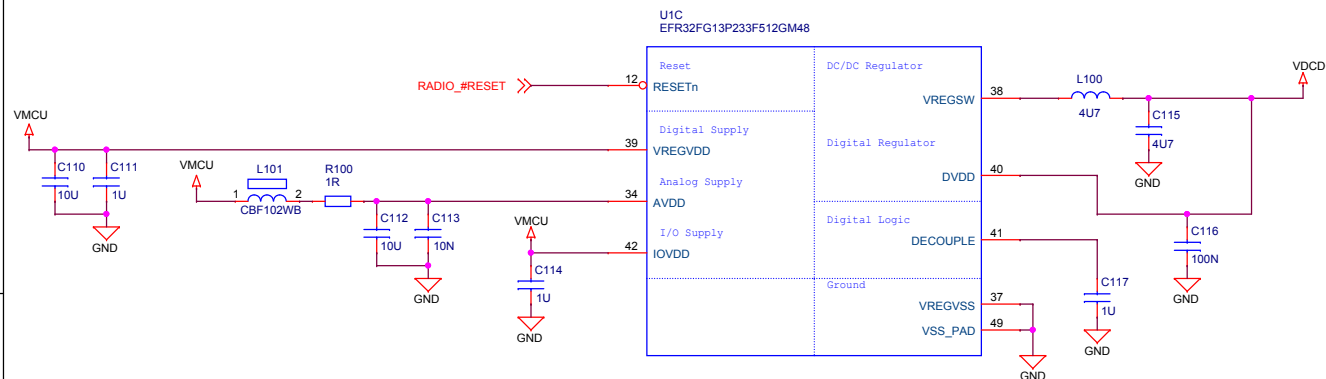
2.4 GHz matching network

PCB Antenna

High Frequency Crystal

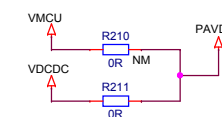


Power & Decoupling

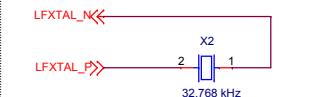


PAVDD Configuration

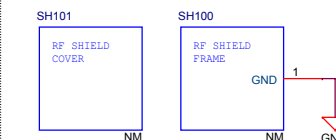
	Power Config 1 VMCU to PAVDD	Power Config 2 DCDC to PAVDD
R210	Mount	Not mount
R211	Not mount	Mount



Low Frequency Crystal



RF Shielding



<Schematic Path>
SCHEMATIC1

		Schematic Title	
EFR32FG13 Dual Band 2400/868 MHz Radio Boa		Page Title	
RF, Antenna & Power		Revision	
A01		Document number	
BRD4256A		Revision	
A01		Sheet Created Date	
Monday, April 02, 2012		Sheet Modified Date	
Friday, October 20, 2017		Sheet	
2 of 4			

The diagram illustrates the pin mapping for the EFR32 device, showing connections between various pins and internal components. The pins are organized into groups: RADIO_PA[5..0], RADIO_PB[15..11], RADIO_PC[11..6], RADIO_PD[15..13], and RADIO_PF[7..0]. The connections are as follows:

- RADIO_PA[5..0]:**
 - RADIO_PA0: US0_TX#0, EXP_HEADER12, WSTK_P9, WSTK_P9, VCOM_TX_MOSI, WSTK_F6, WSTK_F6, TP_VCOM_TX_MOSI
 - RADIO_PA1: US0_RX#0, EXP_HEADER14, WSTK_P11, WSTK_P11, VCOM_RX_MISO, WSTK_F7, WSTK_F7, TP_VCOM_RX_MISO
 - RADIO_PA2: US0_CLK#0, EXP_HEADER3, WSTK_P0, WSTK_P0, VCOM_CTS_SCLK, WSTK_F8, WSTK_F8, TP_VCOM_CTS_SCLK
 - RADIO_PA3: US0_CS#0, EXP_HEADERS, WSTK_P2, WSTK_P2, VCOM_RTS_CS, WSTK_F9, WSTK_F9, TP_VCOM_RTS_CS
 - RADIO_PA4: US1_CS#1, WSTK_P14, WSTK_P14, VCOM_ENABLE, WSTK_F5, WSTK_F5, TP_VCOM_RTS_CS
 - RADIO_PA5: FLASH_SCS, WSTK_P16, WSTK_P16, VCOM_ENABLE, WSTK_F5, WSTK_F5, TP_VCOM_RTS_CS
- RADIO_PB[15..11]:**
 - RADIO_PB11: FRC_DCLK#6, WSTK_P18, WSTK_P18, PTL_CLK, WSTK_F21, WSTK_F21, TP_VCOM_TX_MOSI
 - RADIO_PB12: FRC_DOUT#6, WSTK_P20, WSTK_P20, PTL_DATA, WSTK_F20, WSTK_F20, TP_VCOM_RX_MISO
 - RADIO_PB13: FRC_DFRAME#6, WSTK_P22, WSTK_P22, PTL_SYNC, WSTK_F19, WSTK_F19, TP_VCOM_CTS_SCLK
 - RADIO_PB14: LFXTAL_P, LFXTAL_N
 - RADIO_PB15: LFXTAL_P, LFXTAL_N
- RADIO_PC[11..6]:**
 - RADIO_PC6: US1_TX#11, FLASH_MOSI, FLASH_MISO, FLASH_SCLK
 - RADIO_PC7: US1_RX#11, FLASH_MOSI, FLASH_MISO, FLASH_SCLK
 - RADIO_PC8: US1_CLK#11, FLASH_MOSI, FLASH_MISO, FLASH_SCLK
 - RADIO_PC9: US1_CS#11, EXP_HEADER10, WSTK_P7, WSTK_P7, DISP_SI, WSTK_F16, WSTK_F16, TP_VCOM_TX_MOSI
 - RADIO_PC10: I2C0_SCL#14, EXP_HEADER15, WSTK_P12, WSTK_P12, DISP_SCLK, WSTK_F15, WSTK_F15, TP_VCOM_RX_MISO
 - RADIO_PC11: I2C0_SDA#16, EXP_HEADER16, WSTK_P13, WSTK_P13, DISP_SCLK, WSTK_F15, WSTK_F15, TP_VCOM_CTS_SCLK
- RADIO_PD[15..13]:**
 - RADIO_PD13: LETIM0_OUT0#23, WSTK_P31, WSTK_P31, DISP_EXTCOMIN, WSTK_F18, WSTK_F18, TP_VCOM_TX_MOSI
 - RADIO_PD14: US1_CS#19, WSTK_P33, WSTK_P33, DISP_SCS, WSTK_F17, WSTK_F17, TP_VCOM_RX_MISO
 - RADIO_PD15: WSTK_P35, WSTK_P35, DISP_ENABLE, WSTK_F14, WSTK_F14, TP_VCOM_CTS_SCLK
- RADIO_PF[7..0]:**
 - RADIO_PF0: DBG_SWCLK#0, WSTK_P24, WSTK_P24, DEBUG_TCK_SWCLK, WSTK_F1, WSTK_F1, TP_DEBUG_TCK_SWCLK
 - RADIO_PF1: DBG_SWDIOTMS#0, WSTK_P26, WSTK_P26, DEBUG_TMS_SWCLK, WSTK_F0, WSTK_F0, TP_DEBUG_TMS_SWCLK
 - RADIO_PF2: DBG_SWO#0/DBG_TDO#0, WSTK_P28, WSTK_P28, DEBUG_TDO_SWO, WSTK_F2, WSTK_F2, TP_DEBUG_TDO_SWO
 - RADIO_PF3: DBG_TDI#0, EXP_HEADER13, WSTK_P8, WSTK_P8, UIF_LED0, WSTK_F10, WSTK_F10, TP_DEBUG_TDI
 - RADIO_PF4: EXP_HEADER11, WSTK_P8, WSTK_P8, UIF_LED0, WSTK_F10, WSTK_F10, TP_DEBUG_TDI
 - RADIO_PF5: WSTK_P32, WSTK_P32, UIF_LED1, WSTK_F11, WSTK_F11, TP_DEBUG_TDI
 - RADIO_PF6: EXP_HEADER7, WSTK_P4, WSTK_P4, UIF_BUTTON0, WSTK_F12, WSTK_F12, TP_DEBUG_TDI
 - RADIO_PF7: EXP_HEADER9, WSTK_P6, WSTK_P6, UIF_BUTTON1, WSTK_F13, WSTK_F13, TP_DEBUG_TDI

The diagram also shows connections to various components, including the RP200, VMCU, and various resistors (R203, R204, R205, R206) and capacitors (C207). The connections are color-coded: blue for power, red for ground, and green for signal.

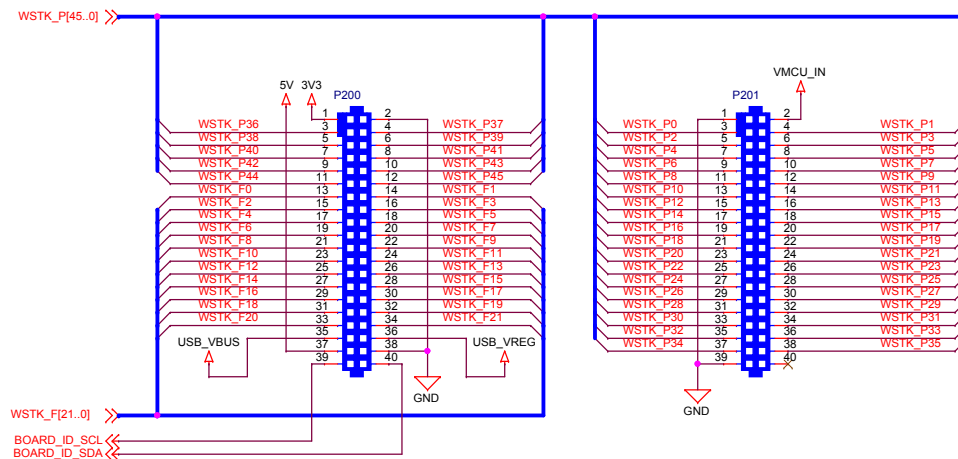
EFMR32 I/O Port Pins

Serial Flash

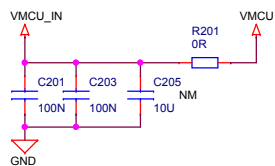
<Schematic Path>
SCHEMATIC1

		Schematic Title EFR32FG13 Dual Band 2400/868 MHz Radio	
Page Title EFR32 I/O Port Connections		Document number BRD4256A	
Designed: JSH	Approved: JNO	Revision A01	Sheet 3 of 4
Size A3	BOM Doc No: <Cage Code>	Design Created Date Monday, April 02, 2012	Sheet Modified Date Friday, October 20, 2017

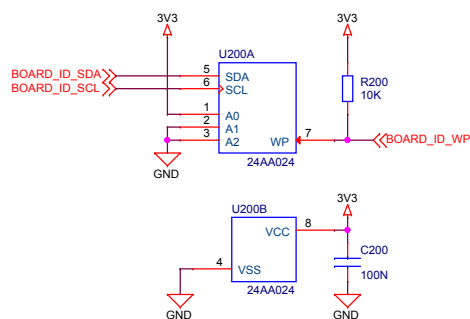
WSTK Connectors



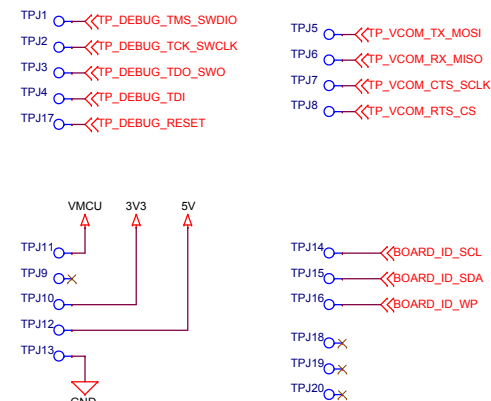
WSTK Power Decoupling



Board Identification



Test Points



<Schematic Path>
SCHEMATIC1

		Schematic Title	
		EFR32FG13 Dual Band 2400/868 MHz Radio Boa	
Designed: JSH		Page Title	
Size A3		WSTK Connectors & Board ID	
BOM Doc No: <Cage Code>		Document number	
Design Created Date: Monday, April 02, 2012		BRD4256A	
Approved: JNO		Revision	
Sheet Created Date: Tuesday, April 03, 2012		A01	
Sheet Modified Date: Friday, October 20, 2017		Sheet 4 of 4	