



**EFR32FG13 Dual Band Radio Board**  
2.4 GHz / 868 MHz 10 dBm, VDCDC to PAVDD


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Revision History	
Rev.	Description
A00	Initial revision.
A01	Updated EFR32 revision to Rev. C. Fixing 32 kHz crystal P/N.
A02	Fixing P/N for C5.

<Schematic Path>  
SCHEMATIC1

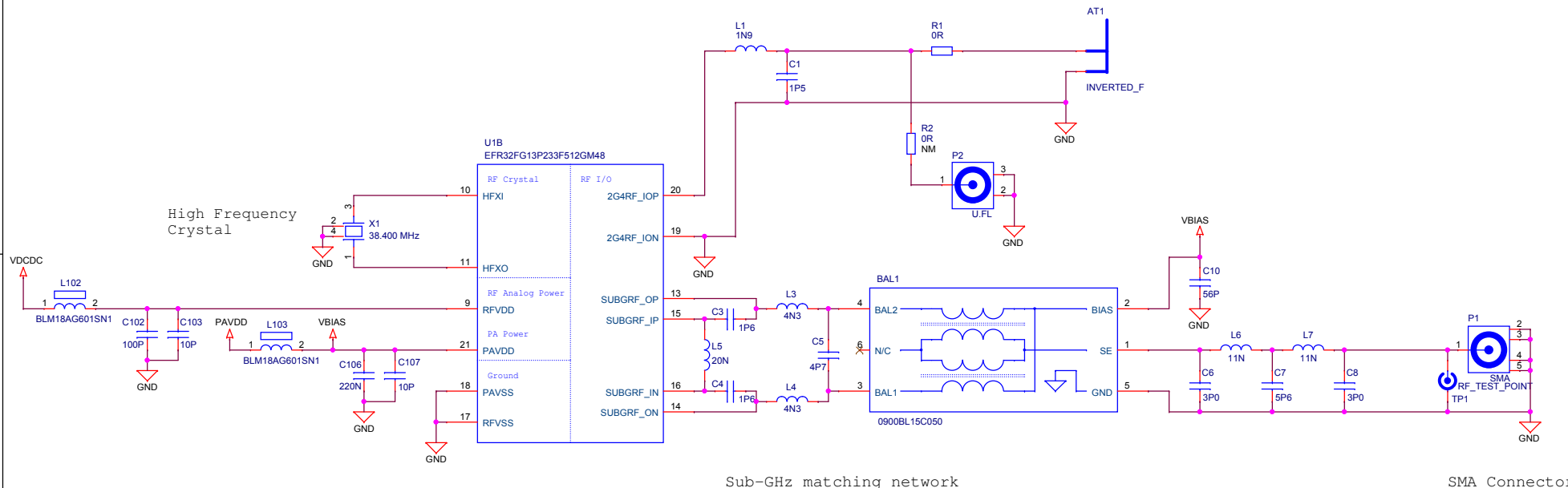
 <b>SILICON LABS</b>		Schematic Title	
		<b>EFR32FG13 Dual Band 2400/868 MHz Radio Bo</b>	
Designed: JSH		Page Title	
Approved: JNO		<b>Title Page</b>	
Size: A3	BOM Doc No: <Cage Code>	Document number	Revision
Design Created Date: Monday, April 02, 2012		<b>BRD4256A</b>	<b>A02</b>
Sheet Created Date: Monday, April 02, 2012		Sheet Modified Date: Monday, December 11, 2017	Sheet 1 of 4

# Antenna & Radio Interface

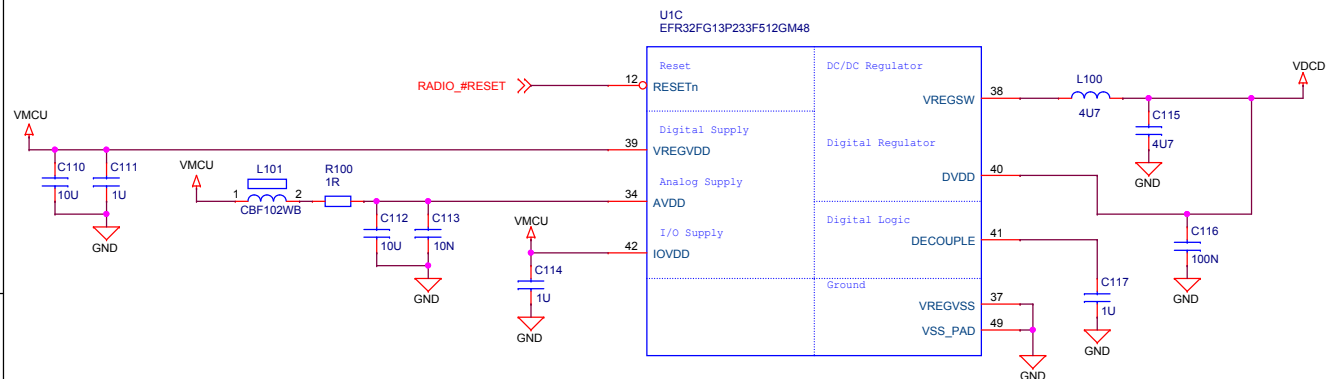
## 2.4 GHz matching network

## PCB Antenna

### High Frequency Crystal

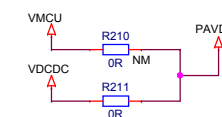


# Power & Decoupling

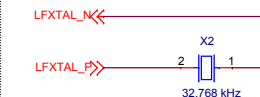


## PAVDD Configuration

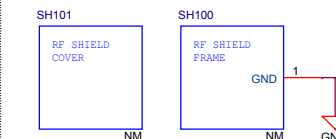
	Power Config 1 VMCU to PAVDD	Power Config 2 DCDC to PAVDD
R210	Mount	Not mount
R211	Not mount	Mount



## Low Frequency Crystal



## RF Shielding



<Schematic Path>  
SCHEMATIC1

		Schematic Title	
<b>SILICON LABS</b>		<b>EFR32FG13 Dual Band 2400/868 MHz Radio Boa</b>	
Designed: JSH Size: A3 Design Created Date: Monday, April 02, 2012		Page Title <b>RF, Antenna &amp; Power</b> Document number <b>BRD4256A</b> Sheet Created Date: Monday, April 02, 2012	
Approved: JNO BOM Doc No: <Cage Code> Sheet Modified Date: Monday, December 11, 2017		Revision <b>A02</b> Sheet 2 of 4	

The diagram illustrates the pin mapping for the EFR32 device, showing connections between various pins and internal components. The pins are organized into groups: RADIO\_PA[5..0], RADIO\_PB[15..11], RADIO\_PC[11..6], RADIO\_PD[15..13], and RADIO\_PF[7..0]. The connections are as follows:

- RADIO\_PA[5..0]:**
  - RADIO\_PA0: US0\_TX#0, EXP\_HEADER12, WSTK\_P9, WSTK\_P9, VCOM\_TX\_MOSI, WSTK\_F6, WSTK\_F6, TP\_VCOM\_TX\_MOSI
  - RADIO\_PA1: US0\_RX#0, EXP\_HEADER14, WSTK\_P11, WSTK\_P11, VCOM\_RX\_MISO, WSTK\_F7, WSTK\_F7, TP\_VCOM\_RX\_MISO
  - RADIO\_PA2: US0\_CLK#0, EXP\_HEADER3, WSTK\_P0, WSTK\_P0, VCOM\_CTS\_SCLK, WSTK\_F8, WSTK\_F8, TP\_VCOM\_CTS\_SCLK
  - RADIO\_PA3: US0\_CS#0, EXP\_HEADERS, WSTK\_P2, WSTK\_P2, VCOM\_RTS\_CS, WSTK\_F9, WSTK\_F9, TP\_VCOM\_RTS\_CS
  - RADIO\_PA4: US1\_CS#1, WSTK\_P14, WSTK\_P14, VCOM\_ENABLE, WSTK\_F5, WSTK\_F5, TP\_VCOM\_RTS\_CS
  - RADIO\_PA5: WSTK\_P16, WSTK\_P16, VCOM\_ENABLE, WSTK\_F5, WSTK\_F5, TP\_VCOM\_RTS\_CS
- RADIO\_PB[15..11]:**
  - RADIO\_PB11: FRC\_DCLK#6, WSTK\_P18, WSTK\_P18, PTL\_CLK, WSTK\_F21, WSTK\_F21, TP\_VCOM\_TX\_MOSI
  - RADIO\_PB12: FRC\_DOUT#6, WSTK\_P20, WSTK\_P20, PTL\_DATA, WSTK\_F20, WSTK\_F20, TP\_VCOM\_RX\_MISO
  - RADIO\_PB13: FRC\_DFRAME#6, WSTK\_P22, WSTK\_P22, PTL\_SYNC, WSTK\_F19, WSTK\_F19, TP\_VCOM\_CTS\_SCLK
  - RADIO\_PB14: LFXALT\_P, LFXALT\_N
  - RADIO\_PB15: LFXALT\_P, LFXALT\_N
- RADIO\_PC[11..6]:**
  - RADIO\_PC6: US1\_TX#11, FLASH\_MOSI, FLASH\_MISO, FLASH\_SCLK
  - RADIO\_PC7: US1\_RX#11, FLASH\_MOSI, FLASH\_MISO, FLASH\_SCLK
  - RADIO\_PC8: US1\_CLK#11, FLASH\_MOSI, FLASH\_MISO, FLASH\_SCLK
  - RADIO\_PC9: US1\_CS#11, EXP\_HEADER10, WSTK\_P7, WSTK\_P7, DISP\_SI, WSTK\_F16, WSTK\_F16, TP\_VCOM\_TX\_MOSI
  - RADIO\_PC10: I2C0\_SCL#14, EXP\_HEADER15, WSTK\_P12, WSTK\_P12, DISP\_SCLK, WSTK\_F15, WSTK\_F15, TP\_VCOM\_RX\_MISO
  - RADIO\_PC11: I2C0\_SDA#16, EXP\_HEADER16, WSTK\_P13, WSTK\_P13, DISP\_SCLK, WSTK\_F15, WSTK\_F15, TP\_VCOM\_CTS\_SCLK
- RADIO\_PD[15..13]:**
  - RADIO\_PD13: LETIM0\_OUT0#23, WSTK\_P31, WSTK\_P31, DISP\_EXTCOMIN, WSTK\_F18, WSTK\_F18, TP\_VCOM\_TX\_MOSI
  - RADIO\_PD14: US1\_CS#19, WSTK\_P33, WSTK\_P33, DISP\_SCS, WSTK\_F17, WSTK\_F17, TP\_VCOM\_RX\_MISO
  - RADIO\_PD15: WSTK\_P35, WSTK\_P35, DISP\_ENABLE, WSTK\_F14, WSTK\_F14, TP\_VCOM\_CTS\_SCLK
- RADIO\_PF[7..0]:**
  - RADIO\_PF0: DBG\_SWCLK#0, WSTK\_P24, WSTK\_P24, DEBUG\_TCK\_SWCLK, WSTK\_F1, WSTK\_F1, TP\_DEBUG\_TCK\_SWCLK
  - RADIO\_PF1: DBG\_SWDIOTMS#0, WSTK\_P26, WSTK\_P26, DEBUG\_TMS\_SWCLK, WSTK\_F0, WSTK\_F0, TP\_DEBUG\_TMS\_SWCLK
  - RADIO\_PF2: DBG\_SWO#0/DBG\_TDO#0, WSTK\_P28, WSTK\_P28, DEBUG\_TDO\_SWO, WSTK\_F2, WSTK\_F2, TP\_DEBUG\_TDO\_SWO
  - RADIO\_PF3: DBG\_TDI#0, EXP\_HEADER13, WSTK\_P8, WSTK\_P8, UIF\_LED0, WSTK\_F10, WSTK\_F10, TP\_DEBUG\_TDI
  - RADIO\_PF4: EXP\_HEADER11, WSTK\_P32, WSTK\_P32, UIF\_LED1, WSTK\_F11, WSTK\_F11, TP\_DEBUG\_TDI
  - RADIO\_PF5: EXP\_HEADER7, WSTK\_P4, WSTK\_P4, UIF\_BUTTON0, WSTK\_F12, WSTK\_F12, TP\_DEBUG\_TDI
  - RADIO\_PF6: EXP\_HEADER9, WSTK\_P6, WSTK\_P6, UIF\_BUTTON1, WSTK\_F13, WSTK\_F13, TP\_DEBUG\_TDI
  - RADIO\_PF7: WSTK\_P4, WSTK\_P4, UIF\_BUTTON1, WSTK\_F13, WSTK\_F13, TP\_DEBUG\_TDI

Additional components and connections include:

- FLASH\_SCS:** Connected to RADIO\_PA5 and RADIO\_PC8.
- FLASH\_MOSI, FLASH\_MISO, FLASH\_SCLK:** Connected to RADIO\_PC6, RADIO\_PC7, and RADIO\_PC8.
- RP200:** A 100R resistor connected to the expansion header pins.
- VMCU:** Connected to the VMCU pin, with a 206 resistor and a 205 resistor.
- SENSOR\_ENABLE:** Connected to the VMCU pin, with a 204 resistor and a 203 resistor.
- DEBUG\_RESET:** Connected to the RADIO\_RESET pin, with a 207 resistor and a 100N resistor.

The diagram illustrates the I/O port pins and serial flash connections for the EFR32 microcontroller. It is divided into two main sections: EFR32 I/O Port Pins and Serial Flash.

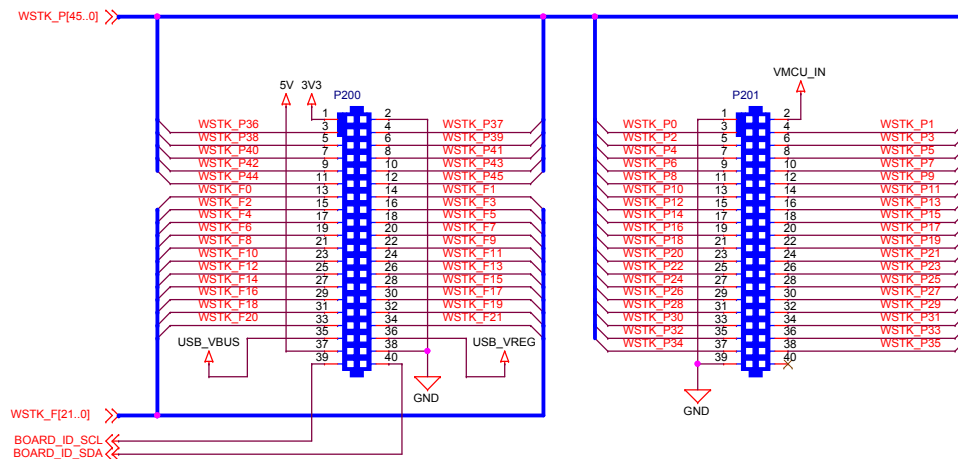
**EFR32 I/O Port Pins:** This section shows the connection of various radio pins to the EFR32 microcontroller (U1A, EFR32FG13P233F512GM48). The pins are grouped into several sets, each connected to a specific port (PA, PB, PC, PD, PF) and then to the microcontroller pins. The connections are as follows:

- RADIO\_PA[5..0]:** Connected to PA0 through PA5.
- RADIO\_PB[15..11]:** Connected to PB11 through PB15.
- RADIO\_PC[11..6]:** Connected to PC6 through PC11.
- RADIO\_PD[15..13]:** Connected to PD13 through PD15.
- RADIO\_PF[7..0]:** Connected to PF0 through PF7.

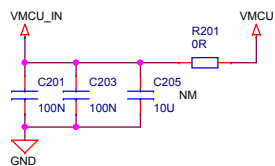
**Serial Flash:** This section shows the connection of the serial flash (U100A, MX25R8035F) to the microcontroller (U100B, MX25R8035F). The connections are as follows:

- FLASH\_MOSI:** Connected to the SI / SIO0 pin of U100A.
- FLASH\_SCLK:** Connected to the SCLK pin of U100A.
- FLASH\_SCs:** Connected to the CS# pin of U100A.
- U100A:** The serial flash is connected to the microcontroller (U100B) via the SI / SIO0, SCLK, and CS# pins.
- U100B:** The microcontroller is connected to the serial flash (U100A) via the SI / SIO0, SCLK, and CS# pins.

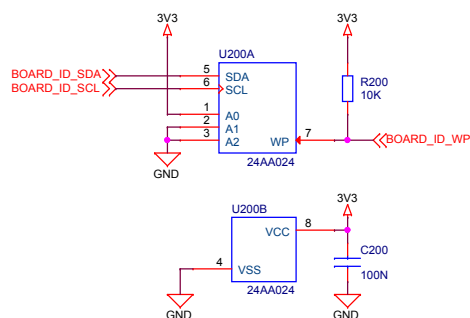
## WSTK Connectors



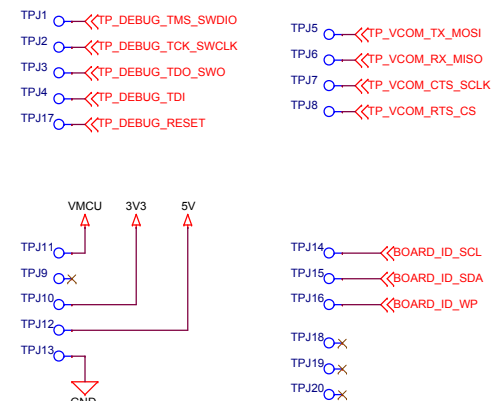
## WSTK Power Decoupling




## Board Identification



## Test Points



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SCHEMATIC1

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