



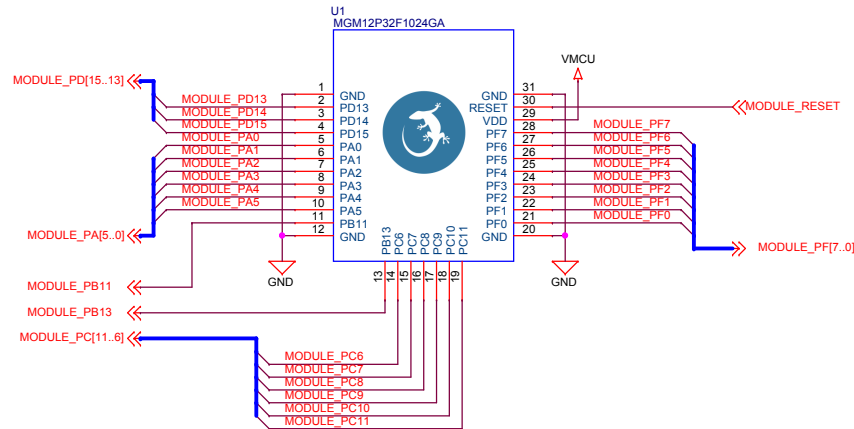
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SCHEMATIC1

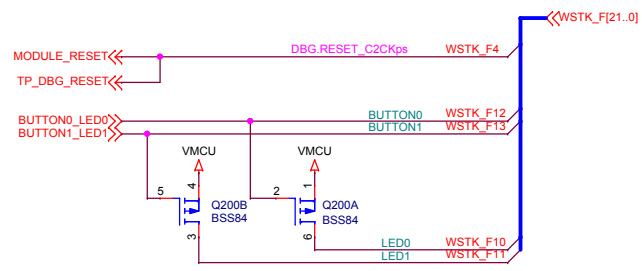
 SILICON LABS		Schematic Title	
		MGM12P Module Carrier Board	
Designed: DDB		Page Title	
Approved: JNO		Title Page	
Size A3	BOM Doc No: <Cage Code>	Document number BRD4304A	Revision A00
Design Created Date: Monday, April 02, 2012		Sheet Created Date Monday, April 02, 2012	Sheet Modified Date Wednesday, January 11, 2017
		Sheet 1 of 3	

Module Footprint



Additional Connections

Reset input from mainboard

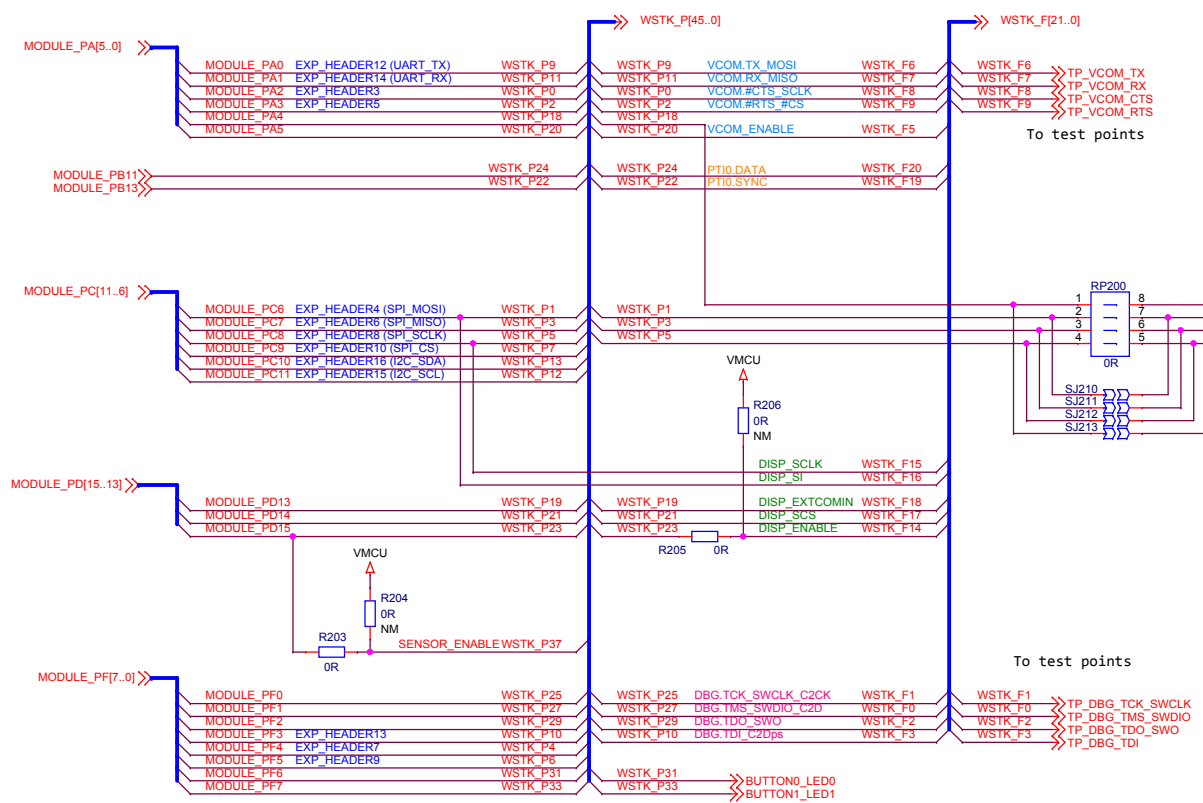


Buttons and leds connected to the same I/O pins:
Output: 0 = LED ON, 1 = LED OFF
Input: 0 = BUTTON PRESSED, 1 = BUTTON RELEASED

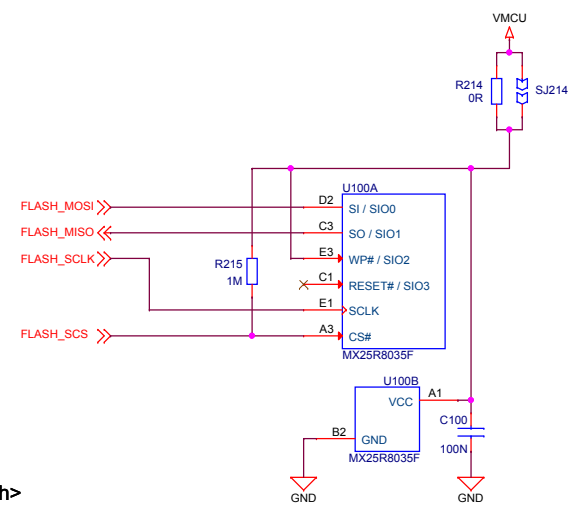
Pin Assignments

Breakout connections

Functional Connections



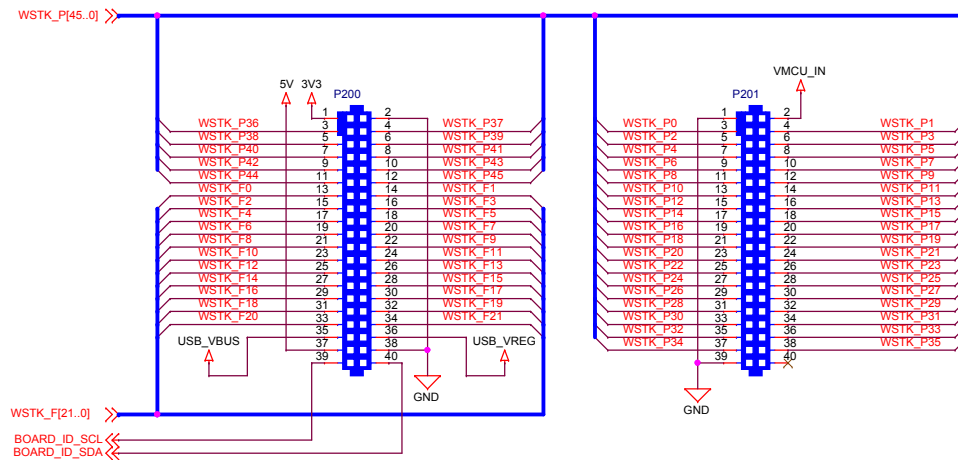
Serial Flash



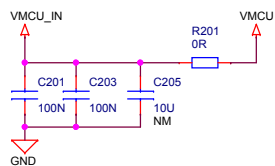
<Schematic Path>
SCHEMATIC1

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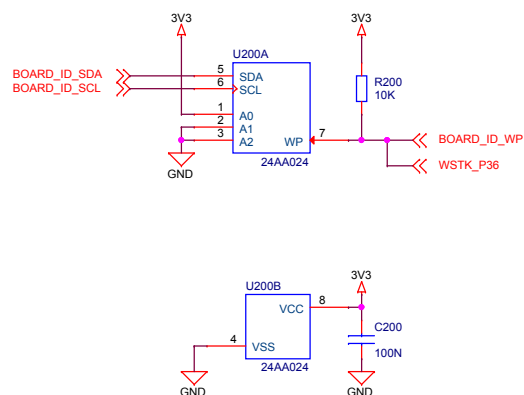
WSTK Connectors



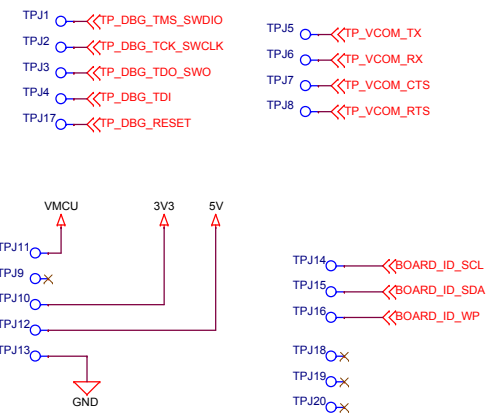
WSTK Power Decoupling



Board Identification



Test Points



<Schematic Path>
SCHEMATIC1

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