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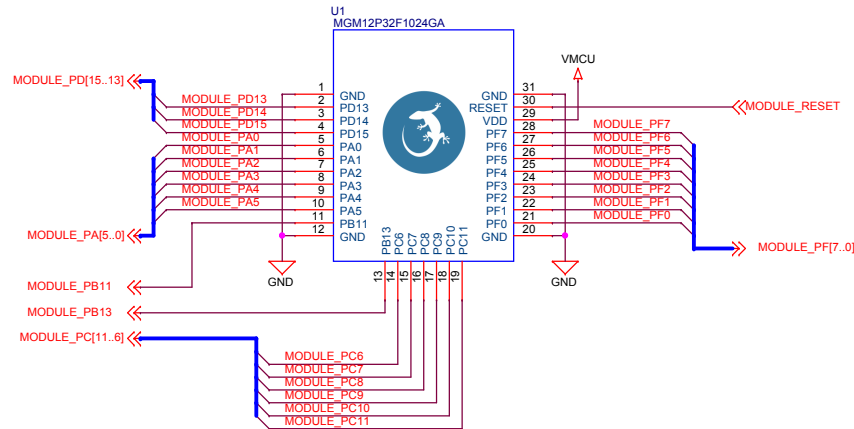


Revision History	
Rev.	Description
A00	Initial release.
A01	Updating MGM12P revision.
A02	Updating MGM12P revision.

<Schematic Path>
SCHEMATIC1

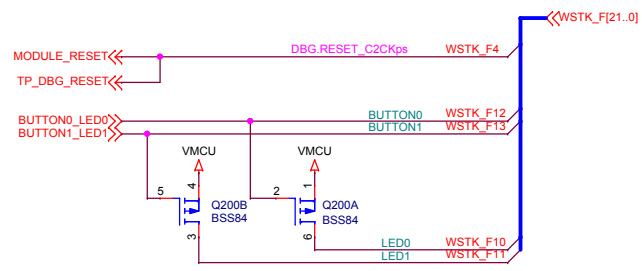
 SILICON LABS		Schematic Title	
		MGM12P Module Carrier Board	
Designed: DDB	Approved: JNO	Page Title	
Size A3		Title Page	
BOM Doc No: <Cage Code>		Document number	Revision
Design Created Date: Monday, April 02, 2012		BRD4304A	A02
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Module Footprint



Additional Connections

Reset input from mainboard

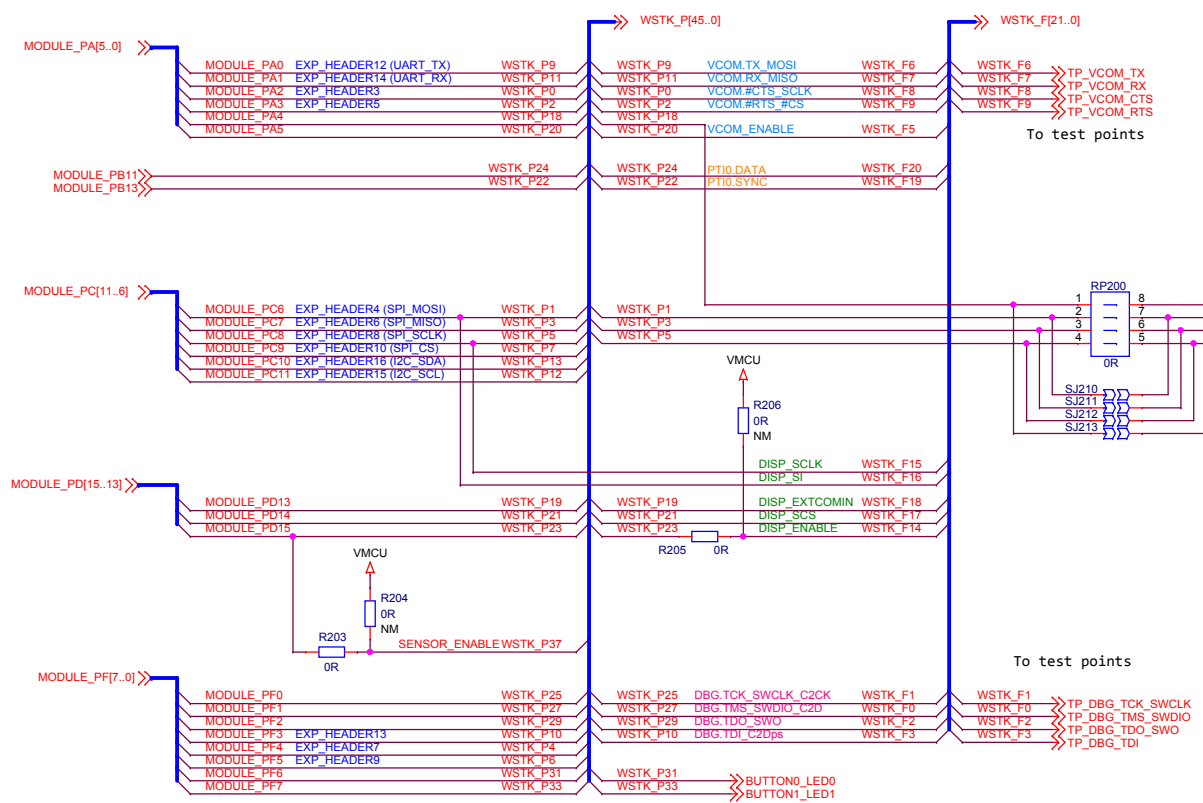


Buttons and leds connected to the same I/O pins:
Output: 0 = LED ON, 1 = LED OFF
Input: 0 = BUTTON PRESSED, 1 = BUTTON RELEASED

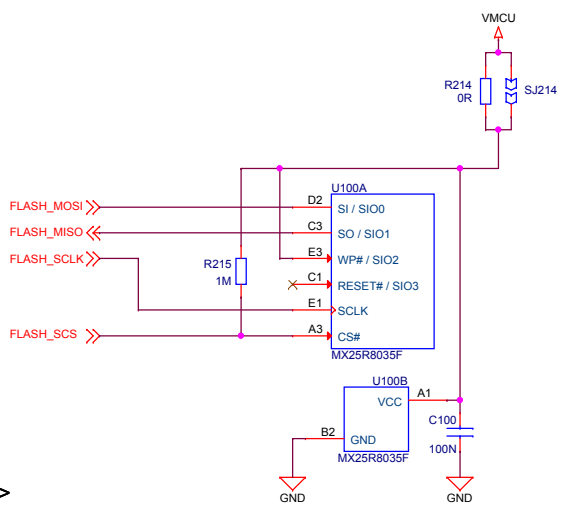
Pin Assignments

Breakout connections

Functional Connections



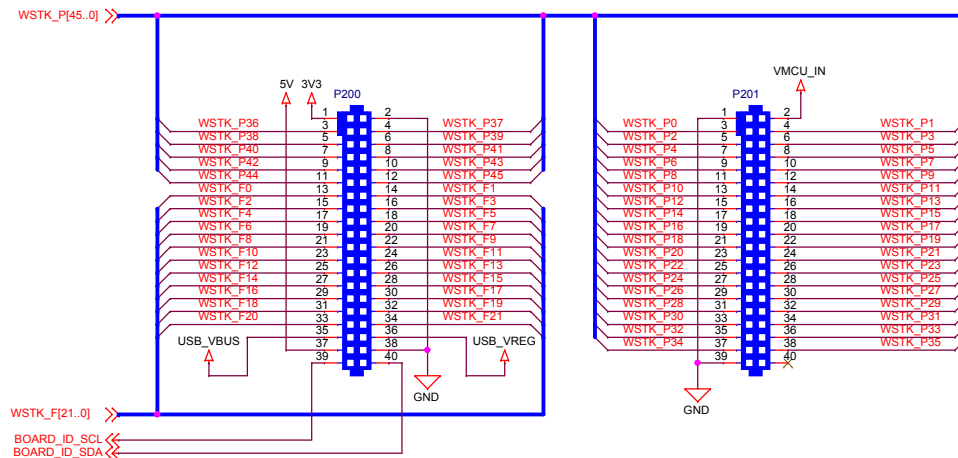
Serial Flash



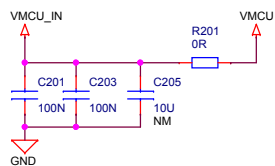
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 SILICON LABS		Schematic Title MGM12P Module Carrier Board	
		Page Title Module	
Designed: DDB	Approved: JNO	Document number BRD4304A	Revision A02
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Design Created Date: Monday, April 02, 2012		Sheet 2 of 3	

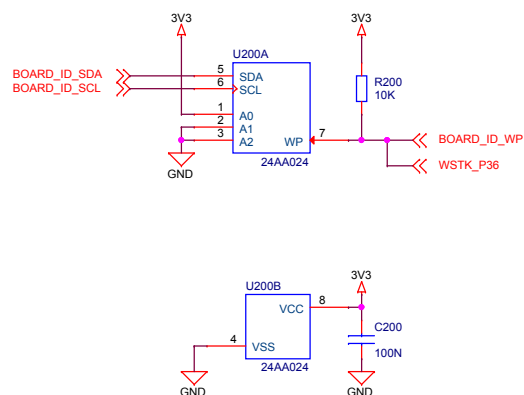
WSTK Connectors



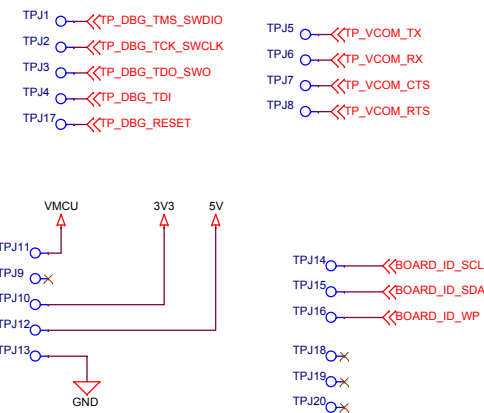
WSTK Power Decoupling



Board Identification



Test Points



<Schematic Path>
SCHEMATIC1

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		MGM12P Module Carrier Board	
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Design Created Date: Monday, April 02, 2012		Sheet Created Date: Tuesday, April 03, 2012	Sheet Modified Date: Friday, July 13, 2018
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