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<div>D</div> <div>C</div> <div>B</div> <div>A</div>	<div> <div> <div>EZR32WG WSTK Radio Board</div> <div>868 MHz +13dBm Direct Tie</div> <table> <tr> <th>Board Function</th><th>Page</th></tr> <tr> <td>Title Page</td><td>1</td></tr> <tr> <td>Power & Crystals & Board ID</td><td>2</td></tr> <tr> <td>Antenna & Radio Interface</td><td>3</td></tr> <tr> <td>I/O Port Pins</td><td>4</td></tr> <tr> <td>WSTK Connectors & Pin Mapping</td><td>5</td></tr> </table> </div> <div>  <div>PCB4502C</div> </div> </div>	Board Function	Page	Title Page	1	Power & Crystals & Board ID	2	Antenna & Radio Interface	3	I/O Port Pins	4	WSTK Connectors & Pin Mapping	5	<div>  <div>SILICON LABS®</div> </div>	<div> <div>Revision History</div> <table> <tr> <th>Rev.</th><th>Description</th></tr> <tr> <td>PA00</td><td>Initial version.</td></tr> <tr> <td>PA01</td><td>Correcting USB section; Changing type of USB conn.</td></tr> <tr> <td>PA02</td><td>Deleting USB_ID; No ext. HFXO for MCU; New DISP_EXTCOMIN mapping, D400 type.</td></tr> <tr><td> </td><td> </td></tr> <tr><td> </td><td> </td></tr> <tr><td> </td><td> </td></tr> <tr><td> </td><td> </td></tr> <tr><td> </td><td> </td></tr> <tr><td> </td><td> </td></tr> </table> <div> <div><Schematic Path></div> <div>SCHEMATIC1</div> </div> <div> <table> <tr> <td colspan="2">  <div>SILICON LABS®</div> </td> <td colspan="2"> <div>Schematic Title</div> <div>EZR32WG 868MHz DT WSTK Radio Board</div> </td> </tr> <tr> <td colspan="2"> <div>Designed:</div> <div>TAB</div> </td> <td colspan="2"> <div>Approved:</div> <div>DDB</div> </td> </tr> <tr> <td> <div>Size</div> <div>A3</div> </td> <td> <div>BOM Doc No:</div> <div><Cage Code></div> </td> <td colspan="2"> <div>Page Title</div> <div>Title Page</div> </td> </tr> <tr> <td colspan="2"> <div>Design Created Date:</div> <div>Monday, April 02, 2012</div> </td> <td> <div>Document number</div> <div>BRD4502C</div> </td> <td> <div>Revision</div> <div>A00</div> </td> </tr> <tr> <td colspan="2"> <div>Sheet Created Date</div> <div>Monday, April 02, 2012</div> </td> <td> <div>Sheet Modified Date</div> <div>Wednesday, October 22, 2014</div> </td> <td> <div>Sheet</div> <div>1 of 5</div> </td> </tr> </table> </div> </div>	Rev.	Description	PA00	Initial version.	PA01	Correcting USB section; Changing type of USB conn.	PA02	Deleting USB_ID; No ext. HFXO for MCU; New DISP_EXTCOMIN mapping, D400 type.													 <div>SILICON LABS®</div>		<div>Schematic Title</div> <div>EZR32WG 868MHz DT WSTK Radio Board</div>		<div>Designed:</div> <div>TAB</div>		<div>Approved:</div> <div>DDB</div>		<div>Size</div> <div>A3</div>	<div>BOM Doc No:</div> <div><Cage Code></div>	<div>Page Title</div> <div>Title Page</div>		<div>Design Created Date:</div> <div>Monday, April 02, 2012</div>		<div>Document number</div> <div>BRD4502C</div>	<div>Revision</div> <div>A00</div>	<div>Sheet Created Date</div> <div>Monday, April 02, 2012</div>		<div>Sheet Modified Date</div> <div>Wednesday, October 22, 2014</div>	<div>Sheet</div> <div>1 of 5</div>	<div> <div>5</div> <div>4</div> <div>3</div> <div>2</div> <div>1</div> </div>
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SILICON LABS

EZR32WG WSTK Radio Board
868 MHz +13dBm Direct Tie

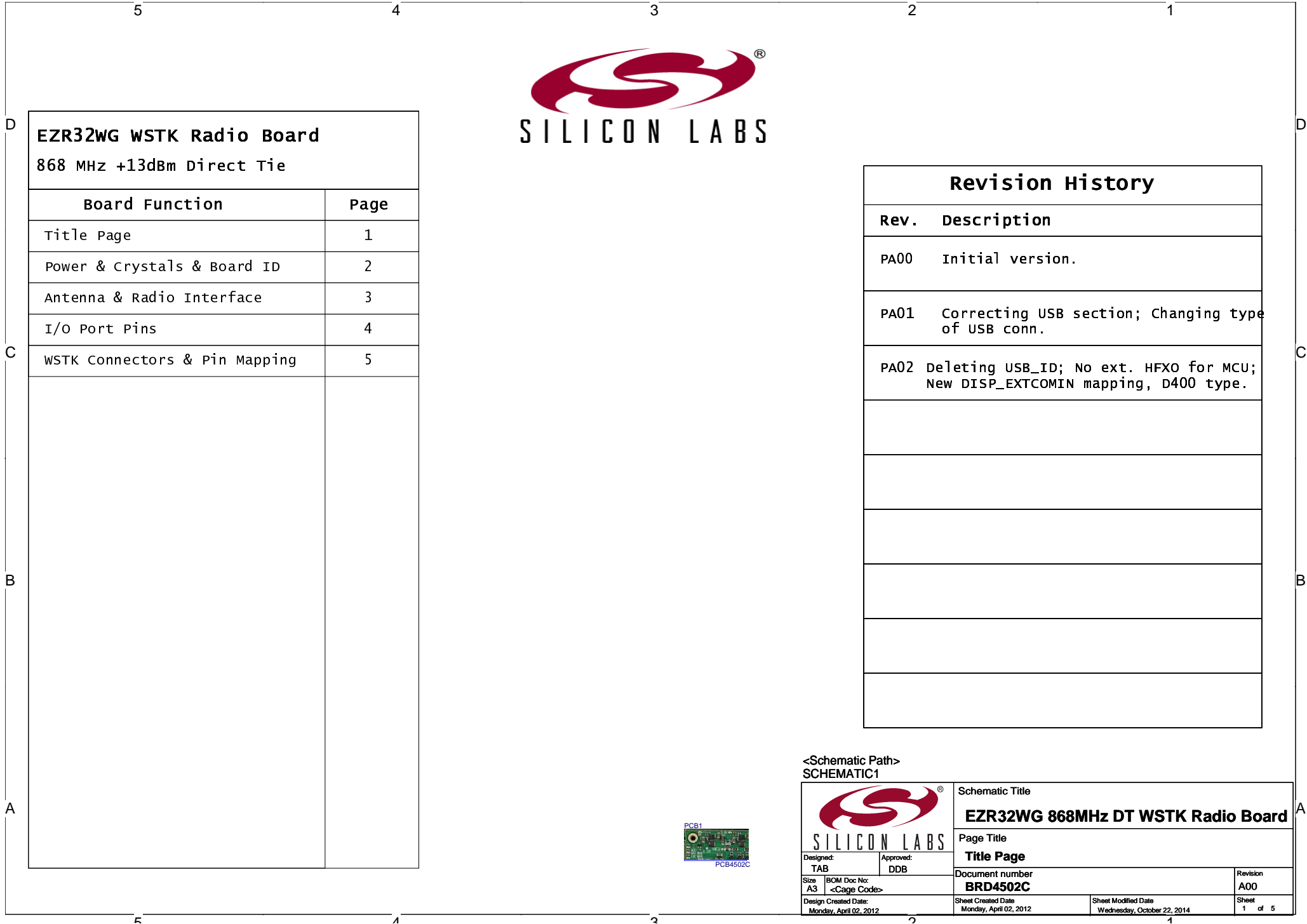
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SCHEMATIC1

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SILICON LABS

EZR32WG WSTK Radio Board
868 MHz +13dBm Direct Tie

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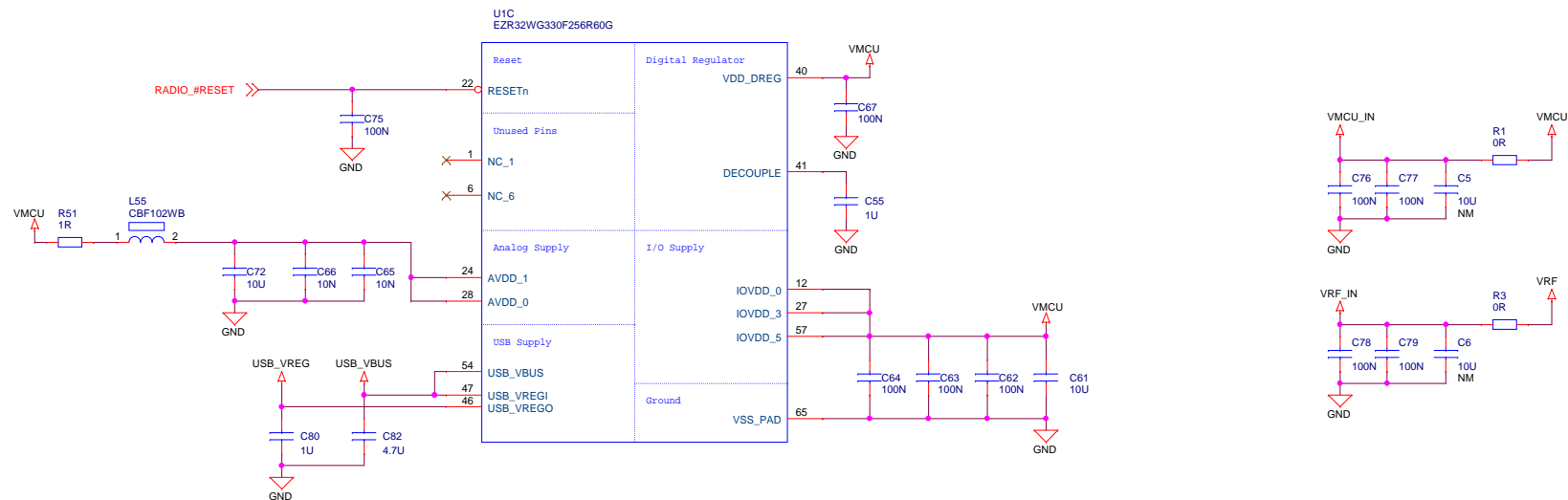
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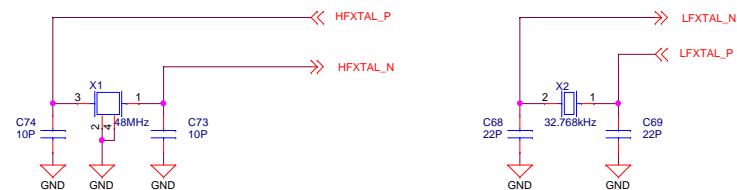
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Power & Decoupling

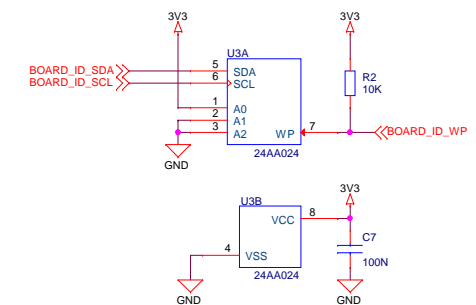


High Frequency & Low Frequency Crystals for MCU



Board Identification

Board ID



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SCHEMATIC1

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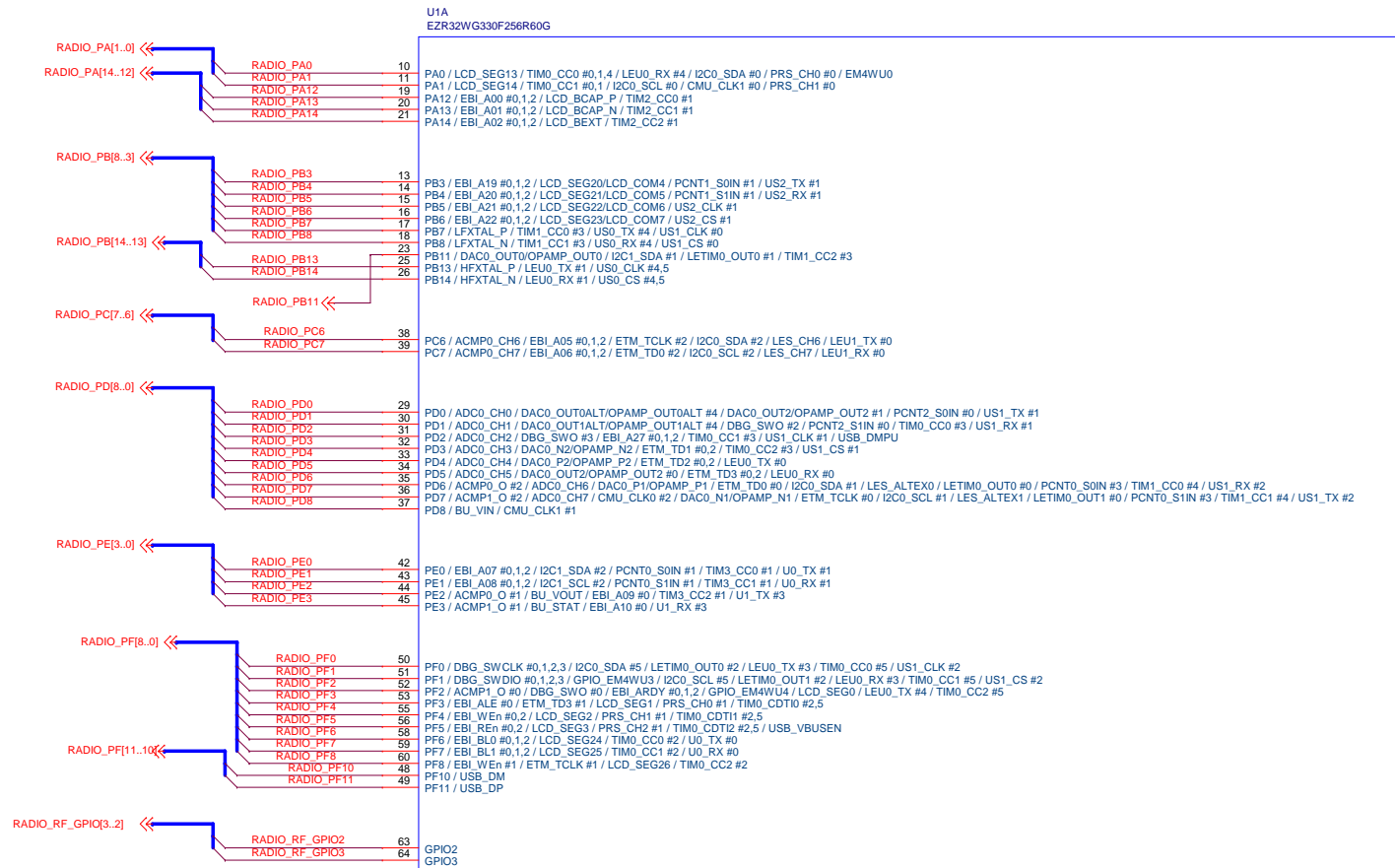
The schematic diagram illustrates the RF front-end circuit for the EZR32WG330F256R60G SoC. The circuit is divided into several functional blocks:

- LNA Balun (U1B):** This block is connected to the VDD_RF pins (7, 9) and the RXN pin (3). It includes components CR1 (3P), CR2 (1P), LR1 (20N), and LR2 (24N).
- PA matching:** This block is connected to the TXN pin (4) and the TXAMP pin (8). It includes components LC (120N), L0 (19N), C0 (3.6P), LM (6.8N), LM2 (6.8N), CM (5.1P), CM2 (10P), CM3 (5.1P), and CC1 (68P).
- Filter:** This block is connected to the TXN pin (4) and the TXAMP pin (8). It includes components CM (5.1P), CM2 (10P), CM3 (5.1P), and CC1 (68P).
- Antenna connector (P1):** This block is connected to the TXN pin (4) and the TXAMP pin (8). It includes components CM (5.1P), CM2 (10P), CM3 (5.1P), and CC1 (68P).

The circuit also includes a VRF input, a VDD_RF input, and a TXAMP input. The output of the circuit is connected to an SMA connector (P1).

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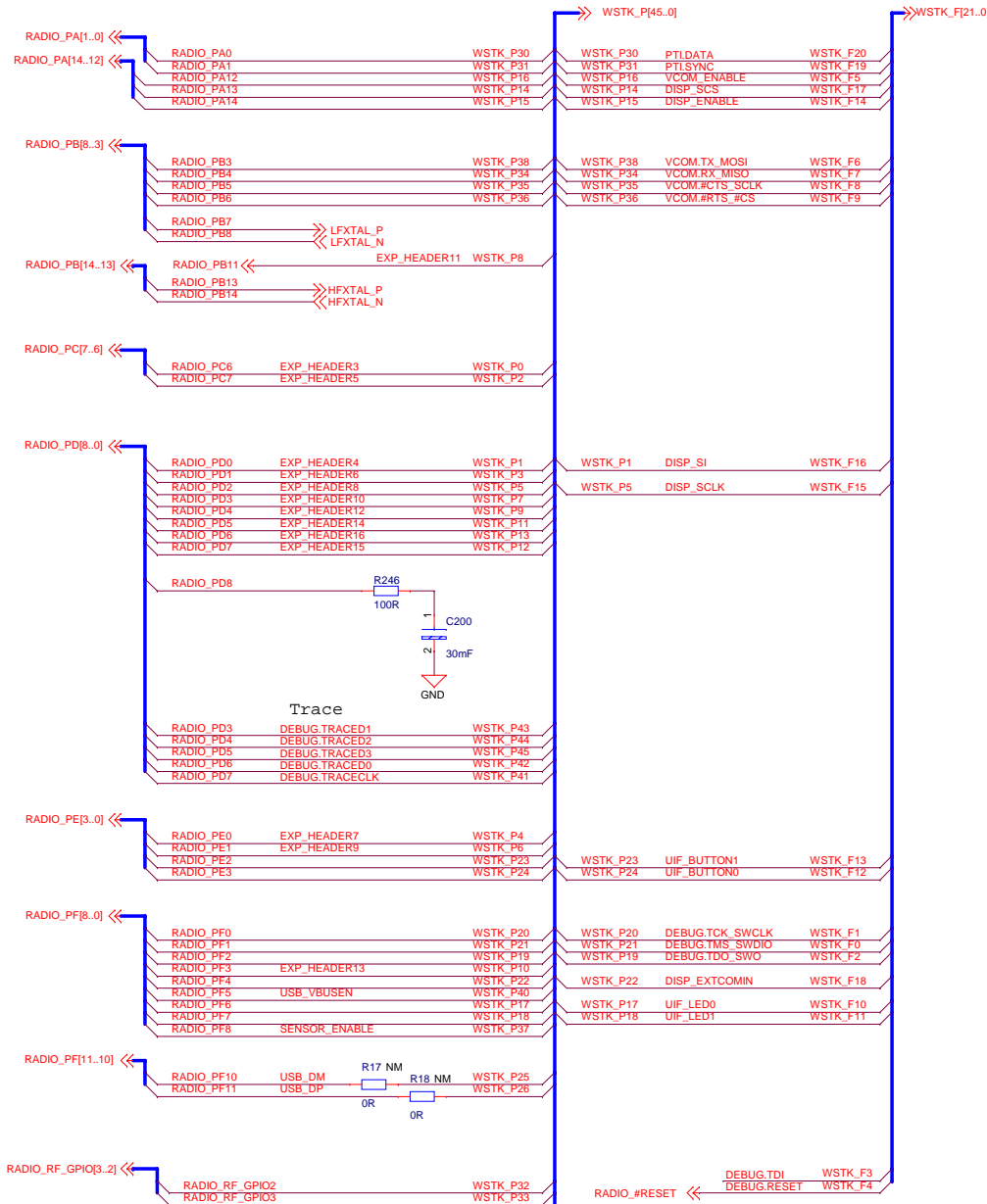
I/O Port Pins



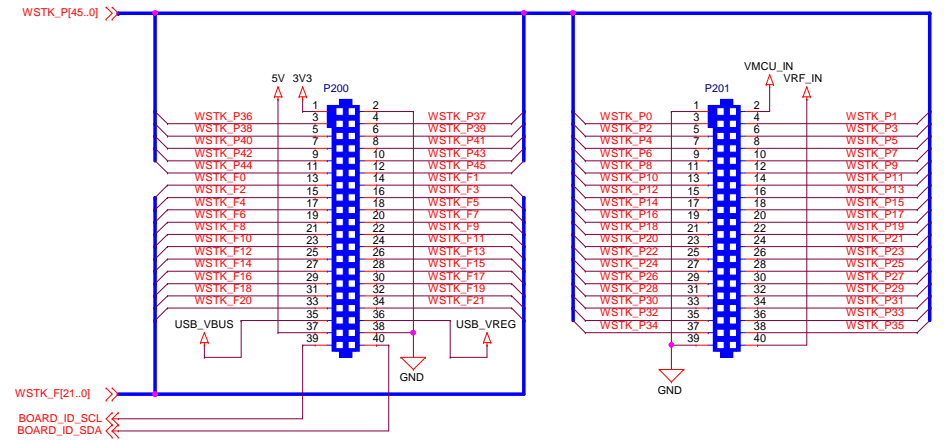
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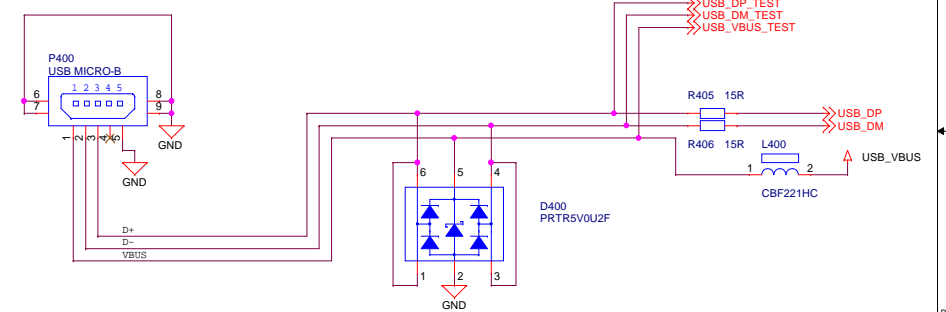
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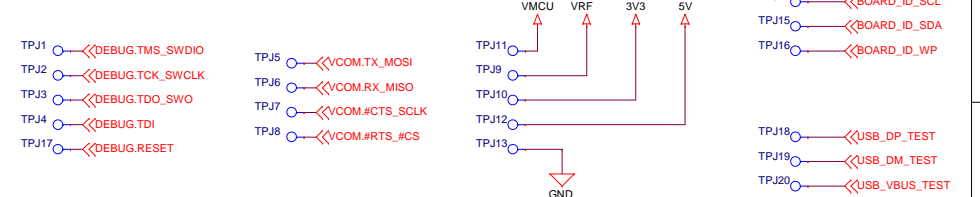
WSTK Connectors



USB Connection and ESD protection



Test Points



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