



EFM8UB1 Universal Bee STK

Board Function	Page
Title Page	1
User Interface	2
Signal Assignments	3
EFM8 Power & I/O	4
Target Voltage Supply	5
AEM	6
Debug Interface	7
Simplicity & VCOM	8
Power	9
Board Controller	10
Board Controller Misc	11



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Revision History

Rev.	Description
A00	Update to new STK platform

SILICON LABS		Board Name EFM8UB1 Universal Bee STK	
		Page Title Title Page	
Designed SKV	Approved RGU	Board Number BRD5000B	Revision A00
Size A3	Sheet Modified Date Tuesday, June 22, 2021	Copyright Silicon Laboratories Inc. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE	
		Sheet 1 of 11	

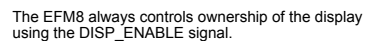
5



C



A

5

4



2



1

2	VMCU		
4	P1.0	SPI0_MOSI	CMP1.0/ADC0.8
6	P0.7	SPI0_MISO	CMP0.7/ADC0.7
8	P0.6	SPI0_SCK	CMP0.6/ADC0.6
10	P1.1	SPI0_NSS	CMP1.1/ADC0.9
12	P2.1	UART1_TX	CMP1.10/ADC0.21
14	P2.2	UART1_RX	CMP1.11/ADC0.22
16	P1.2	I2C0_SDA	CMP1.2/ADC0.10
18	5V		
20	3V3		

1



Page Title
User Interface

Revision	A00
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Sheet
2 of 11

D



B



1



2

D



D



B

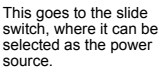
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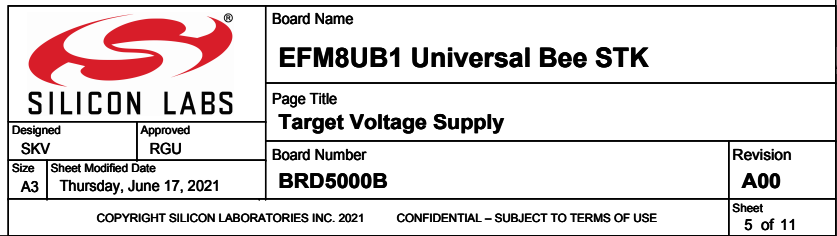
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A



Calibration currents include contribution from sense and bleeder resistors.

Calibration currents include contribution from sense and bleeder resistors.



A

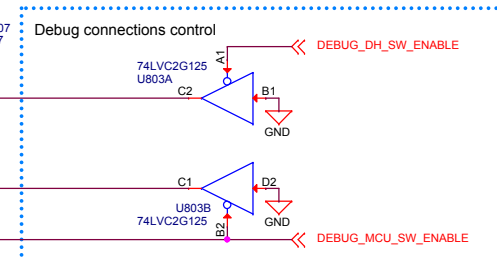
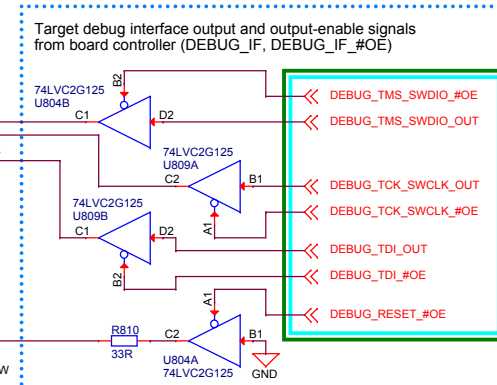
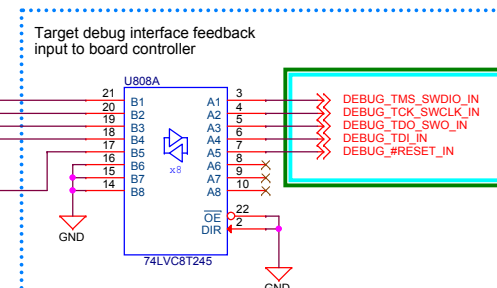
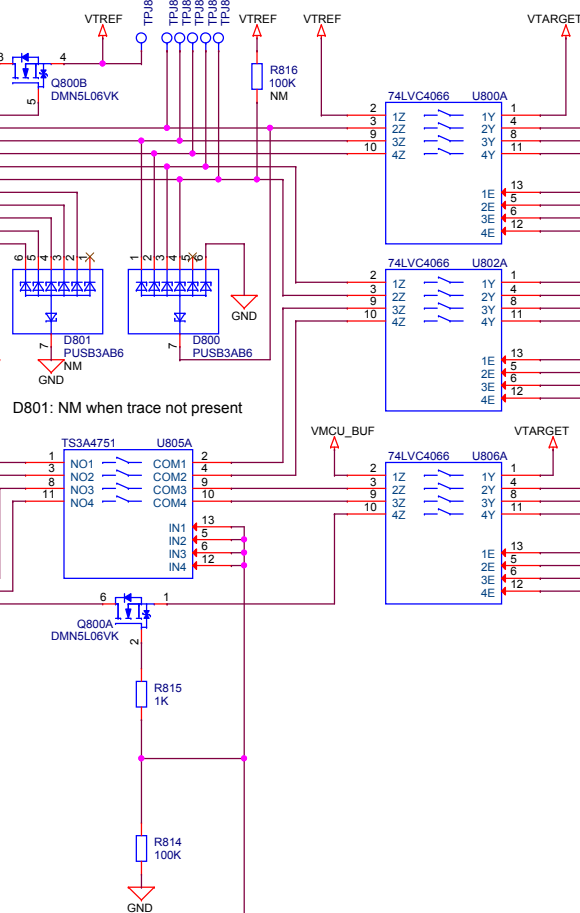
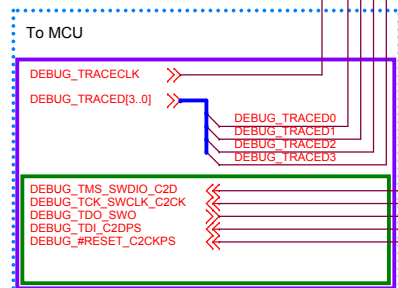


ARM Coresight 20-pin
Debug + ETM header

P800

Pin	Signal
1	DH TMS SWDIO
2	DH TCK SWCLK
3	DH TDO SWO
4	DH TDI
5	DH #RESET
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	

GND



Mode	DEBUG_DH_SW_ENABLE	DEBUG_MCU_SW_ENABLE	DEBUG_IF_#OE	VTREF	VTARGET
Debug Out	1	0	0/1	External voltage	External voltage
MCU Debug	0	1	0/1	Disconnected	VMCU
Debug In	1	1	1	VMCU	VMCU
Debug Off	0	0	1	-	-

Color coded frames indicates which groups of signal nodes that are active in a given debug mode



Board Name

EFM8UB1 Universal Bee STK

Page Title	Debug Interface
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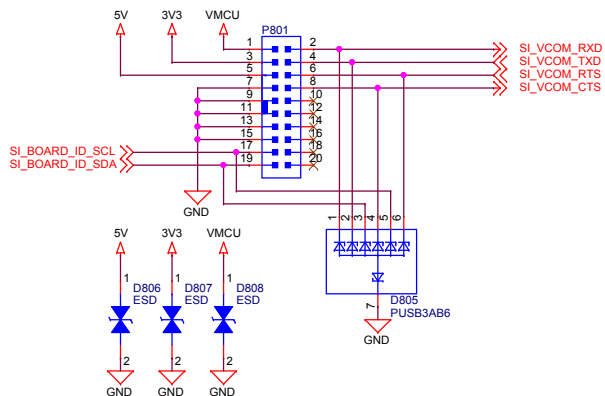
Board Number	BRD5000B
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Revision	A00
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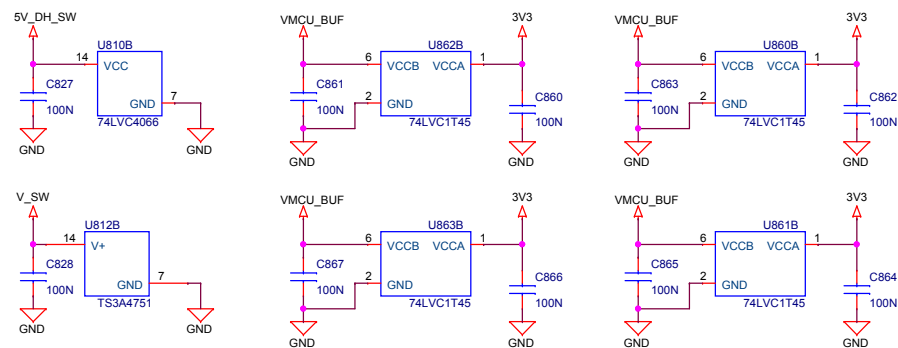
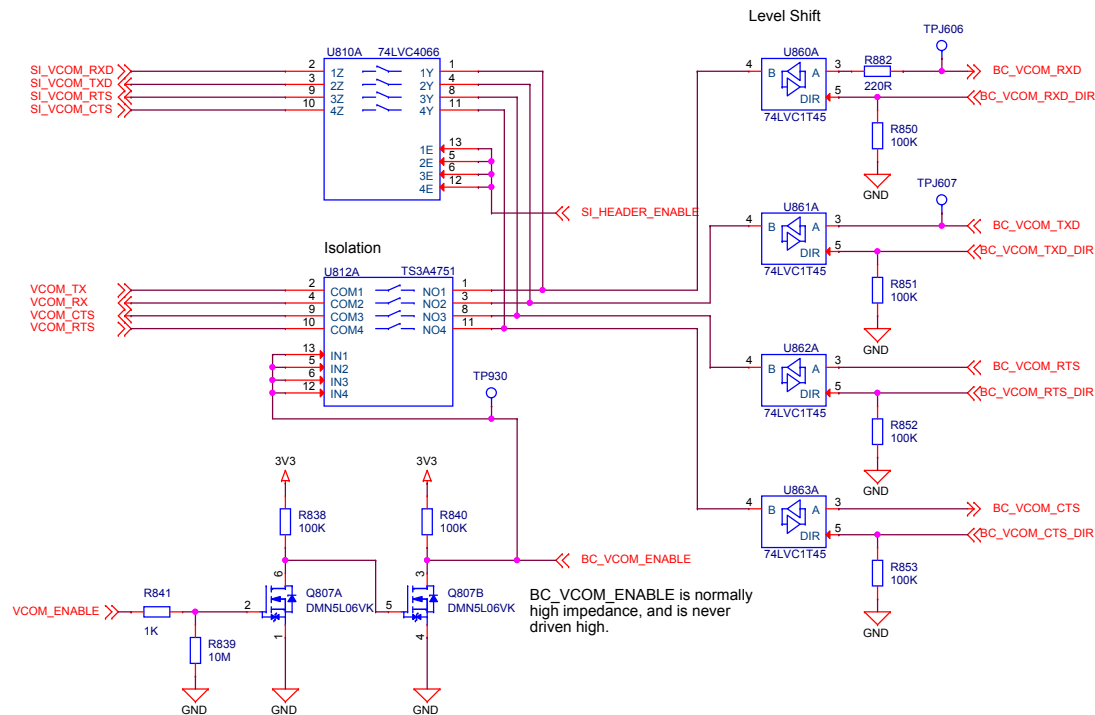
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Sheet
7 of 11

Simplicity Connector



VCOM Interface



		Board Name	
		EFM8UB1 Universal Bee STK	
Designed SKV		Page Title	
Size A3		Simplicity & VCOM	
Sheet Modified Date Thursday, June 17, 2021		Board Number	
		BRD5000B	
		Revision	
		A00	
		Sheet 8 of 11	

J-Link USB Port

WR_COM_USB_MINI_B

P601

1 2 3 4 5

6 7 8 9

Place these TPs close to USB header

TPJ614

TPJ613

5V

L600

742792662

1 2

USB_DP

USB_DM

TPJ611

TPJ612

D600

DT1446-04

6 5 4

2

GND

3V3 Regulator

The schematic diagram illustrates a 3V3 Regulator circuit. The central component is the LP3982ILD-ADJ (U600) voltage regulator. The input (IN, pin 2) is connected to a 5V supply through a 100nF capacitor (C600) and a 10uF capacitor (C611). The shutdown pin (SHDN, pin 7) is connected to the input through a 10k resistor (R600). The ground pins (GND, GND_HEAT, CC, pins 3, 9, 6) are connected to ground. The output (OUT1, pin 1) is connected to a 3V3 output through a 180k resistor (R601) and a 33nF capacitor (C602). The fault pin (FAULT, pin 8) is connected to ground through a 110k resistor (R602). The output is also connected to a 10uF capacitor (C607) and a TPJ600 test point. Three LEDs (M1, M2, M3) are connected to ground.

C

VTARGET Voltage Mirror

5V

R690 33R

C652 10U

U622B MCP6001T

VDD

GND

2

GND

VTARGET

R629 1K

C653 100N

U622A MCP6001T

3

4

1

GND

C654 100P

R689 10K

5V

Q605 BC846BWT1G

R686 0R

R688 4K7

R687 3R3

VTARGET_BUF

C655 10U

GND

GND

B

Power Supply for Analog Switches

Analog switches used for isolation are powered by 3V6_SW when the USB cable is connected, otherwise by VMCU.

J-Link USB Cable	PMOS State	NMOS State	V_SW	VMCU_SENSE
Connected	Off	On	3.6V	VMCU
Disconnected	On	Off	VMCU	Isolated

The circuit diagram illustrates the power supply for the analog switches. A 5V input is connected to the IN pin of U603 (TLV70536). The EN pin of U603 is connected to the A2 pin of C609 (1uF capacitor) and the B2 pin of U603. The OUT pin of U603 is connected to the B1 pin of U603 and the A1 pin of C608 (1uF capacitor). The GND pins of both capacitors are connected to ground. The output of the switch is connected to the 3V6_SW line. Additionally, the VMCU line is connected to the 5V input through a resistor R622 (47R).

VMCU Voltage Mirror

The schematic diagram illustrates the VMCU Voltage Mirror circuit, divided into three main sections: 5, 4, and 3.

Section 5: A buffer stage using the MCP6001T (U606B) op-amp. The input is connected to the non-inverting input (+), and the output is connected to the inverting input (-) and the output pin. A 10uF capacitor (C660) is connected between the input and ground. The output is labeled 5V_BUF.

Section 4: An isolation stage using the DMN5L06VK (Q601B) MOSFET. The gate is connected to the 5V_SW input. The drain is connected to the output of Section 5 through a 1M resistor (R628). The source is connected to ground.

Section 3: A voltage divider and buffer stage. The output of Section 4 is connected to the non-inverting input (+) of the MCP6001T (U606A) op-amp through a 1K resistor (R672). The inverting input (-) is connected to ground through a 100nF capacitor (C621) and a 100pF capacitor (C620). The output of the op-amp is connected to the base of the BC846BWT1G (Q602) MOSFET through a 0R resistor (R679). The emitter of the MOSFET is connected to ground through a 4K7 resistor (R674). The collector is connected to the output VMCU_BUF through a 3R3 resistor (R675). A 10uF capacitor (C625) is connected between the output and ground.

The diagram shows a red wire connected to a blue wire through a resistor R623 (10K) and a capacitor C610 (1N). Both components are connected to ground (GND).

[illegible]

Power & Decoupling

B

A

Board ID & Button Isolation

BC Serial Flash

Board Version

SILICON LABS

Board Name
EFM8UB1 Universal Bee STK

Page Title
Board Controller

Board Number
BRD5000B

Revision
A00

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Sheet 10 of 11

Board ID & Button Isolation

BC Serial Flash

Board Version

SILICON LABS

Designed SKV	Approved RGU
Size A3	Sheet Modified Date Thursday, June 17, 2021

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Board Name	
EFM8UB1 Universal Bee STK	
Page Title	
Board Controller	
Board Number	Revision
BRD5000B	A00
Sheet	
10 of 11	

BC Serial Flash

BC_SPI_COP1
BC_SPI_SCLK
3V3
R906 10K
BC_SPI_CS
BC_SPI_CPO
U902A
D2
E1
A3
E3
C1
SI / SIO0
SCLK
CS#
WP# / SIO2
RESET# / SIO3
SO / SIO1
C3
MX25R8035F
3V3
U902B
VCC
GND
B2
C914 100N
GND
GND
MX25R8035F
BOARD_VER0
BOARD_VER1
R931 1K
R930 1K
GND
GND

Board Version

BOARD_VER0
BOARD_VER1
R931 1K
R930 1K
GND
GND

Name	
M8UB1 Universal Bee STK	
Title	
Board Controller	
Part Number	Revision
D5000B	A00
INC. 2021	Sheet
CONFIDENTIAL – SUBJECT TO TERMS OF USE	10 of 11

1

BC Serial Flash

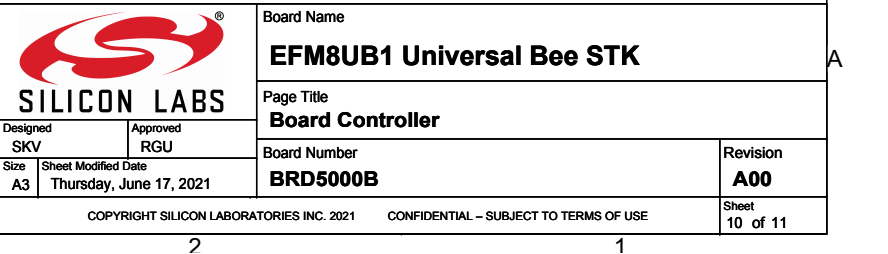
BC_SPI_COP1
BC_SPI_SCLK
3V3
R906 10K
BC_SPI_CS
BC_SPI_CPO
U902A
D2
E1
A3
E3
C1
SI / SIO0
SCLK
CS#
WP# / SIO2
RESET# / SIO3
SO / SIO1
C3
MX25R8035F
3V3
U902B
VCC
GND
B2
C914 100N
GND
MX25R8035F
GND
BOARD_VER0
BOARD_VER1
R931 1K
R930 1K
GND
GND

Board Version

BOARD_VER0
BOARD_VER1
R931 1K
R930 1K
GND
GND

Name	
M8UB1 Universal Bee STK	
Title	
Board Controller	
Part Number	Revision
D5000B	A00
INC. 2021	Sheet
CONFIDENTIAL – SUBJECT TO TERMS OF USE	10 of 11

1



Board Name EFM8UB1 Universal Bee STK		A
Page Title Board Controller		
Board Number BRD5000B	Revision A00	
LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE		Sheet 10 of 11

Board Name EFM8UB1 Universal Bee STK		A
Page Title Board Controller		
Board Number BRD5000B	Revision A00	
LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE		Sheet 10 of 11

Board Name EFM8UB1 Universal Bee STK		A
Page Title Board Controller		
Board Number BRD5000B	Revision A00	
LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE		Sheet 10 of 11

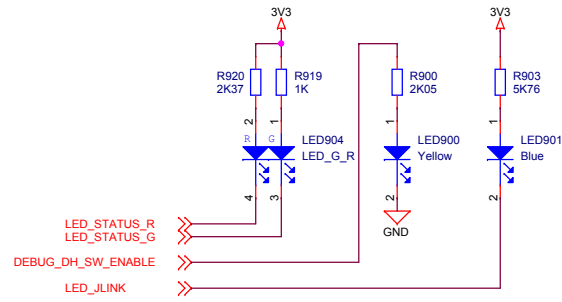
Board Name EFM8UB1 Universal Bee STK		A
Page Title Board Controller		
Board Number BRD5000B	Revision A00	
LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE		Sheet 10 of 11

Board Name EFM8UB1 Universal Bee STK		A
Page Title Board Controller		
Board Number BRD5000B	Revision A00	
LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE		Sheet 10 of 11

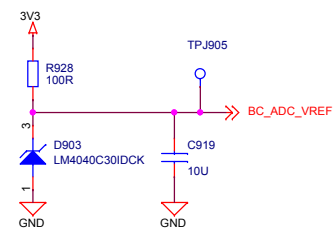
Board Name EFM8UB1 Universal Bee STK		A
Page Title Board Controller		
Board Number BRD5000B	Revision A00	
LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE		Sheet 10 of 11

Board Name EFM8UB1 Universal Bee STK		A
Page Title Board Controller		
Board Number BRD5000B	Revision A00	
LABORATORIES INC. 2021 CONFIDENTIAL – SUBJECT TO TERMS OF USE		Sheet 10 of 11

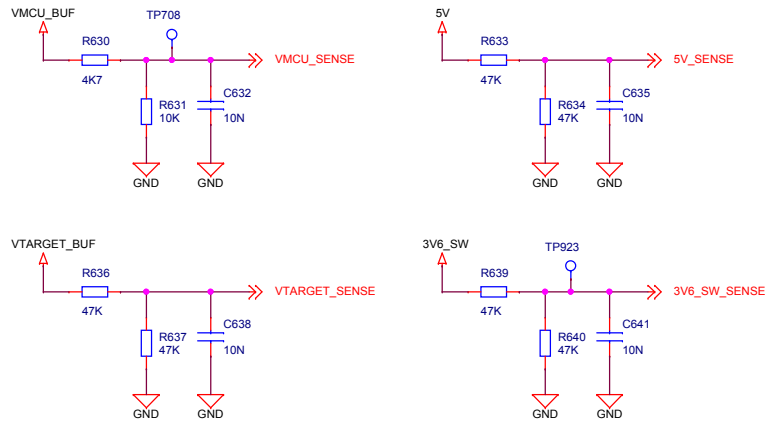
Indicator LEDs



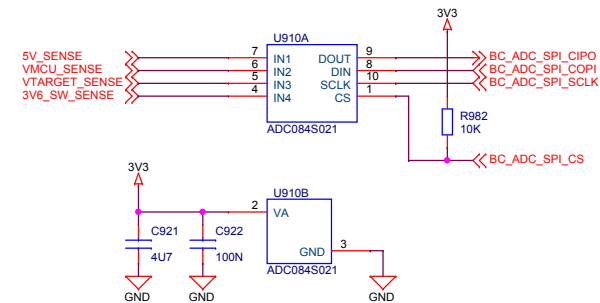
BC ADC Reference



BC Voltage Sense



BC Voltage Sense ADC



		Board Name	
		EFM8UB1 Universal Bee STK	
Designed SKV		Page Title	
Size A3		Board Controller Misc	
Sheet Modified Date Thursday, June 17, 2021		Board Number	Revision
		BRD5000B	A00
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